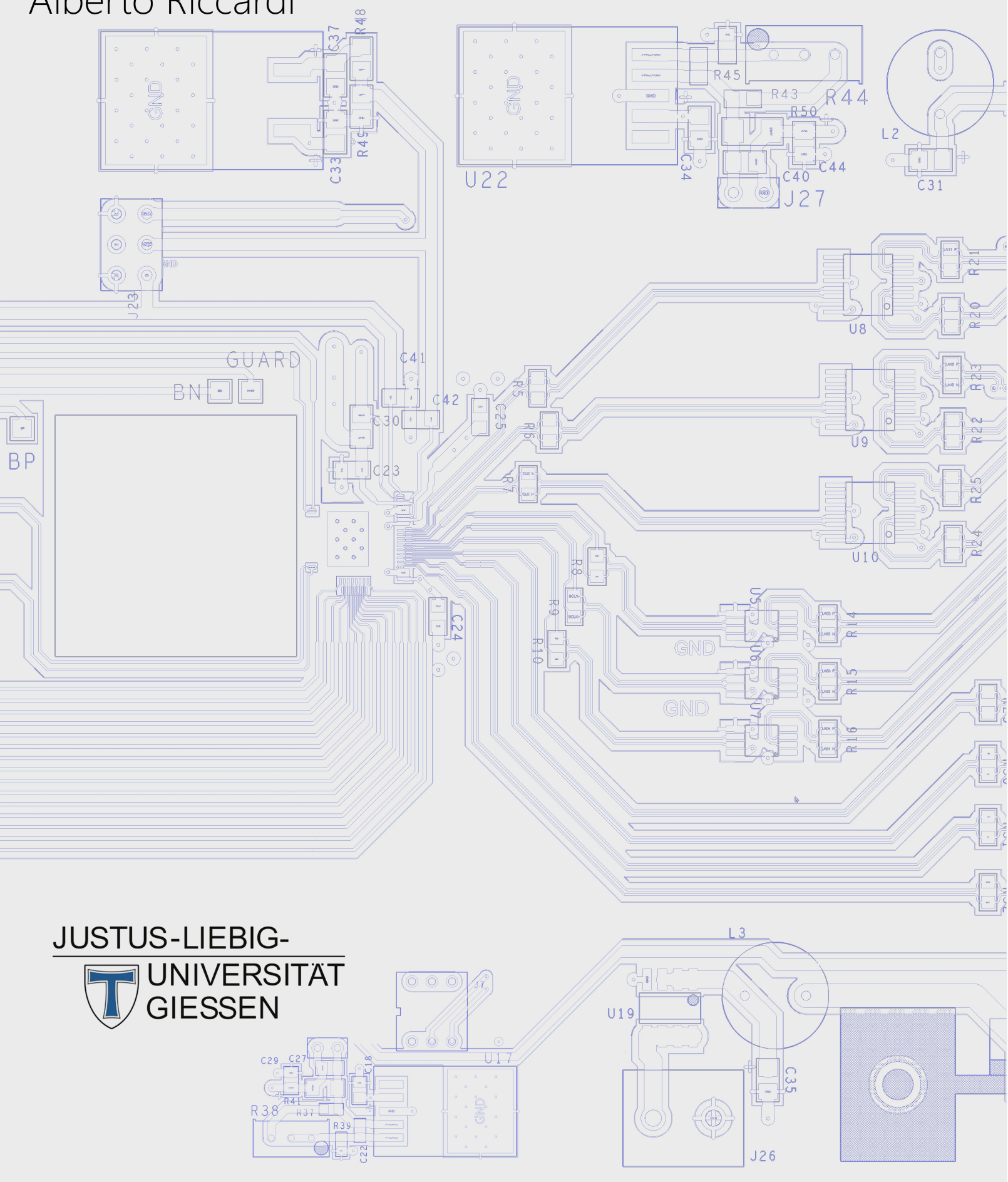
LOW POWER INTEGRATED SYSTEM FOR A SIMULTANEOUS TIME AND ENERGY MEASUREMENT IN THE PANDA MICRO-STRIP DETECTOR

Alberto Riccardi



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Low power integrated system for a simultaneous time and energy measurement in the $\overline{P}ANDA$ micro-strip detector

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Alberto Riccardi

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Dekan:	Prof. Dr. Bernhard Mühlherr
Prodekan:	Prof. Dr. Kai-Thomas Brinkmann
Betreuer und 1. Gutachter:	Prof. Dr. Kai-Thomas Brinkmann
2. Gutachter	Prof. Dr. Claudia Höhne

ABSTRACT

The $\overline{P}ANDA$ experiment is one of the main projects foreseen at the Facility for Antiproton and Ion Research (FAIR). Its task is to measure the products of the reactions between an antiproton beam, with a beam momentum between 1.5 GeV/c and 15 GeV/c, and a proton or nucleon fixed target. In order to acquire data on many physics channels at the same time, it is necessary to have a trigger less experiment.
The innermost detector of $\overline{P}ANDA$ is the Micro Vertex Detector (MVD). The MVD has to distinguish secondary vertexes from the primary one. The detector is composed of two structures, the barrels and the disks, equipped with two types of sensors: silicon hybrid pixels and double-sided silicon micro strips.
The main purpose of this thesis is the design and the first characterisation of PANDA STrip ASIC (PASTA). After a brief overview of the experiment, a complete description of the chip is given. In this part, the motivations that lead to the development of this prototype and the measurement concept are explained. Moreover, the behaviour of all the building blocks, with a particular attention on the analog structures, is shown. In the last part of the thesis the layout, with few details about the implementation of the channels and how the chip was assembled, is described. Finally, after an overview of the experimental setups, the first laboratory analysis of the chip and a preliminary characterisation of a typical channel are reported.

ZUSAMMENFASSUNG

Das PANDA Experiment ist eines der Hauptprojekte an der im Aufbau befindlichen Beschleunigerzentrum FAIR (Facility for Antiproton and Ion Research). Bei diesem Experiment werden die Reaktionsprodukte, die in Antiproton-Proton- bzw. Antiproton-Kern-Kollisionen mit ruhendem Target entstehen, vermessen. Der hierbei zum Einsatz kommende Antiprotonenstrahl deckt einen Impulsbereich von 1.5 GeV/c bis 15 GeV/c ab.
Um Daten für möglichst viele physikalische Fragestellungen gleichzeitig aufnehmen zu können wird das Experiment mit freilaufendem Trigger durchgeführt.
Der Micro Vertex Detektor (MVD) ist beim PANDA Experiment die strahlnächste Detektorkomponente. Seine Aufgabe ist es unter anderem, die Trennung sekundärer Vertices vom primären Interaktionspunkt zu ermöglichen. Der Detektor besteht aus zwei wesentlichen Teilen, den vier konzentrisch um die Strahlachse angebrachten, zylindrischen 'Barrels' sowie den sechs in Vorwärtsrichtung angebrachten 'Discs' (Scheiben). Hierbei kommen zwei Arten von Sensoren zum Einsatz, Silizium-Hybrid-Pixel und doppelseitige Silizium-Microstrips.
Ziel dieser Arbeit ist das Design und erste Charakterisierungsmessungen des PANDA STrip ASIC (PASTA). Nach einem kurzen Überblick über das PANDA Experiment wird der Chip detailiert beschrieben. Hierbei wird auf die Motivation für die Entwicklung eines eigenen Chip-Prototyps sowie die prinzipiellen Messkonzepte eingegangen. Zudem wird das Verhalten der einzelnen Komponenten, mit besonderem Augenmerk auf den Analogteil, beschrieben.
Im Weiteren wird auf das Layout und die Implementierung der Kanäle sowie die eigentliche Fertigung des Chips eingegangen. Abschließend, nach einer Beschreibung der relevanten experimentellen Aufbauten, werden die ersten Labormessungen sowie eine vorläufige Charakterisierung eines typischen Kanals gezeigt.

CONTENTS

1

$\overline{P}ANDA$ EXPERIMENT

1.1 Overview of FAIR

The antiProton ANnihilation at DArmstadt ($\overline{P}ANDA$) experiment is one of the main pillars of the Facility for Antiproton and Ion Research (FAIR) which is under construction in Darmstadt (Germany). The facility, as shown in Figure 1.1, is based on the already existing GSI Helmholtzzentrum für Schwerionenforschung GmbH (GSI) center, which will be the first part of the acceleration chain (blue line). The new structure will have several accelerator rings, the red part of the picture, while in green the four pillars are denoted that group all the different experiments present at FAIR.

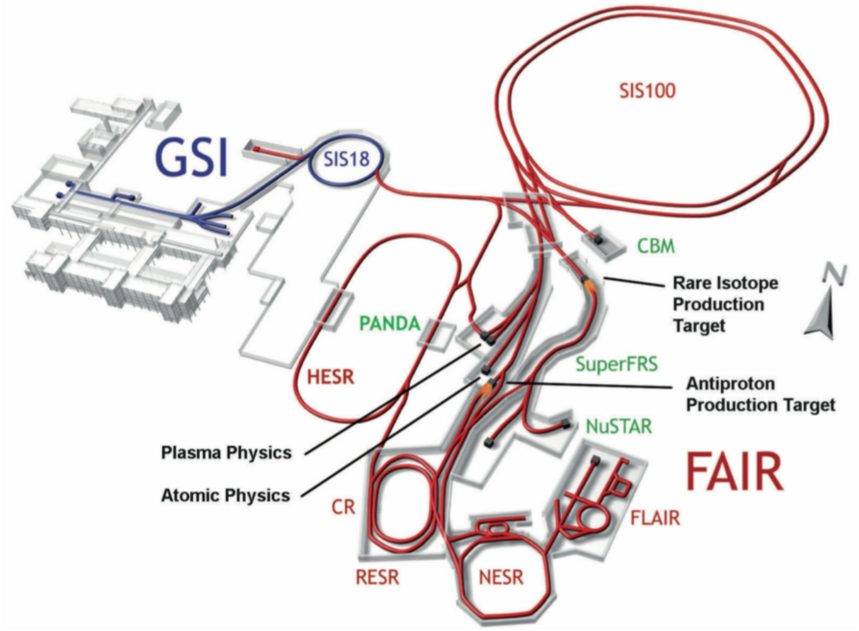


Figure 1.1: Overview of the future FAIR facility.

The four pillars are in detail:[1] :

- Atomic, Plasma Physics and Applications (APPA): a set of smaller experiments that investigate plasma physics, ultra-strong electromagnetic fields and radiation effects on materials.
- Nuclear Structure, Astrophysics and Reactions (NuSTAR): like APPA, a collaboration of several experiments, but, in this case, the main task is related to nuclear structure and properties of heavy radioactive elements. Since these elements can be formed in star collapses there is a close connection between this project and astrophysics.
- Compressed Baryonic Matter (CBM): the fields of study are the Quantum ChromoDynamics (QCD) phase diagram in regions of high net baryon densities and moderate temperatures, the deconfinement towards quark-gluon plasma, and matter at neutron star-like densities.
- $\overline{P}ANDA$: like CBM, a complex detector, in this case the purpose is to study antiproton-proton annihilations in the charm mass regime and antiproton-nuclei interactions. More details about the physics program of $\overline{P}ANDA$ are presented in Section 1.2.

1.2 Physics program of $\overline{P}ANDA$

QCD is a relativistic quantum field theory of quarks and gluons interacting according to the laws of non-abelian forces between colour charges [2] and its Lagrangian density is:

$$\mathcal{L}_{\mathcal{QCD}} = -\frac{1}{4} G_a^{\mu\nu} G^a_{\mu\nu} + \sum_f \overline{q}_f [i\gamma^\mu D_\mu - m_f] q_f \tag{1.1}$$

where f represents the quark flavours, for $\overline{P}ANDA$ u, d, s, c. The gluon tensor is given by:

$$G_a^{\mu\nu} = \partial^\mu A_a^\nu - \partial^\mu A_a^\nu + g f_a^{bc} A_b^\mu A_c^\nu \tag{1.2}$$

and the gauge covariant derivative involving the gluon field A_a^μ:

$$D^\mu = \partial^\mu - i\frac{g}{2} A_a^\mu \lambda^a \tag{1.3}$$

g is related to the strong coupling constant as $\alpha_s(k^2) = \frac{g_s^2(k^2)}{4\pi}$.
For the high energy regime, a perturbative approach is allowed if the running coupling constant α_s is smaller than 0.1180 [3].

QCD, as part of the Standard Model, is well understood and tested at high energies [4, 5, 6]. In these conditions, the interaction between quarks and gluons can be described using perturbation theory. However, in the low energy range, QCD becomes a strongly coupled theory and perturbation theory can not be applied. In this regime, many aspects are not yet well understood and a lot of questions are still open. So far, there is not a unique descriptive framework.. The existing framework can be studied with two approaches: the Effective Field Theories (EFT) and the Lattice Quantum ChromoDynamics (LQCD) methods.

Effective Field Theories

The principle of these theories is to study the strong interaction in a specific regime in a different way, integrating out the degrees of freedom (related for example to high energies) in order to define a scale separation. The Non-Relativistic QCD theory is an example in which heavy quarks are considered to be non-relativistic [7]. Since the gluon dynamics depend on the heavy quark velocity, in the case of $\overline{P}ANDA$ it depends on the charm quark.
These theories, with hadronic degrees of freedom, have been developed for the description of meson and baryon class properties, since they can provide input to lattice calculations. For the physics program of $\overline{P}ANDA$ it is possible to use these theories to study hypernuclear dynamics, baryon and open-charm spectroscopy [2].
One more example of EFT, this time based on the partial chiral symmetry of the QCD Lagrangian, is the Chiral Perturbation Theory (ChPT) [8]. This approach can be applied since quark masses are finite, but it is possible to approximate the light quarks, if compared with the hadronic scales, as massless degenerate states. For ChPT there is a spontaneous breaking of the higher chiral symmetry due to hadronic degrees of freedom at low energies. Within the $\overline{P}ANDA$ physics program, this approach may help the study of possible exotic states in the open-charm sector. Previous studies have already demonstrated that prediction for exotic states can be made, in particular for πD and ηD^* channels [9].

Lattice Quantum Chromo Dynamics

This theory is based on the study of the equations of motion of the QCD Lagrangian, discretising the space-time into a four-dimensional lattice and numerically solving the equations, with a large scale of simulations [10]. For the sake of simplicity, some boundary conditions can be applied and the Z partition function is written as similar as possible to a Feynman's path integral:

$$Z = \int D_\varphi(x,\tau) e^{-S_E[(x,\tau)]} \tag{1.4}$$

In equation 1.4, φ is the field in terms of Feynman's integrals, D_φ is its differential and S_E is the Euclidean action. One of the main problems concerns the calculation requirements; for

this reason, several simplifications were adopted. Nowadays, since the computing capability has grown, it is possible to reduce the effects of these simplifications. The mass of some of the open-charm and open-bottom mesons can be calculated by LQCD, as well as the ones of charmonium and bottomonium states [11]. Moreover, studies of the proton form factor, which in $\overline{P}ANDA$ will be performed analysing the reaction $\overline{p}p \longrightarrow e^+e^-$, will also benefit from LQCD.

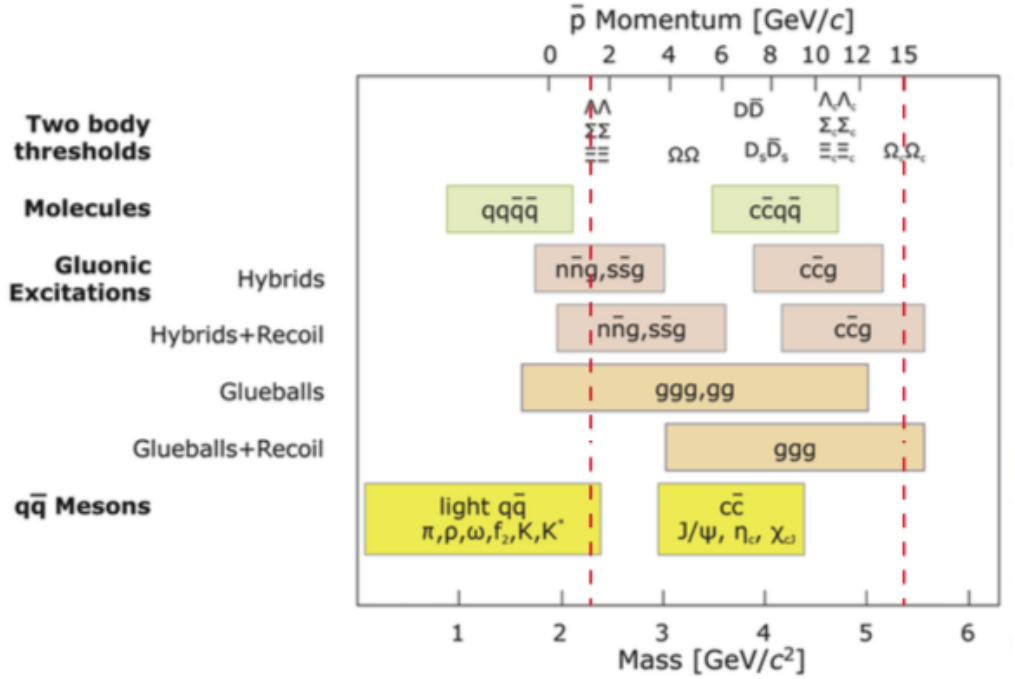


Figure 1.2: Available states as function of invariant mass and antiproton momentum [12].

The $\overline{P}ANDA$ experimental program comprises several topics related to the strong interaction, in particular, the investigation of QCD. The main goal of $\overline{P}ANDA$ is to answer some of the open questions in the QCD field, having a program designed to collect high-quality data. Using the High-Energy Storage Ring (HESR), described in Section 1.3.1, it is possible to have an antiproton beam in a high resolution mode. A precision of up to $\delta p/p = 10^{-5}$ and a resolution of the order of 30 keV [13] allows an accessible mass range from 2.2 GeV/c^2 to 5.5 GeV/c^2. The possible states to be studied are shown in Figure 1.2.

The $\overline{P}ANDA$ physics program can be summarised in four different pillars:

- Hadron spectroscopy
- Properties of hadrons in matter
- Nucleon structure
- Hypernuclei

1.2.1 Hadron spectroscopy

The first field of $\overline{P}ANDA$ is the classification and investigation of the hadronic bound state spectrum, with special attention to mesons that contain charm and baryons containing charm and strange quarks.

Charmonium spectroscopy

Charmonium, as a $c\bar{c}$ state, defines a group of neutral meson states. It is considered "hidden charm", since charmonium has a net charm of zero. The first experimental evidence of the charmonium, in particular; the J/ψ ($J^P = 1^-$), was found simultaneously in 1974 by two different groups. The first one is the group of RICHTER, AUGUSTIN, BOYARSKI, et al. at SLAC [14] and, the second is AUBERT, BECKER, et al. [15] at Brookhaven National Laboratory(BNL). Thanks to this discovery, both group leaders got the Nobel Prize in 1976. Even if the state was discovered a long time ago and many experiments were built to study the charmonium spectrum, there are regions of the spectrum that are still not understood. Eight states were discovered, as can be seen in Figure 1.3, in the region below the $D\overline{D}$ threshold, corresponding to 3.73 GeV. Note that in this region the energy is smaller than the one needed to form a couple of open-charmed ground state mesons. Some of these states have been measured precisely with an error of ten keV for their masses. Other states, like the singlet η_c, have not a precise mass measurement yet. The mass error for the η_c is 1.3 MeV and the one in the total width is 4 MeV [16].
In the Figure 1.3 the solid blacks line correspond to theoretical predictions while the experimental results are shown with shaded lines [18]. The red dots represent states that can be interpreted as charmonium states and consequently the most probable quantum number is shown. There are also states, in the right part of the graph, that don't fit any standard quantum number and for this reason they are called "exotic".
The contribution of $\overline{P}ANDA$ will not only be the measurement of exotic states with a higher precision but may also increase the resolution of the mass and width for states like the η_c. $\overline{P}ANDA$ is not the only charmonium oriented experiment, for example at Fermilab there are

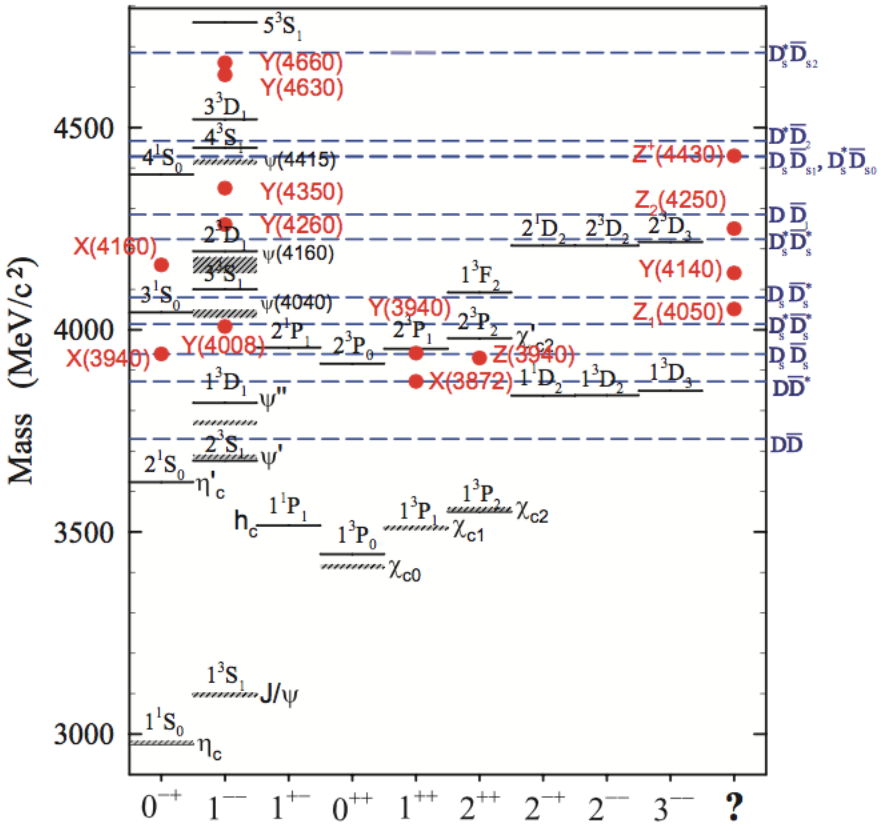


Figure 1.3: States of the charmonium spectrum with quantum number assignments [17].

also E760 and E835. However, $\overline{P}ANDA$ will have a ten times higher luminosity and momentum resolution thanks to HESR and its antiproton beam [2].

Open charm spectroscopy

The open charm mesons are composed of one charm and one light quark, giving a non-zero total charm value. The first open charm was detected in 1976; more correctly, there were two different particles, the D^0 discovered by the group of GOLDHABER, PIERRE, ABRAMS, et al. [19] and the $D^{\pm}$ by PERUZZI, PICCOLO, FELDMAN, et al. [20]. In the following years many others states have been found, leading to the present spectrum illustrated in Figure 1.4. In the spectrum, the black and red dots represent experimental measurements while the green dotted lines and the black lines come from two different theoretical predictions and the blue lines are the thresholds for decays.
In order to evaluate the two different theoretical interpretations of the spectrum, further experiments are needed and $\overline{P}ANDA$ could perform relevant studies in this context. One example is the D^*_{s0} (2317) that has a mass just below the DK threshold and few MeV as the upper limit on

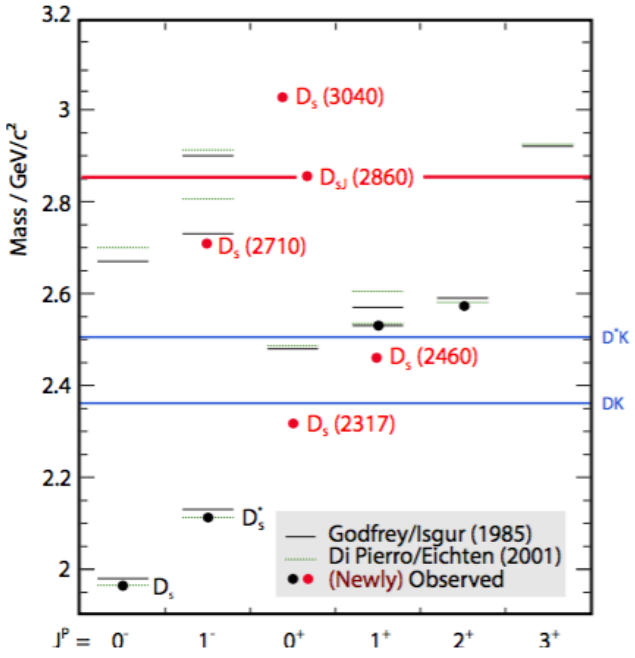


Figure 1.4: Spectrum of open charm meson D_s [17].

its width. $\overline{P}ANDA$, according to the simulations, will have a resolution for the width of these states in the order of 100 keV [21].

Baryon spectroscopy

Another important feature, in order to have a better comprehension of nonperturbative QCD, is the study of the baryon spectrum [22]. At the moment, this spectrum is not well understood. Indeed, according to the "Review of Particle Physics" [23] for several baryons, important properties like mass width and decay channels are only roughly measured. The agreement between some experimental data and the quark model predictions is also quite poor, since the expected masses are different from the measured ones and some resonances, predicted by the theoretical model, have not been observed yet [24].
$\overline{P}ANDA$ will add important data for the clarification of this spectrum, due to its 4π acceptance for particle identification and tracking detectors. This implies that it will be possible to measure the decay of $\overline{p}p$ into $\overline{\Omega}\Omega$,$\overline{\Lambda_c}\Lambda_c$ or $\overline{\Sigma_c}\Sigma_c$ [25]. While at a beam momentum around 3 GeV/c the baryon production probability is similar than the meson one, with the increased momentum (up to 12 GeV/c) the baryon production cross section becomes more and more relevant, with a ratio between baryons and mesons of about two. Indeed, when it will be possible to use the high luminosity mode in HESR, for the Ωs, a production of 700 Ω baryons having a threefold strangeness per hour it is expected [2].

Gluonic excitation

According to QCD, gluons, as mediator bosons of the strong interaction between quarks, can create bound states. Even if they have not been identified yet, theory predicts two different states: hybrids in which a valence gluon is part of a $\bar{q}q$ pair (Figure 1.5 a), and glueballs (Figure 1.5 b), that are states composed only of gluons.

a) b)

Figure 1.5: Model for the gluonic excitation.

HYBRID STATES

In the hybrid system, due to the presence of the gluon that adds another quantum number ($J^P = 1^{\pm}$) and another degree of freedom, it is possible to reach energy levels otherwise forbidden to structures that contain only quarks. According to theory, eight states are predicted combining the S-wave mesons with a gluon excitation, three of them having exotic quantum numbers that can not be interpreted as standard $\bar{q}q$ pairs. Until now the clearest experimental evidence of possible hybrid state comes from the LEAR facility, where $\overline{p}p$ annihilation were studied. In particular two particles with $J^{PC} = 1^{-+}$ were measured: the π_1 (1400) and the π_1 (1600) [26]. In the charmonium sector, hybrids are expected to be in the mass region between 3 and 5 GeV/c^2. In the $\overline{P}ANDA$ experiment, the strategy to find exotic hybrids is to use the highest beam momentum that is possible to reach with the HESR [2].

GLUEBALLS

Fifteen different states are predicted by LQCD calculations in the momentum range provided by the HESR [27] and in $\overline{P}ANDA$ it would be possible to measure these states. Glueballs with exotic quantum numbers are called oddballs. The lightest oddball predicted by LQCD has a mass of 4.2 GeV/c^2 and $J^{PC} = 2^{+-}$ [28]. In Figure 1.6 the simulated glueball spectrum is reported: the respective quantum number configuration J^{PC} is the number next to each state. The pink ones are the oddballs states, while the different colours represent their total angular momentum J. The mass is given in two different ways, for the right axis the scale is directly in GeV/c^2 while the scale on the left gives the mass in units of the hadronic scale parameter

r_0 as multiples of r_0^{-1} = 410 MeV [27]. $\overline{P}ANDA$ will have an important role in collecting more statistics compared to the existing measurements concerning regular and light glueballs [29].

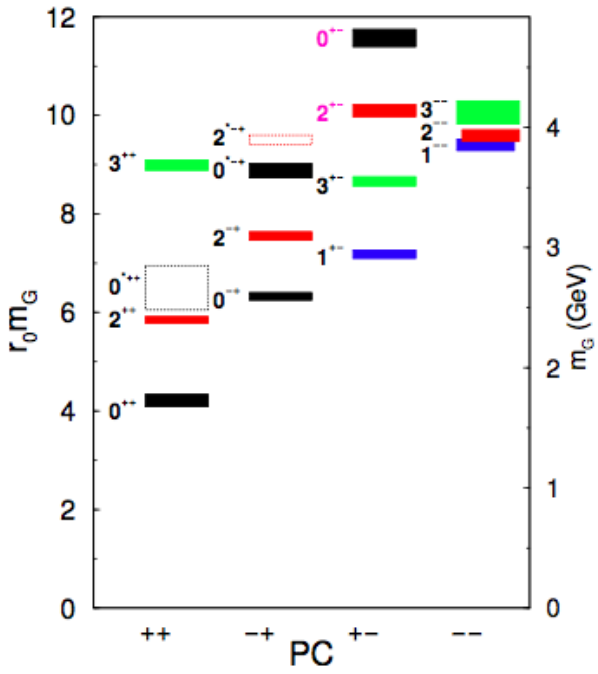


Figure 1.6: Spectrum predicted by LQCD for glueballs [30].

1.2.2 Properties of hadrons in matter

The properties of hadrons change when they are embedded into nuclear matter due to the surrounding interactions. The studies are mainly focused on the modification of the mass level spectrum, as shown in Figure 1.7. Mass values of the hadrons can be modified by the medium in which they have been created. This effect can be attributed to differences in the chiral symmetry breaking due to the finite density value [31].
The in-medium mass shift and splitting have been already studied by several experiments but none of them investigates them using $\overline{p}p$ annihilations. In $\overline{P}ANDA$ it will be possible to study low momentum hadrons in a nuclear environment and, since the effects are more pronounced in this energy region, give a comprehensive understanding of this effect. Moreover, with the beam momentum range provided for $\overline{P}ANDA$ it will be possible to implant charmed mesons in the nuclear matter with high statistics. It is expected theoretically that the mass shift for the J/ψ is between 5 MeV/c^2 and 10 MeV/c^2 while for other states it is much bigger; as in the case of D mesons where the predicted mass shift range is from 50 MeV/c^2 to 100 MeV/c^2 [32].

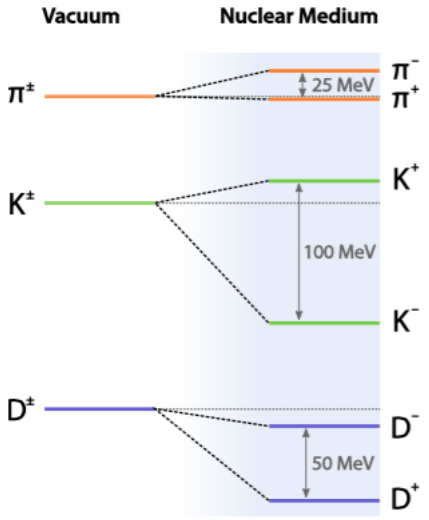


Figure 1.7: Representation of the mass spectrum in vacuum and the nuclear medium [29].

Another interesting field, that is possible to investigate with antiproton-nucleus collisions in the $\overline{P}ANDA$ environment, is the $J/\psi N$ dissociation cross section, which needs further studies. The dissociation cross section of J/ψ and other charmonium states is important for the study of Quark-Gluon Plasma (QGP) in ultrarelativistic nucleon-nucleon collisions [33].

1.2.3 Nucleon structure

The nucleons as constituents of matter are an important topic to investigate. In the energy regime of $\overline{P}ANDA$ it is possible to perform several measurements to study the nucleon structure. One of these studies concerns the Generalized Parton Distributions (GDP) [29, 34] which is usually studied in lepton scattering. Due to the interactions like $\overline{p}p \longrightarrow \gamma\gamma/\pi^0\gamma$ and using the handbag technique, in $\overline{P}ANDA$ it will be possible to study even the distribution of partons. Another one is the study of the transverse distribution of the partons within the nucleon. This can be done with Drell-Yan reactions like $\overline{p}p \longrightarrow l^+l^- + X$, where l^+ and l^- represent a lepton pair. In particular, with $\overline{P}ANDA$ separate studies of the form factors of the proton, magnetic $|G_M|$ and electric $|G_E|$, is feasible in a momentum range up to $q^2 \backsimeq 28\,(GeV/c)^2$ due to the reconstruction of $\overline{p}p \longrightarrow e^+e^-/\mu^+\mu^-$ [35, 36]. At present only the Fermilab experiments E760 and E835 [37] have provided some data in the region $q^2 \backsimeq 15\,(GeV/c)^2$ but with low statistics, therefore, it is impossible to determine the two coefficients independently in this momentum range [38, 39].

1.2.4 Hypernuclei

The last topic of the $\overline{P}ANDA$ physics program is the study of hypernuclei. Hypernuclei are nuclei where one or two nucleons are replaced with hyperons featuring s quarks. This change implies that the hyperons, bound in the nucleus, have one more degree of freedom. Consequently, the nuclei have the possibility to assume different states that were unaccessible due to previous constraints. The hypernuclei are an interesting tool to study the nuclear structure and energy levels. As represented in Figure 1.8, several hypernuclei have already been found experimentally. In the ground plane (S = 0) nuclei without hyperons are located, the S = 1 plane contains the hypernuclei with Λ or Σ as hyperons while in the plane S = 3 there are nucleons with $\Lambda\Lambda$ or Ξ hyperons.

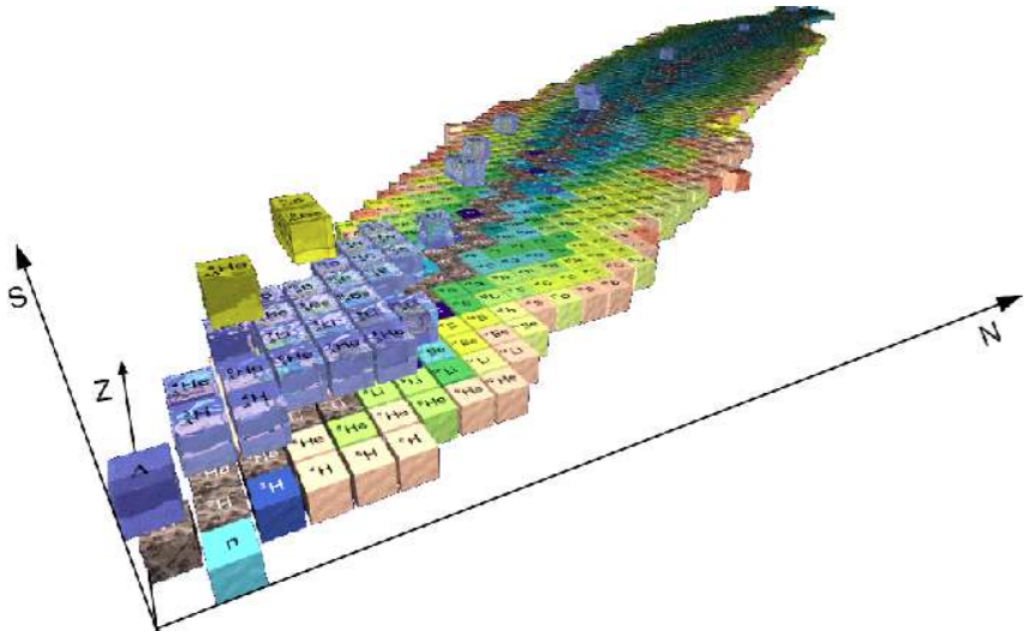


Figure 1.8: Representation of hypernuclei in 3 dimensions, N the number of neutrons, Z of protons and S of strangeness

$\overline{P}ANDA$ will study $\Lambda\Lambda$ hypernuclei, which are produced in the reaction $\overline{p}p \longrightarrow \Xi^-\overline{\Xi}^+$ or $\overline{p}n \longrightarrow \Xi^-\overline{\Xi}^0$ [40, 41], using a dedicated experimental setup which modifies the inner part of the $\overline{P}ANDA$ apparatus. The Ξ^- will be stopped of a secondary target made by sections of silicon detector layers and target foils, where the hypernuclei will be actually formed. Once formed, γ-rays, emitted after the de-excitation of the hypernuclei will be detected by germanium detectors. Approximately 80 γ-rays per month are expected [2] since the cross section for $\overline{p}p \longrightarrow \Xi^-\overline{\Xi}^+$ is about $2\mu b$ and the $\Xi^- p \longrightarrow \Lambda\Lambda$ conversion has a probability of around 5% [25].

1.3 Acceleration structures for protons and antiprotons

FAIR will be a complex structure with several accelerators, storage and cooler rings in order to fulfil all the requirements from the several experiments at the same time. As seen in Figure 1.9, the consequences of this are several beam lines and different paths depending on the beam itself. The orange line is the path that will be used to obtain antiprotons in the High-Energy Storage Ring (HESR) where $\overline{P}ANDA$ is situated.

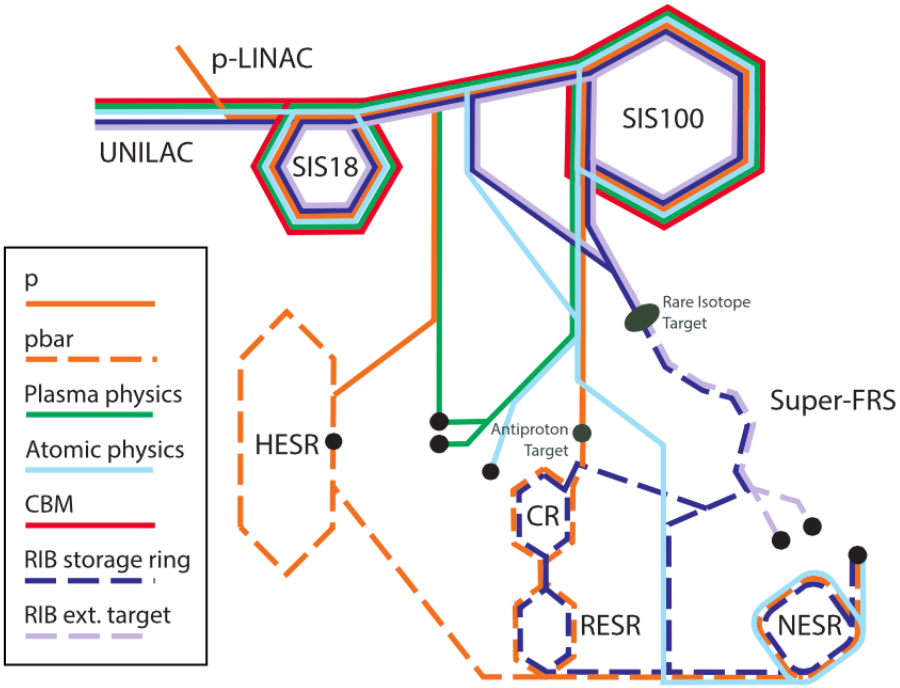


Figure 1.9: Several paths for the beam in the FAIR accelerators and storage rings [42].

The protons will be accelerated up to 70 MeV, by a p-LINAC, with the beam parameters matched to the SIS18. This ring is already used at GSI as a heavy-ion synchrotron but, after the upgrade, it will be possible to store and accelerate also protons to a kinetic energy of 2 GeV in one cycle [42, 43]. The energy reached at this point is enough to be accepted by the SIS100, that has a circumference of about 1,1 km and a magnetic rigidity of 100 Tm. Its goal is to achieve an intensity of $4 \cdot 10^{13}$ protons per pulse at 29 GeV with a cycle length of 2 seconds. As can be seen in Figure 1.9, after the SIS100, the protons are sent to the antiproton target to generate the corresponding beam. To obtain its maximum intensity the target is the crucial component. Since the antiproton yield grows with the target thickness until the absorption of the produced antiparticles dominates the process. To find the optimum target length two different parameters must be taken into account: the density of the material and its heat capacity. Materials with higher

densities are interesting because they allow having thinner targets, increasing the efficiency of the production. The drawback of these materials is that they have a relatively low heat capacity and this means that the target could melt due to the heat produced by the collisions. After several studies, simulations showed that a 11 cm thick target made of copper or nickel it the best compromise. This means that, with the proton beam coming from the SIS100 at 29 GeV, it is possible to have a production of 10^{-5} antiprotons per primary proton. The resulting antiproton beam of 10^8 antiprotons is injected into the Collector Ring (CR). This ring is smaller than the previous one, with a circumference of about 211 m and a beam rigidity of 13 Tm. For the whole facility, the CR has three different tasks but only one is related to the antiprotons. Its goals are stochastic pre-cooling of the antiparticles at a fixed kinetic energy of 3 GeV and to bunch the antiprotons in 25 ns bunches.

1.3.1 The High Energy Storage Ring (HESR)

The HESR is the final ring for the antiproton beam. According to Figure 1.10, the antiprotons are injected from the CR. As written in the previous section, the antiprotons' input energy is 3 GeV. In the HESR, they are accelerated or decelerated to the required energy. The achievable range is from 0.83 GeV to 14.1 GeV, corresponding to a beam momentum of 1.5 GeV/c to 15 GeV/c [44]. With this energy, it is possible to explore the research areas of hadron structure and quark-gluon dynamics. The circumference of the HESR is 574 m, with 132 m of straight sections, and the magnetic rigidity is 50 Tm.
The $\overline{P}ANDA$ experiment will be located in one of the straight sections, while the second one is occupied by the electron cooler. As shown in Figure 1.10, there is also a stochastic cooling present. In particular, the pickup is located close to the end of the experiment straight section while the kicker is at the beginning of the opposite straight section. A stochastic cooling is needed to adjust energy spread and to control the emittance. Since the beam velocity is relativistic, the information necessary to modify the magnetic field by the kicker can not travel faster than the beam. Considering also that the modifications are not instantaneous, it is clear that the path of the data coming from the pickup to the kickers must be significantly shorter than the beam path. This is the reason why pickup and kicker are placed on opposite sides. Using both cooler system it is possible to reach a minimal momentum spread of $\delta p/p = 10^{-5}$, but due to the electron cooler the momentum range is limited to 8.9 GeV/c and the luminosity is limited to $2 \cdot 10^{31}$ cm^{-2} s^{-1}. This operating mode is called ***High-precision mode (HP)***. It is also possible to use just the stochastic cooling leaving out the limitations coming from the electron cooler. In this way it is possible to reach a higher luminosity of $2 \cdot 10^{32}$ cm^{-2} s^{-1}, and the full momentum range can be covered. The disadvantage is reflected in a larger momentum spread $\delta p/p = 10^{-4}$. This mode is called ***High-luminosity mode (HL)***.

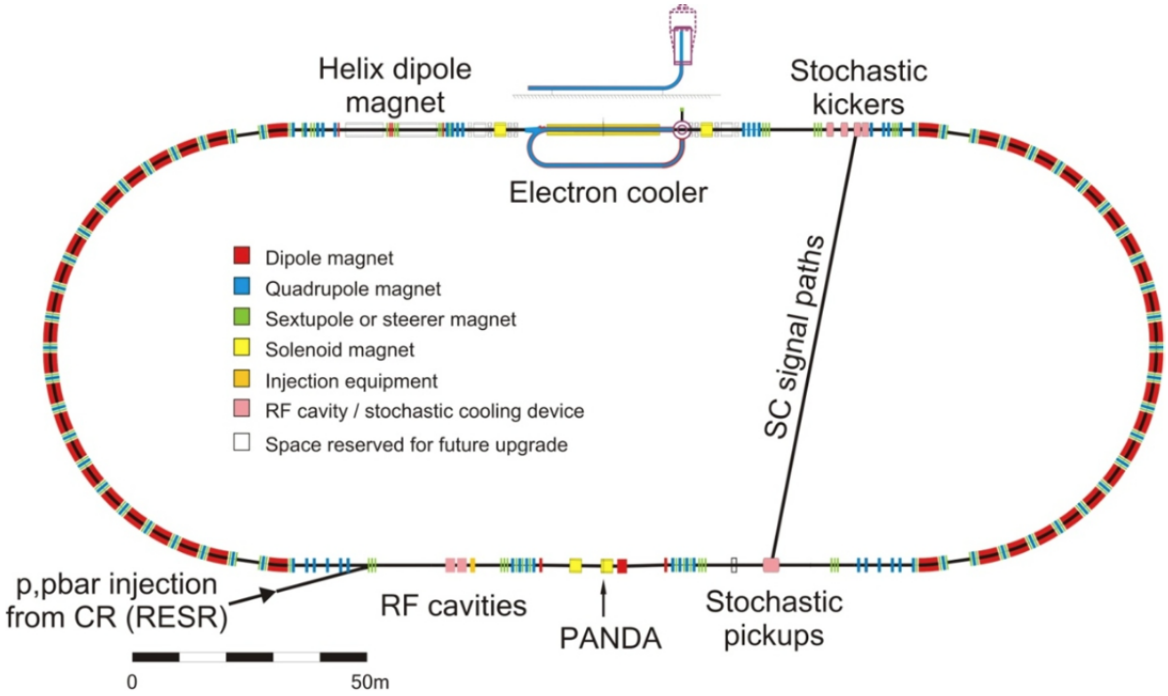


Figure 1.10: Scheme of the HESR used to accelerate and store antiprotons [45].

1.3.2 Target system

The $\overline{P}ANDA$ physics program, described in Section 1.2, is mainly focused on proton-antiproton interactions. This implies, since the beam is composed of antiprotons, that a pure proton target is needed. It is also planned to study in-medium modifications, thus the target system must be able to provide several materials. For the antiproton-proton interactions, the material chosen is hydrogen, for the antiproton-neutron interactions, the target system is made of noble gases from He to Kr and other gases like N_2. The most difficult challenge is to introduce the material into the beam pipe without destroying the ultra high vacuum or modifying the beam quality[46]. There are two concurrent projects that fulfil the requirements, a cluster jet or a pellet system. Both will provide a flow of particles with a size in the region of micrometers or nanometers that will cross the beam pipe in the transverse direction.

Cluster target

This target system, shown in Figure 1.11, is based on a pre-cooled gas that is expanded into a vacuum through a convergent-divergent Laval-type nozzle with an opening that can vary from $10\mu m$ to $100\mu m$ [46]. In the nozzle, the gas is adiabatically cooled and a supersonic stream is

produced. The resulting gas can travel for several meters in the vacuum without divergence. The cluster features are strongly dependent on the general system design, for example, the size of the cluster and the beam intensity depend on the design of the nozzle (a typical value is 10^3-10^5 atoms per cluster) while the final volume density is related to the pressure that the gas has before.

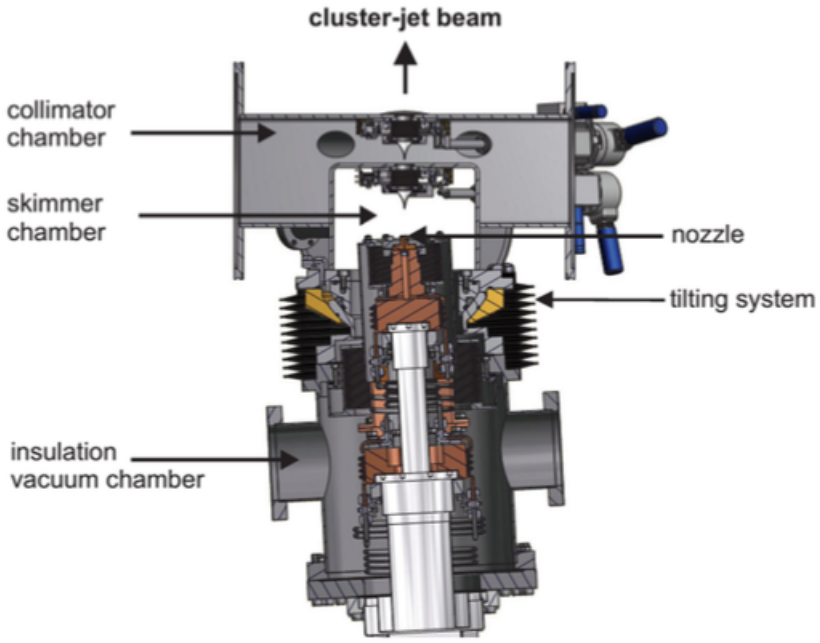


Figure 1.11: Design for the jet cluster target system developed for $\bar{P}ANDA$ [46].

Once created, the cluster beam passes the skimmer and the collimator chambers to modify its shape. After this, it enters the vacuum pipe leading to the interaction point. In the case of hydrogen fluid, operating conditions are a temperature of 25K-35K and a pressure of up to 25bar.

Pellet target

The pellet target system will be implemented in $\overline{P}ANDA$ at a later stage. Some of the main advantages are the possibility of an exact target tracking within the beam pipe and the high effective target thickness. However, since the target has a high thickness it is more affected by variations.
As shown in Figure 1.12, to create the pellet first of all a triple point chamber is needed. Here, through a small nozzle, a desired material is injected as a liquid at cryogenic temperatures. The chamber contains the same material injected with the nozzle or in some cases helium in gaseous

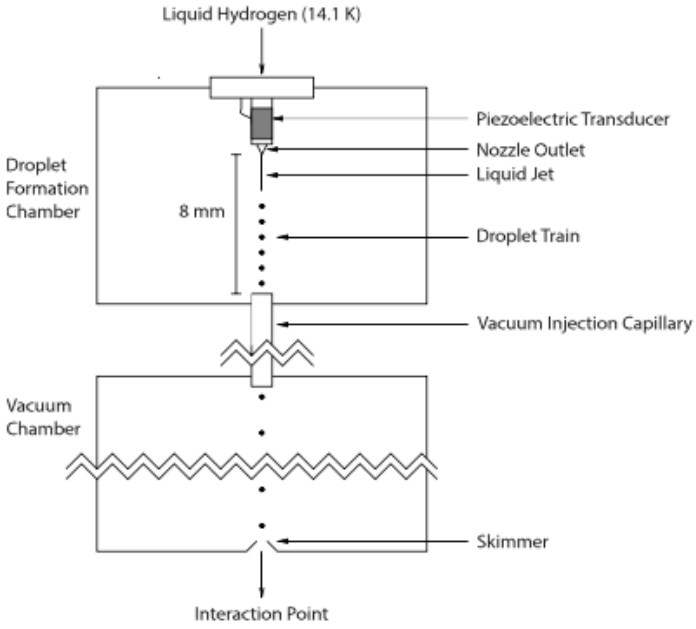


Figure 1.12: Schematic for the pellet target system developed for $\overline{P}ANDA$ [46].

form. The nozzle is periodically stimulated by a piezoelectric trasconducer inducing the jet to oscillate. If the amplitude of the oscillation is equal to the jet radius, the drops are created and thus it is possible to create a continuous and homogenous flow. The latter is injected into the vacuum pipe through a capillary and can be tracked by an optical detector. At this point it is ready to be sent to the interaction point [46].

1.4 $\overline{P}ANDA$ detectors

Considering the physics program described in Section 1.2 it is clear that a completely custom design for the detector is needed. Since the $\overline{P}ANDA$ apparatus is an experiment with a fixed target, reaction products will have a boost in forward direction. The detector can be mainly divided into two parts, the Target Spectrometer (TS), that surrounds the interaction point, and the Forward Spectrometer (FS), that extends behind the interaction point, as shown in Figure 1.13. Another important thing to keep in mind during the design of the detectors is the necessity to have, for a high energy and spatial resolution, a 4π coverage of the solid angle and a high radiation tolerance against photons, neutrons, kaons and many other particles [46, 29].

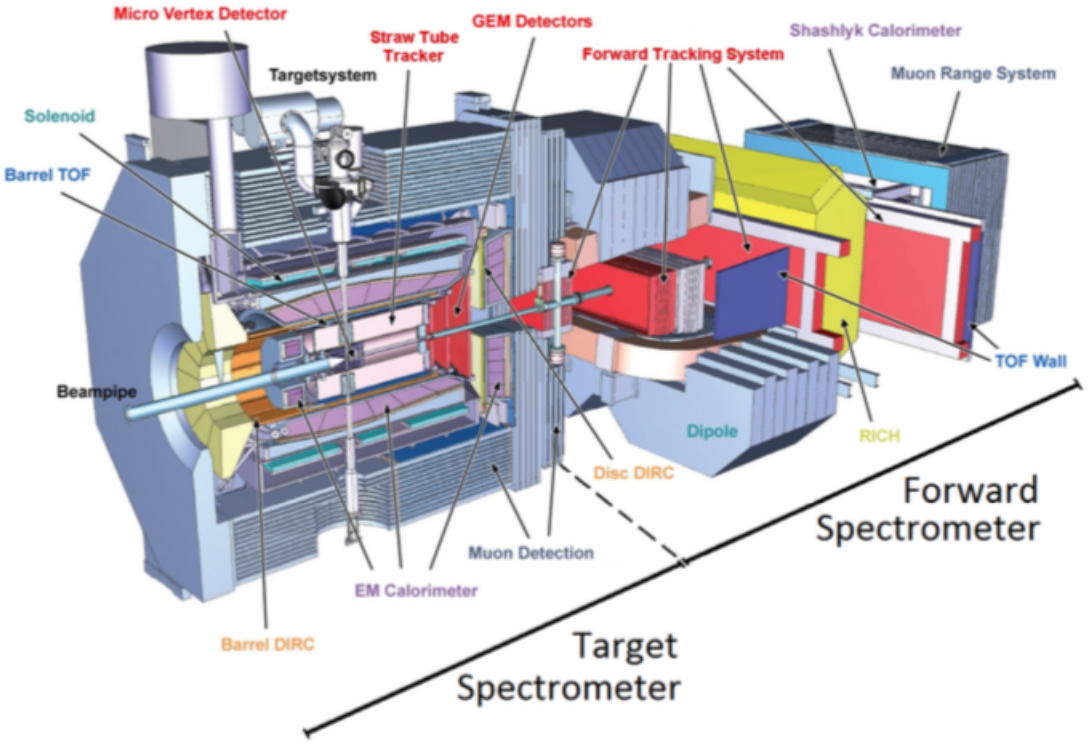


Figure 1.13: Overview of the whole $\overline{P}ANDA$ experiment.

1.4.1 Target Spectrometer

The TS, as already mentioned, is placed around the interaction point and consists of several detectors as shown in Figure 1.14. It covers polar angles from 5° (in the horizontal plane) and 10° (in the vertical plane) to 170°. As can be seen in Figure 1.14, the target pipe crosses every layer, from the external magnet to the innermost detector (the Micro Vertex Detector (MVD)). This fact poses one of the most influent constraints for the mechanical design.
It is possible to group the structure of the TS in different parts:

- Tracking system
- Particle Identification detectors
- Electromagnetic Calorimeter
- Solenoid Magnet
- Muon Detector

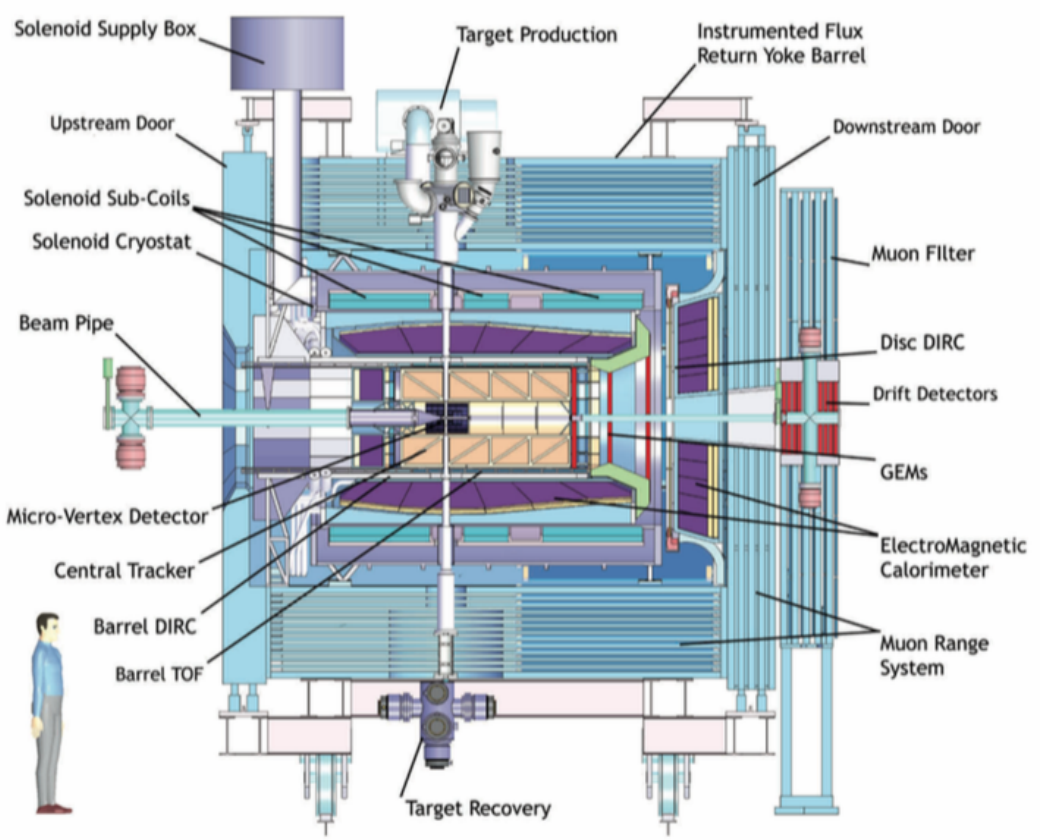


Figure 1.14: Layout of the Target Spectrometer.

1.4.1.1 Tracking system

The tracking system is the innermost one and it is made of three different detectors: the Micro Vertex Detector (MVD), the Straw Tube Tracker (STT) and the Gas Electron Multiplier (GEM). In particular, the MVD surrounds the interaction region which in turn is surrounded by the STT. In the forward direction three GEM disks are placed. An overview of the tracking system is shown in Figure 1.17.

The Micro Vertex Detector

As already mentioned, the MVD is the innermost detector of $\overline{P}ANDA$. Its structure, shown in Figure 1.15, is designed to optimise tracking information as close as possible to the interaction region [45].
The main goals of this detector are the primary and secondary vertex reconstruction. This implies that a high spatial resolution, a good radiation hardness and the capability to handle high rates are important features. The material budget must not exceed 10% of one radiation length

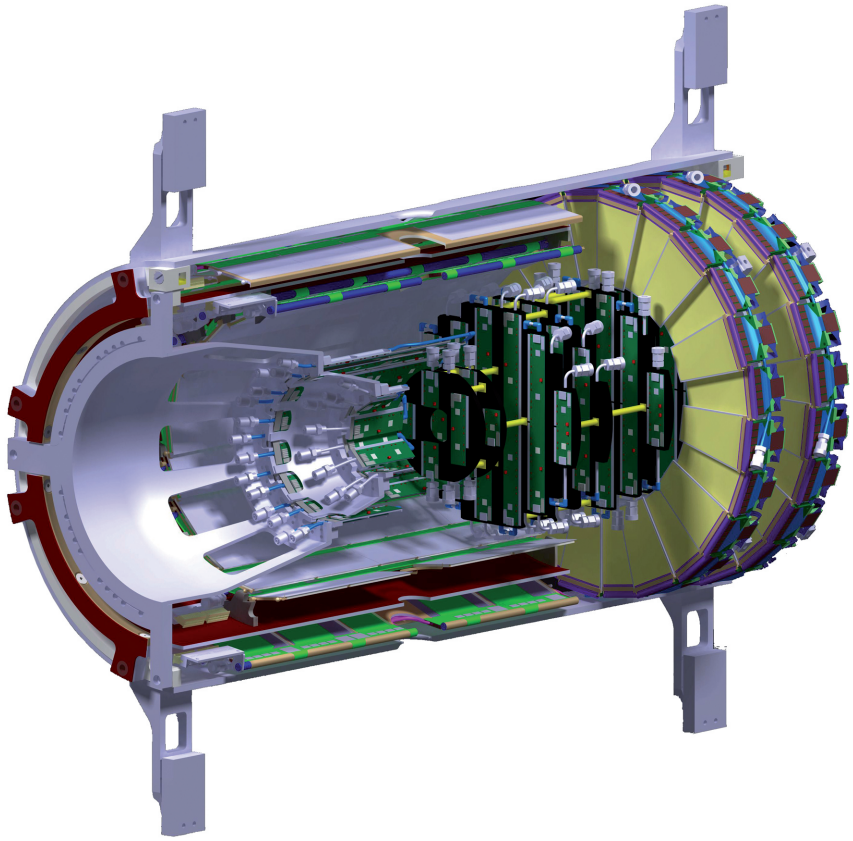


Figure 1.15: Layout of the MVD [47].

for the entire acceptance of the detector. Since this thesis is concerned with the development of part of this detector, it will be described in detail in Section 1.5.

The Straw Tube Tracker

The STT consists of long narrow tubes called straws and it is considered the central tracker of the experiment [48]. The detector in Figure 1.16 has a cylindrical shape, is composed of 4636 straws arranged in 27 layers. Each straw is filled with a gas mixture of Ar and $CO_2$with a ratio 90:10 and an overpressure of 1 bar, contained within Mylar aluminised foil with a thickness of 27 μm. Its diameter is 10 mm while the length is 150 cm. A voltage difference of few kV is generated by the wall of the straws, acting has a cathode, and a single 20 μm gold plated tungsten wire along the axis of the straw as an anode. This voltage difference produces a drift of both ions and electrons with a maximum drift time of 200ns.
To increase the detector resolution, the 27 layers divided into three different groups. The first one consists of 19 layers that are parallel to the z-axis, this results in a spatial resolution of 150 μm in the x-y plane. The second group includes 4 layers that have an orientation of +2.9° with

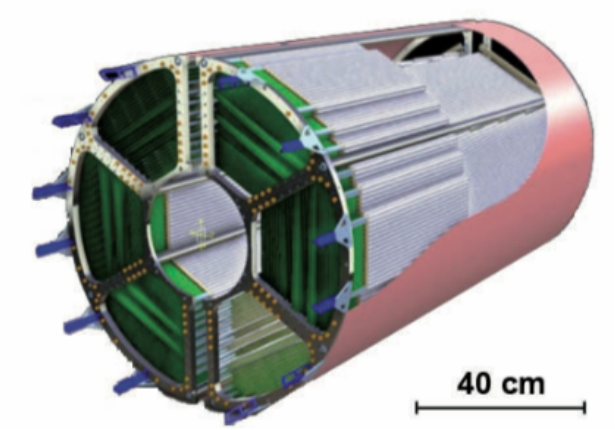


Figure 1.16: Layout of the STT.

respect to the previous group, while the third one has 4 layers with an orientation of -2.9°. The idea is to alternate 2 layers of the second group with 2 layers of the third group in the middle of the 19 layers. With this structure, it is possible to achieve a resolution of 3 mm in the z direction. The complete design is expected to have a 2.5m longer detector that covers a polar angle between 10° to 140° with a low material budget in the order of 1.2% of one radiation length.

The GEM

Particles with small angles are not detected by the STT or they hit this detector in only few points, making the track reconstruction difficult. For this reason, three GEMs will be installed after the STT (Figure 1.17), placed at 1.1m, 1.4m and 1.9m from the interaction point respectively. The diameter increases with the distance, 45 cm for the first disk, 56 cm for the second and 74 cm for the last one. In the center there is a hole for the beam pipe, the latter has a diameter of 5 cm which defines the lower limit of their angular acceptance. With these geometrical limits, it is possible to cover an angular range of 3° to 22°[29, 49].
The three disks act as amplification stages, each GEM is made of a Kapton foil with a thickness of 50 μm that is micro-perforated. The foils are coated on both sides with copper and applying a high voltage between the two faces it is possible to generate an electric field of around 50 kV/cm. The field lines go into the perforation, increasing the density of the field leading to an avalanche multiplication of the drifting electrons.

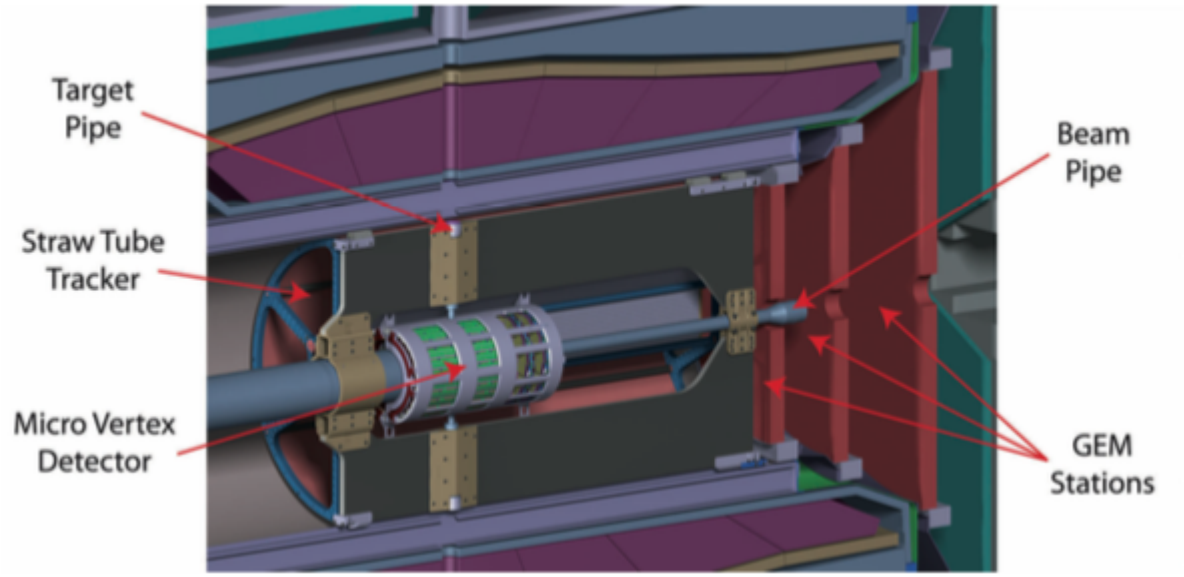


Figure 1.17: Layout of the GEM.

1.4.1.2 Particle identification

The particle identification is performed using two different approaches, one use the Cherenkov effect while the other using Time of Flight (ToF). For the Cherenkov method two different DIRC detectors (Detection of Internally Reflected Cherenkov light) are planned, the barrel DIRC and the disk DIRC. For ToF measurements, a Scintillator Tile (SciTil) detector is used.

The Barrel DIRC

The use the Cherenkov method to identify the particles, it is necessary to measure the light emitted from particles that cross a medium faster than the speed of light in that medium. The light is emitted in a cone with a characterising angle Θ_c that depends on the particle's velocity $\beta = \frac{v}{c}$. Combining this information with the momentum from the tracking system it is possible to determine the mass of the particle.
The barrel part employs the concept developed for the BaBar DIRC [51]. It will cover the polar angle in a range from 22° to 140° [52]. The structure is shown in Figure 1.18 and consists of 80 fused artificial quartz slabs that surround the beam line in a distance of 47.6 cm. At the downstream edge mirrors are placed to reflect the light to the opposite side. At this point the readout is performed. The slabs are coupled to an expansion volume, the light is thus focused on Micro-channel plate photomultiplier tubes (MCP-PMTs), placed in the backside of the volume to convert the light into an electrical signal. The time is measured with a precision

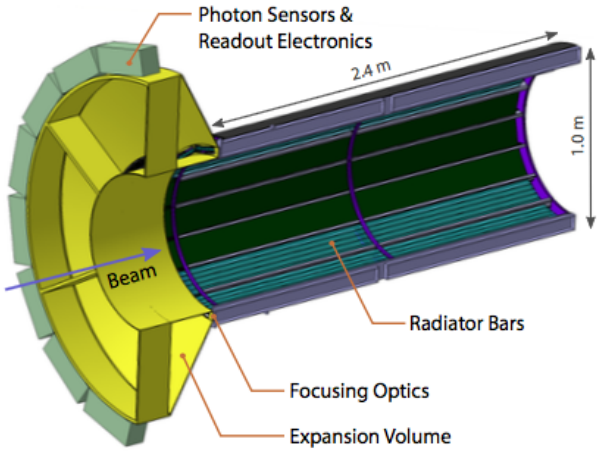


Figure 1.18: Layout of the Barrel DIRC detector [50].

of 100 ps while the angular resolution is around 9 mrad. This structure will be able to provide $\pi - K$ separation for particle momenta up to 3.5 GeV/c from about 1 GeV/c.

The Disk DIRC

It is necessary to add the structure shown in Figure 1.19 to increase the acceptance of the DIRC. With this structure, placed at the end of the barrel, it is possible to cover the angular range from 5° (in the vertical plane) and 10° (in the horizontal plane) to 22°. Moreover, is also increases the $\pi - K$ separation power, in particular, it provides separation up to 4 GeV/c. The disk DIRC has a dodecagon shape with a radius of 110 cm and a thickness of 2 cm. The material is the silica already present in the barrel. The signals are read out with MCP-PMTs or Silicon Photomultipliers (SiPMs) placed on the outer edge of the detector.

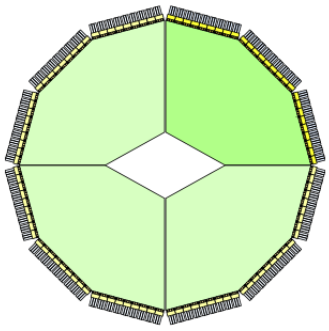


Figure 1.19: Layout of the Disc DIRC detector [50].

The Scintillating Tiles

The SciTil is the ToF detector in the TS, its barrel shape will surround the DIRC detectors. This detector has two different tasks, the first one is to provide a fast response for identification of particles with momenta lower than 1 GeV/c: the output signal has a time resolution of 100 ps [53]. The second task is to provide track seeds for pattern recognition.

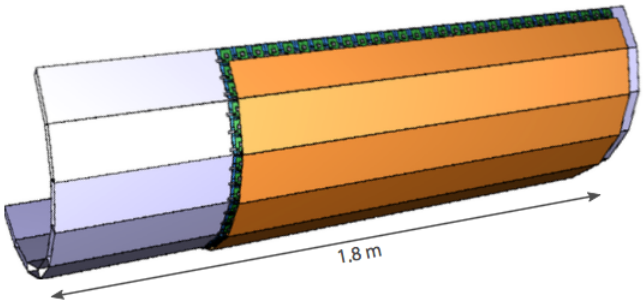


Figure 1.20: Layout of the Scintillating Tiles detector [54].

The layout of the detector is shown in Figure 1.20 and includes 8000 plastic scintillator tiles. Each tile has a side that can vary from 20mm to 30mm while the thickness is fixed to 5mm, together they form a barrel. The tiles are read out by two SiPMs each, reaching the time resolution required.

1.4.1.3 Electromagnetic Calorimeter

The outermost particle detector in the TS is the ElectroMagnetic Calorimeter (EMC), its layout is shown in Figure 1.21. Its task is to determine the energy of the particles that, crossing the material of this detector, create an electromagnetic shower [55, 56]. The EMC is designed to cover 99% of the 4π polar angle. The high count rate and the need for a compact layout leads to different challenges during its design. The maximum energy resolution that is possible to achieve is in the order of 2% while the time resolution is better than 2 ns at 1GeV.
The EMC is divided into three sections, the forward endcap for particles with polar angles between 5° and 22°, the barrel that is shown in blue in Figure 1.21 for tracks over 22° and the backwards endcap, shown in green in Figure 1.21 for particles with polar angles larger than 140°. The chosen scintillation material for the calorimeter is lead tungstate ($PbWO_4$), because it has a short radiation length in the order of 8 mm, a fast response and a good radiation hardness. The crystals are 20 cm long and they will operate at -25° C to increase the light yield by a factor of 4 with respect to room temperature. In total 11360 crystals are present in the barrel section along with 3600 in the forward and 592 in the backward end caps. The readout is performed with large area avalanche photodiodes for the barrel and the backward endcap while for the forward endcap a vacuum photo-triode readout system is used [57].

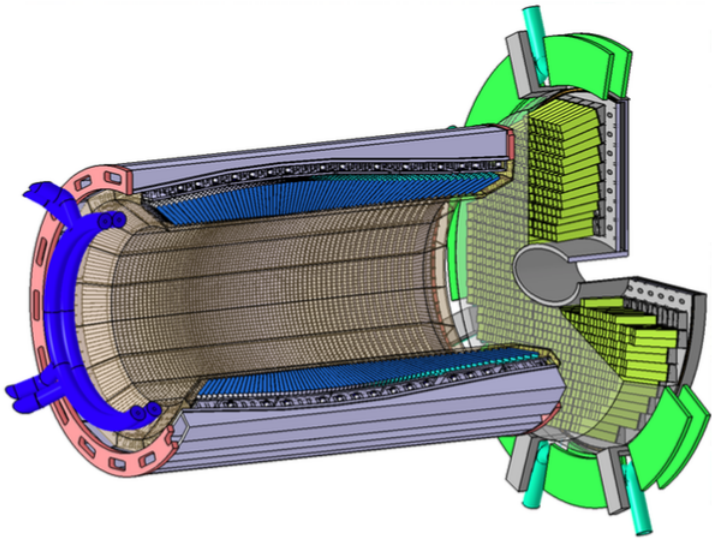


Figure 1.21: Layout of the Electromagnetic Calorimeter [56].

1.4.1.4 Solenoid magnet

The magnetic field in an experiment like $\overline{P}ANDA$ is important for particle identification because, measuring the curvature of the trajectory of charged particles and knowing the magnetic field, it is possible to obtain further information about the primary particles. For this task in a solenoid magnet is installed in the TS, which is shown in Figure 1.22.

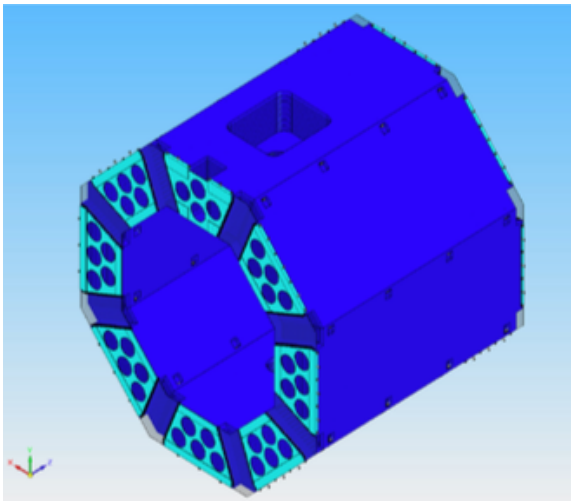


Figure 1.22: Layout of the Solenoid magnet [58].

The solenoid will provide a homogeneous magnetic field of 2 T, with a maximum fluctuation of 2% [58]. The target system has to pass through the magnet, so a gap has to be left open, as can

be seen in Figure 1.22, which leads to a non-homogeneity of the magnetic field. To avoid this problem, the magnet consists of three coils connected in series, where the outer two have 232 turns while the central one has 104 turns. All three have been designed to work with 5kA. An overview of a section of the magnet is shown in Figure 1.23. For the semiconducting part NbTi is used, specifically, Rutherford-type cables are formed [58]. This means that several cables are grouped together and compressed until a rectangular shape is reached. This technique is important to increase the radial alignment. The wires are then folded inside the coil former that in this case is made of aluminium. There are two different way to increase the strength of the magnetic field in the tracking region: the first one is to build a bigger solenoid, the second and more practical one is to cover the entire magnet with a flux-return yoke made of iron. With this technique it is also possible to achieve a better orientation of the field flux lines and reduce the radial components.

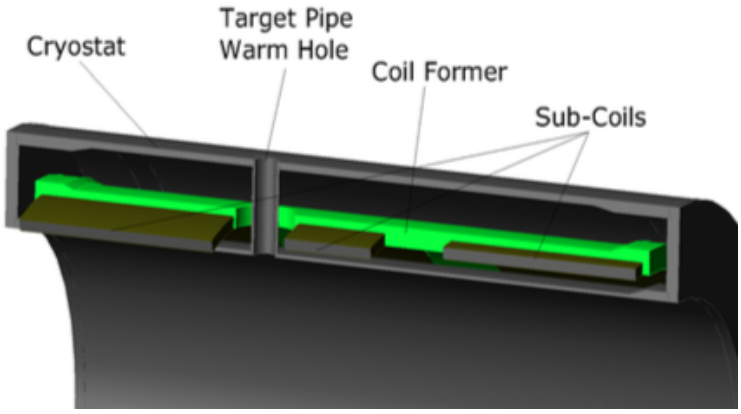


Figure 1.23: Section view of the Solenoid magnet [58].

1.4.1.5 Muon detector

Only few particles reach the region after the calorimeter and the solenoid magnet only a few particles are still alive, most of them are pions or high energetic muons. For the Drell-Yan processes, D-meson decays and the J/Ψ decay, the detection of muons and above all the separation between muons and pions is important.
The structure chosen for the detection of the muons is a Range System, in particular, a series of rectangular aluminium Mini Drift Tubes (MDTs) interleaved in the iron layers of the solenoidal magnet yoke is used [60]. Since the MDTs work as normal drift tubes, it is necessary to add capacitively coupled strips to the rectangular tubes to have the longitudinal position information. With this technique, it is possible to achieve a position accuracy in the order of 1 cm. The muon detector can be split in two parts a barrel and a forward endcap. The first one consists

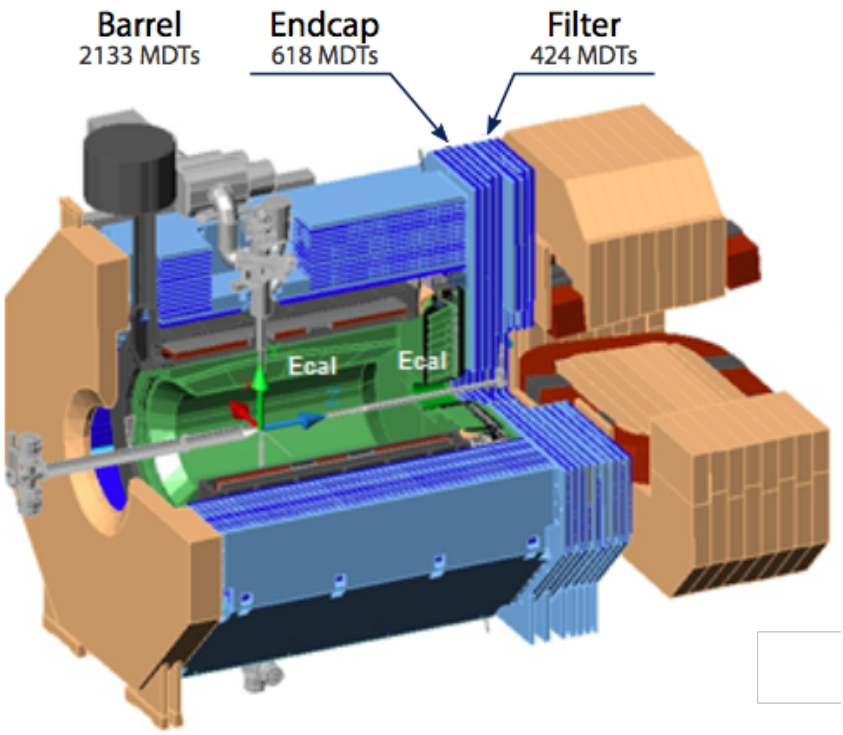


Figure 1.24: Layout of the muon detector with the respective MDTs [59].

of 13 MDT layers interspersed with iron foils. Every iron section has a thickness of 3 cm except for the first and last that have a thickness of 6 cm. The second part is composed of 6 layers of sensitive material, each one is separated from the other by an iron foil for a total of 5 iron layers. In this part, each section is 6 cm thick and it is designed for higher particle momenta. As shown in Figure 1.24 behind the endcap a muon filter made of 5 **MDTs!** layers and 4 iron layers is placed, to increase the detection capability but also to shield the forward magnet to the solenoid.

1.4.2 Forward Spectrometer

The FS covers the angular range below the 5° in the vertical plane and 10° in the horizontal direction. It is placed behind the TS as shown in the left part of Figure 1.25. The structure of the FS is grouped in different parts:

- Tracking system
- Dipole Magnet
- Particle Identification detectors
- Shashlyk Calorimeter
- Muon Detector

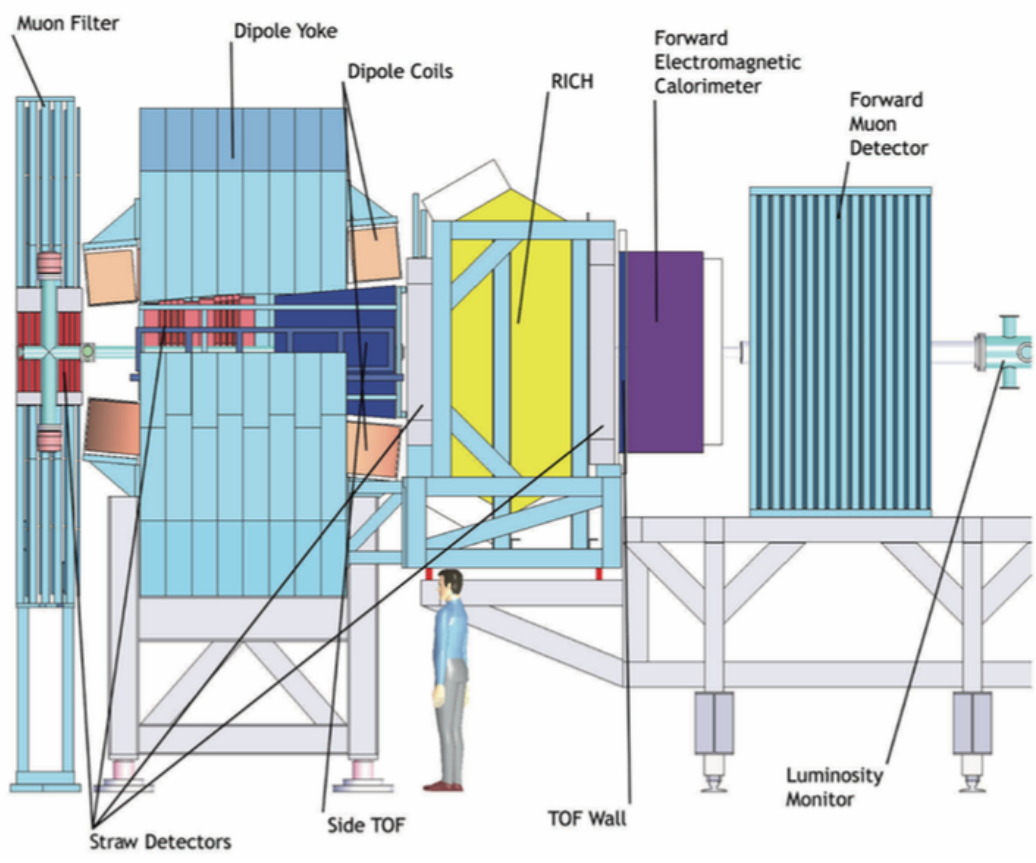


Figure 1.25: Layout of the Forward Spectrometer [58].

1.4.2.1 Tracking

In the FS the tracking system is based only on the STT. As shown in Figure 1.26 there are three regions and each one is composed by two detectors. The STTs are constituted of four double layers of straw tubes, two of them with vertical wires while in the two remaining ones the wires are skewed by $\pm 5°$. This gives the necessary information for the reconstruction in the vertical plane. The first block is placed in the muon filter and has 1024 straws, the second one composed of 4736 straws is placed inside the dipole magnet and the third is the biggest one, featuring 13000 straws, placed after the magnet. These straw tubes are filled with a gas mixture 90:10 Ar-CO_2, while the drift time is in the order of 140ns depending on the magnet's field strength.

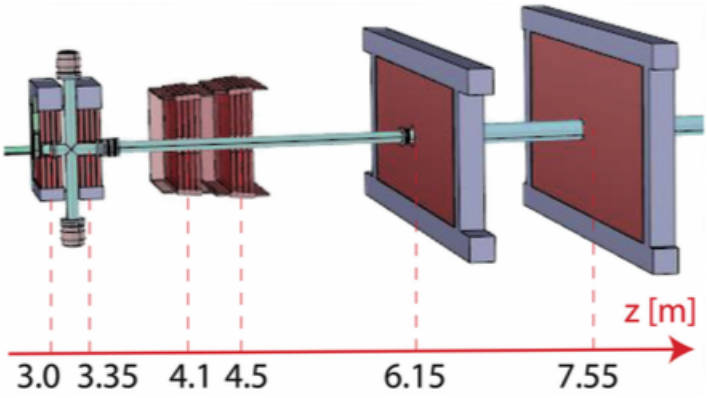


Figure 1.26: Layout of the STT in the FS [58].

1.4.2.2 Dipole magnet

Figure 1.27 shows the magnet structure in the FS. It is a dipole magnet with an opening of 1 m high and of 3 m wide, and a maximum rigidity of 2 Tm [58]. To achieve this rigidity, the structure works with a 2.16 kA current that flows into copper coils. It is placed 3.9 m from the interaction point and it extends for 2.5 m in the beam direction.
The drawback of this structure is the orientation of the magnetic field that is perpendicular to the beam direction. At the full beam momentum, of 15 GeV/c, this implies a deviation of the antiprotons from the nominal direction of 2.2°. For this reason, as shown in Figure 1.10, it is necessary to add additional dipole magnets before and after the $\overline{P}ANDA$ detector in order to adjust this deflection.

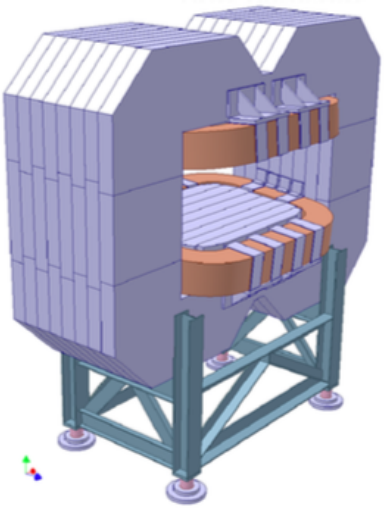


Figure 1.27: Layout of the dipole magnet [58].

1.4.2.3 Particle identification

In the FS two detectors are used for particle identification as shown in Figure 1.28, the ToF and the Ring Imaging Cherenkov (RICH). The first one will be placed 7 m away from the interaction point, it is composed of three walls of plastic scintillator slabs, each plate 140 cm long and 2.5 cm thick. The readout is placed on top and at the bottom of the slabs, the signal is fed to a photomultiplier tube by a light guide. With this set up, it is possible to achieve a time resolution in the order of 50 ps and ensure a good π/K separation up to 2.8 GeV/c and a good K/p separation up to 4.7 GeV/c [61].

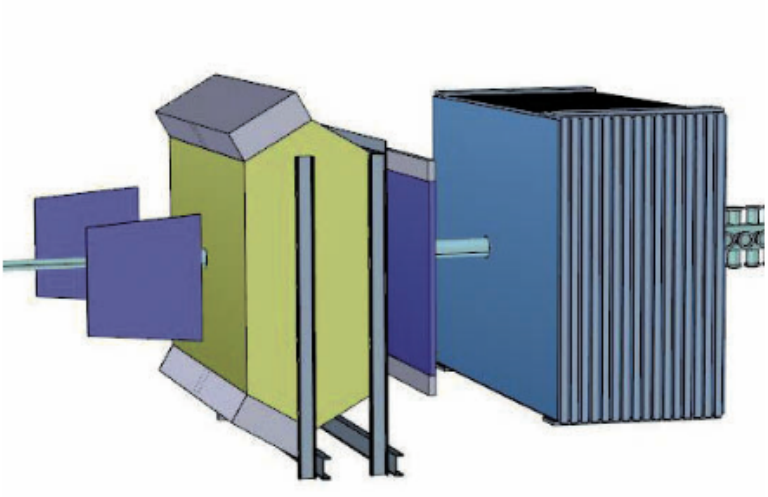


Figure 1.28: Layout for the particle identification detectors.

The structure of the RICH is based on the one used at HERMES [62], a dual radiator made of silica aerogel with refraction index of n = 1.0304 and filled with C_4F_{10} featuring a refraction index of n = 1.00137. This detector allows a good particle identification in the momentum range between 2 and 15 GeV/c, in particular a good π/K and K/p separation. The Cherenkov light is focused on an array of phototubes, placed outside of the detector, with a mirror.

1.4.2.4 Shashlyk Calorimeter

The calorimeter designed for the FS is based on the Shashlyk principle. This technique has been chosen for its high performance at a relatively low cost [55, 63] and the resulting layout is shown in Figure 1.29. The light produced is extracted via wavelength shifting fibers placed in the scintillators. The detector will be placed 7.5 m from the interaction point and is realised with 0.275 mm thick plastic scintillators alternated with lead absorber layers with a thickness of 1.5 mm. To achieve a higher spatial resolution, each module is subdivided into four submodules and connected individually to one photomultiplier. The complete structure is made of 351 modules divided into 13 rows and 7 columns. With this structure, an energy resolution of $4\%/\sqrt{E}$can be achieved.

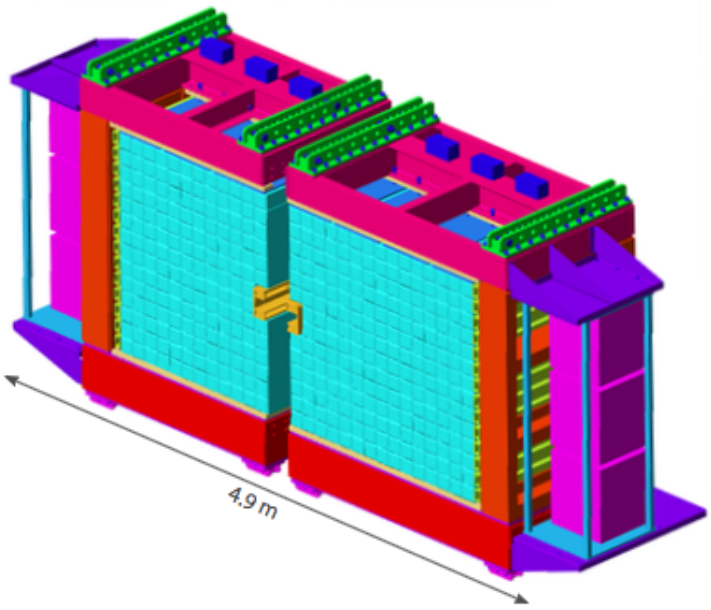


Figure 1.29: Layout of the forward calorimeter [63].

1.4.2.5 Muon detector

The muon detector, shown in Figure 1.30, is placed 9 m from the interaction point. The design is the same as for the muon detector of the TS. However, in this case, it has to manage particles with energies of up to 10 GeV. The MDT aluminium layers are alternated, as in the previous muon detector, with 6 cm thick iron foils. In addition to being able to discriminate between pions and muons, it is possible to use the system as a hadronic calorimeter with moderate energy resolution [64].

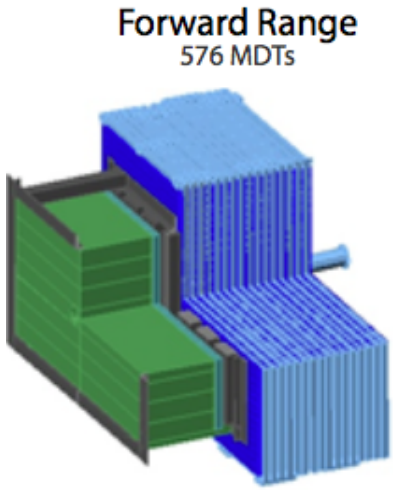


Figure 1.30: Layout of the muon detector for the forward spectrometer [63].

1.4.3 Luminosity detector

The general task of the luminosity detector is the determination of the cross section σ of physical processes. The way to obtain this is to extract, in a time interval dt, the time integrated luminosity L and following the relation $N = L \cdot \sigma$ it is possible to have a correlation between the measured number of events N in a time interval dt and the cross section σ [65]. For $\overline{P}ANDA$, this detector will reconstruct the angle of elastically scattered antiprotons in the Coulomb-nuclear interference region. This angle is particularly small, from 3 mrad to 25 mrad with respect to the beam axis [66]. For this reason, the detector is placed 11 m from the interaction point.
In Figure 1.31 the layout of the detector is shown. It has four tracking planes and each of them is equipped with 10 High-Voltage Monolithic Active-Pixel Sensors (HV-MAPS) modules [68]. In this particular design, 60000 pixels are present in one HV-MAPS with a channel pitch of 80 μm. To minimise the scattering of the antiprotons, the detector is surrounded by a box that keeps

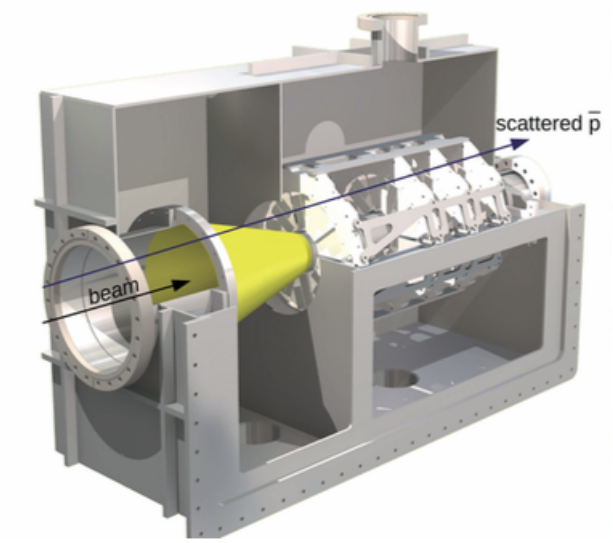


Figure 1.31: Layout of the luminosity detector [67].

the vacuum around the detector. To maximise its acceptance, the beam is fed to it through a cone in order to decrease the beam pipe diameter.

1.5 Micro Vertex Detector

Since the topic of this thesis is the design of the readout electronic system for the strip sensors of the MVD, this detector is therefore described in more detail on the next pages. As mentioned in Section 1.4.1.1, its main tasks are the reconstruction of decay vertices and the momentum of charged particles. In order to increase the precision as much as possible, the detector is designed to have the hit points as close as possible to the interaction region [45]. Additionally, it must be able to distinguish the primary interaction vertex from the secondary vertices. The distance between the main vertex to the others can vary a lot, in particular, in $\overline{P}ANDA$, the decay lengths are roughly from hundreds of microns, i.e. $c\tau(D^0) = 123\,\mu m$, to few centimetres, i.e. $c\tau(\Lambda) = 7.9\,cm$ [23].

1.5.1 Detector requirements

The design of the detector is mandated by the physics requirements, as well as certain engineering constraints. The volume available for the MVD is limited by the beam pipe and the outer detectors. For the innermost layer, the minimum distance from the center of the beam pipe is 1 cm [69] that is the outer radius of the pipe while, for the outer layer, the maximum

possible distance is 15 cm from the center of the beam pipe in order to not compromise the design of the surrounding detectors. Being the innermost detector leads to another restriction, the material budget. It is important to limit it in order to minimise multiple scattering and consequently reduce the impact on the outer detectors. For the MVD the material budget is limited to 10 % of one radiation length over the full detector acceptance. To maximise the detector acceptance it is necessary that the solid angle is covered fully, but, since there are other detectors surrounding the MVD, the beam pipe positioned in its center and other structures, the polar angle range is limited to 3° to 150°. Besides the mentioned geometrical constraints, the design of a detector largely depends on the physics that is to be investigated. In $\overline{P}ANDA$, the nominal interaction rate is $2 \cdot 10^7$ $p\overline{p}$ annihilations per second, that means that the MVD will have to deal with high data rates. High data rates, in the order of kHz/channel, heavily affect the granularity of the detector and the development of the sensors and of the readout electronics. In addition, a resolution of around 100 μm in z and tens of μm in the $x - y$ plane is necessary to detect secondary vertices. Another consequence of being close to the point of interaction is the high radiation load, it is estimated to be 10 Mrad of total ionising dose and $10^{13} - 10^{14}$ $n_{1MeVeq}\, cm^{-2}$ of non-ionising in 10 years of data taking at 50% duty cycle.

1.5.2 Detector Layout

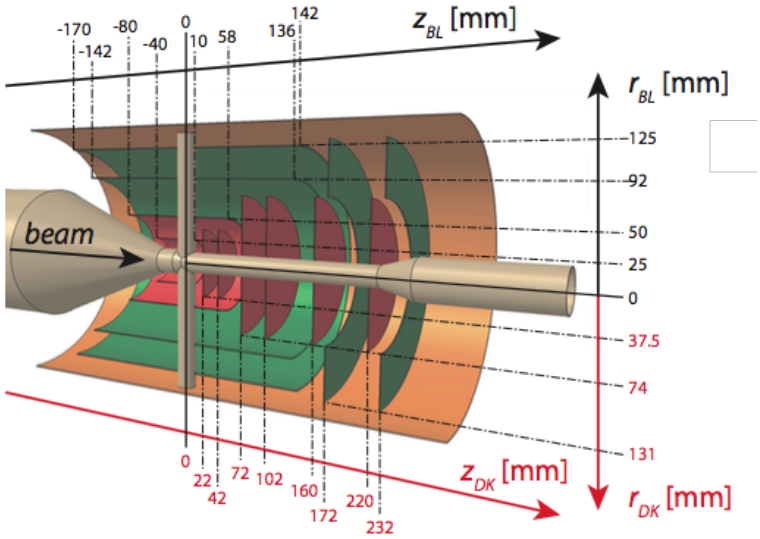


Figure 1.32: Geometrical layout of the MVD [69].

Following the requirements described previously, the basic geometry of the MVD is as follows. It consists of four concentric barrels that surround the beam pipe and six disks in the forward

direction. Since the detector is placed close to the interaction point, a high rate is expected. For this reason, the innermost layers, two barrels and part of the disks, are equipped with hybrid pixel detectors [70]. For the rest of the detector, the two external barrels and the external crowns for the last two disks, double-sided silicon strip detectors are used. The reason for this choice is that the silicon micro-strips are able to cope with the rates predicted in these regions, have a lower material budget than the pixels and are able to readout a large area with less channels [71]. The layout is shown in Figure 1.32. The hybrid pixel layers are given in red, along with the according axes, while the strip layers are given in green (black axes). The zero of the axes is positioned in the interaction point.The inner barrel has a radius of 2.5 cm while the outer layer has a radius of 12.5 cm. For the disks the smaller ones have a radius of 3.75 cm while the larger disks have 7.4 cm as radius for the pixel part and 13.1 cm for the strip crown part.
From Figure 1.32 and Figure 1.33 can be seen that the detector is designed to provide tracking for particles with an angle between 3° and 150°. With this particular design it is possible to have a minimum of four hit points for tracks between 9° and 140°. In the z-direction the detector extends from -17 cm to 23.2 cm. The operation temperature foreseen for the detector is 35°C, therefore a sophisticated cooling system is needed. It is realised using under-pressurised water that is injected with a temperature of 18°C.

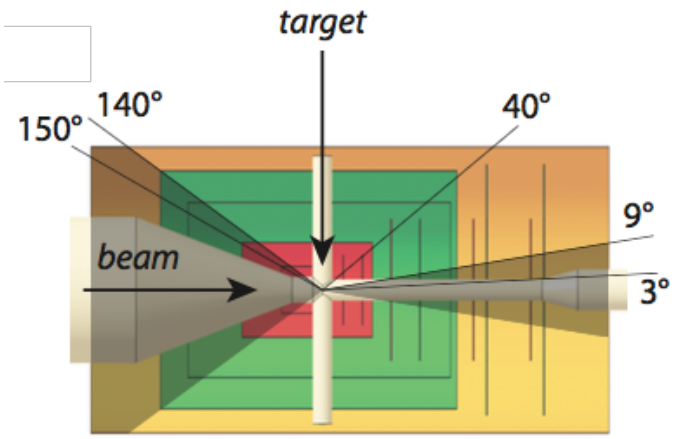


Figure 1.33: Geometrical layout of the MVD [69].

Every part added increases the material budget of the detector, the major contribution is given by cables for data and voltage supply, amounting to 37.7% of the entire material budget of the detector. The second largest contribution is given by the support structures that result in 28.5%, the cooling pipes account for 13.6%. Only the remaining 20.2% are taken up by the active material itself [45].

1.5.3 Pixel Detectors

As mentioned in the previous section, there are two different type of sensors, the hybrid pixels and the double sided micro-strips. In the following sensors and their readout are described in more detail.

In the MVD the sensors used to build the inner two barrels and disks are hybrid pixel. This technology is well studied and developed for high energy physics at CERN for the Large Hadron Collider (LHC) experiments. The basic principle is the following: a charged particle crossing the sensor generates electron-hole pairs due to ionisation, and the created pairs are separated by means of applying a reverse bias to the sensor. The charge is then collected and the resulting signal is amplified by the readout electronics that is directly connected to the sensors. Using Czochralski (Cz) wafer as substrate it is possible to grow an epitaxial layer of up to 150 μm. The epitaxial layer is segmented on the top creating a diode matrix. The complete structure for the hybrid pixels is then created by soldering each pixel to the corresponding cell on a readout chip through an In or Sn-Pb bump. In Figure 1.34 a cross-section of an hybrid pixel is shown.It is important to remark that the Czochralski substrate is removed at the end of the process in order to minimise the material budget.

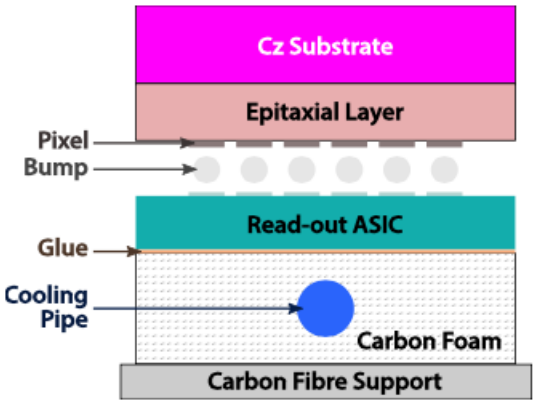


Figure 1.34: Cross-section of the hybrid pixel detector[45].

For the MVD each chip features 116 x 110 readout cells, each cell has a square shape of 100 μm x 100 μm. The pixels are implemented as p^+-type implants on an n-type epitaxial layer [72]. Since it is necessary to build disks with different radii, it is planned to have four different modules, as shown in Figure 1.35. The total amount of readout channels is $10.3 \cdot 10^6$, divided into 338 chips for the barrels and 472 chips in the disks.

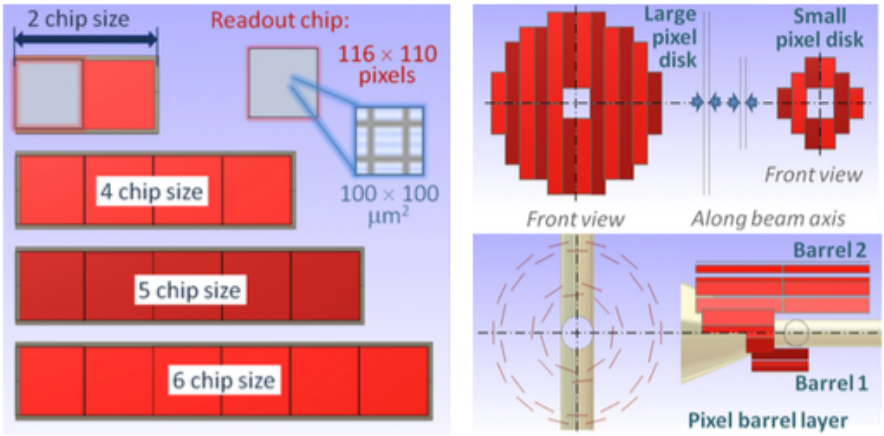


Figure 1.35: Pixel modules used to build disks and barrels [45].

As mentioned, each pixel is directly connected to its front-end readout, the Application-Specific Integrated Circuit (ASIC) called Torino Pixel (ToPix), developed in 130 nm CMOS technology [73]. The chip is based on the Time over Threshold (ToT) concept, which means that to measure the charge collected by the sensor, it is sufficient to measure the time that the signal processed by the front-end spends above a fixed threshold. This concept will be explained further in the next chapters.
The ASIC has an input charge range up to 50 fC, a preamplifier noise level lower than 200 e^- Equivalent Noise Charge (ENC). There are already four different prototypes delivered and tested. The fourth prototype has a power consumption of 120 mW per chip, working at the nominal clock of 160 MHz, leading to less than 800 mW/cm^2[47]. The time resolution is 6.8 ns with the nominal clock frequency. ToPix serialises the data to send to the off-detector components, it is therefore connected to a Gigabit Transceiver ASIC (GBTX) chip with a bi-directional transmission speed of up to 4.8 GB/s [74].

1.5.4 Strip Detectors

The strips are designed to provide a precise measurement in one direction since the silicon sensor is segmented in narrow strips, while for the second coordinate it is necessary to have a tilted array of strips as shown in Figure 1.36. As for the pixels, each strip is a reverse-biased junction allowing to collect the electron-hole pairs generated in the sensor. The signal is then amplified by the readout electronics positioned on the sensor edge. The achievable resolution with this system is given by the strip pitch p. If the particle hitting the sensor produces a signal on only one strip and assuming a uniform distribution of particles over the strip width,

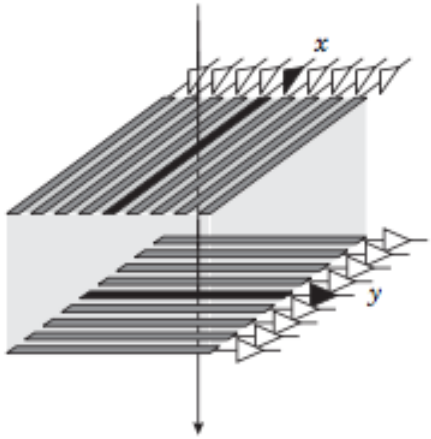


Figure 1.36: General concept for strip detectors.

the resolution becomes $\sigma = p/\sqrt{12}$. It is also possible to increase the spatial resolution if the charge is shared among neighbouring strips [70, 75]. The main advantage with respect to the pixels is that the number of readout channels is lower because one strip can cover a bigger region. The main disadvantage is that the particle rate is lower due to the ghost hit effect. This particular effect happens when two particles, at the same time, hit the strips as shown in Figure 1.37. Two sets of x and y coordinates are registered, and it is not possible to distinguish which is the real hit and which one is the ghost.

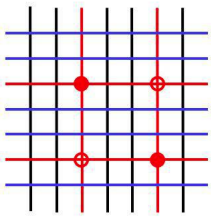


Figure 1.37: The two full dots are the real hits, the other two are the ghost points.

In the MVD, the sensors are double-sided micro-strips. The advantage of this kind of strips is that only one bulk is needed, minimising the material budget. The drawback is that there are some technical difficulties, for example, the proper biasing of the two types. The voltage between the two sides is strongly different, so it is important to isolate the two sides carefully. As in the case of pixels more shapes are needed to build the detector. In particular, rectangular and square shapes are needed for the two external barrels while a trapezoidal shape is needed for the crown of the last two disks. Figure 1.38 shows the layout for the three different modules. There are a few important difference between the barrel sensors and the trapezoidal sensors. The first one is the stereo angle of the strips that is 90° in the square and rectangular sensors

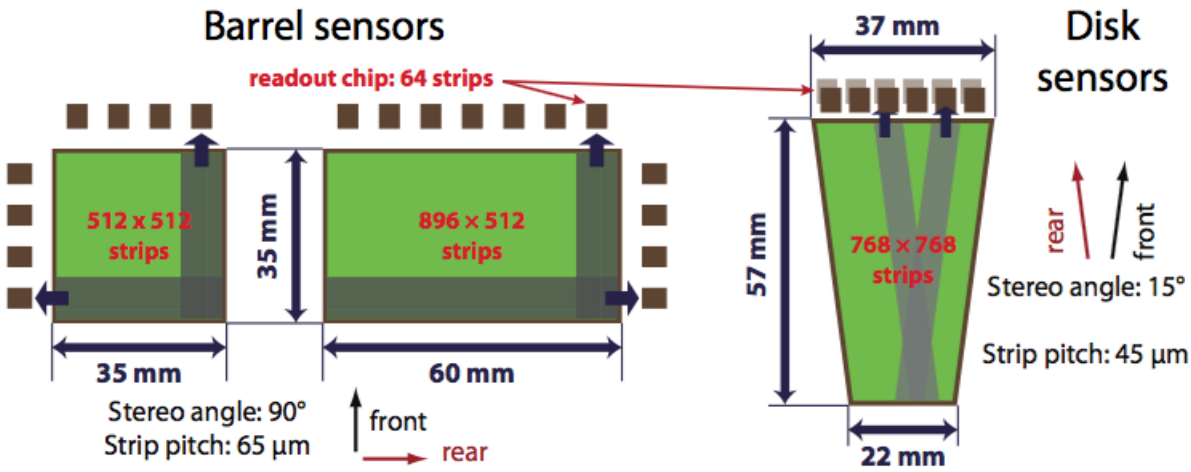


Figure 1.38: Layout of the three different shapes of strip sensors [69].

while for the trapezoidal sensors it is 15°. The second important difference is the strip pitch that is 65 µm in the barrels and 45 µm in the disks. However, all sensors have the same thickness of 285 µm and it is expected to put one passive intermediate floating strip between the strips connecting the readout electronics. In this way it will be possible to improve the spatial resolution due to charge sharing [76]. The main properties for the strips are summarised in Table 1.1.

Parameter	Value	Note
Capacitances	<10 pF	Rectangular short strips
	<50 pF	Rectangular long strips
	<20 pF	Trapezoidal strips
Input ENC	<800 e^-	C_{sensor} =10 pF
	<1000 e^-	C_{sensor} =25 pF
Dynamic range	240 ke^-	meaning around 38.5 fC (MIP = 4 fC)

Table 1.1: Double sided micro-strip properties [45].

The readout for the strip sensor is called PANDA STrip ASIC (PASTA), it is a highly-integrated front-end. It is produced with a commercial 110 nm CMOS technology, each ASIC has 64 readout channels. Since the design of PASTA is the main topic of this thesis, the details of the design and the characterisation of the prototype are described in detail in the next chapters. To cover the strip part of the MVD, up to 3112 PASTA chips are needed, leading to about 200000

readout channels. The total amount of channels is then 50 times smaller than one for the pixel part while covering more than four times the area.

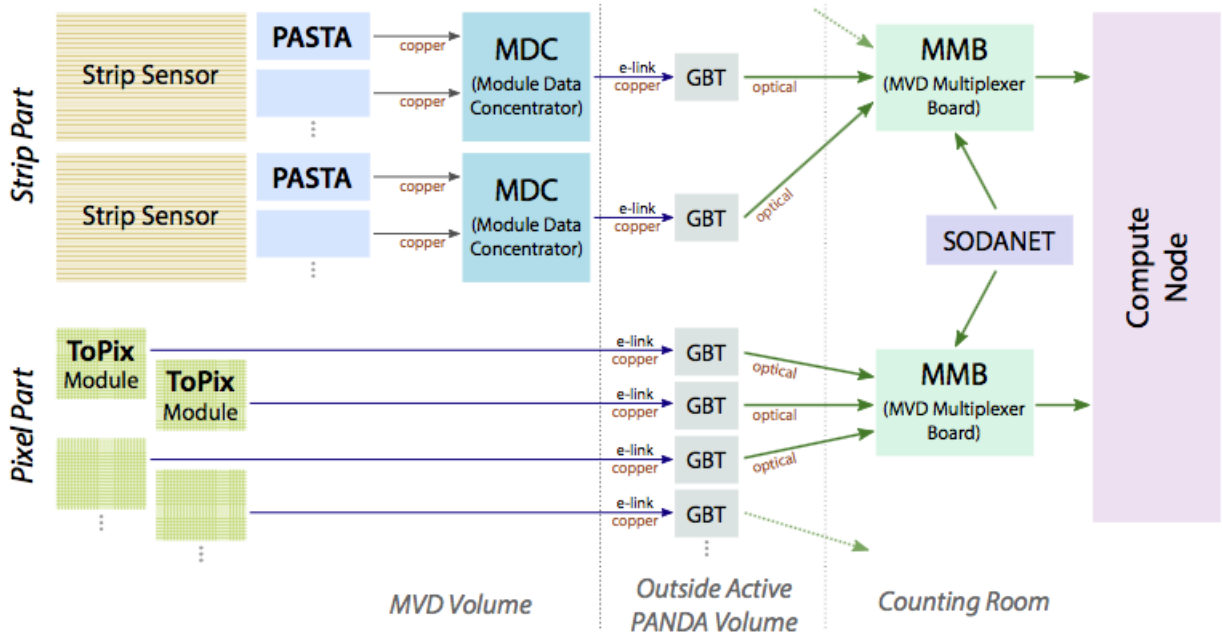


Figure 1.39: Block diagram for the MVD readout system from the sensor to the compute node.

The complete readout system designed for the MVD is shown in Figure 1.39. The strip sensors are readout by PASTA, the information is then processed inside the chip and sent to the Module Data Concentrator (MDC) [77] which is connected to the GBTX. The GBTXs, like in the pixel part, are connected via optical fibre to the MVD Multiplexer Board (MMB) from where the data are sent to the compute nodes.

2

PASTA ARCHITECTURE

In the previous chapter, it is described how the MVD is built. It is also shown which are the types of sensors that will be used and the respective readout chips. From this chapter to the last one the focus is on the development and the first tests of PASTA. The ASIC will be described from the top level to the deep structures with a particular focus on the analog Time to Digital Converter (TDC).

2.1 Motivation

For this project one of the most important requests is directly given by the $\overline{P}ANDA$ experiment, a trigger-less readout architecture. Another important point is the estimation of the $\overline{P}ANDA$'s reaction rate that is up to 20 million collisions per second [2]. From physics simulations, a resolution better than 20 ns is needed to distinguish two different events, thus the readout must be able to determine events, at least, with this time resolution. The average frequency expected of event in a single strip is 40kHz/channel [45]. The last constraint is given by the sensor. As mentioned in 1.5.4, there are three different shapes of strip sensors and this leads to a different input capacitance for the front-end architecture, as shown in Table 1.1.
The three different conditions outline a specific profile for the readout. Neither commercial circuits nor ASIC designed for different experiments match with the $\overline{P}ANDA$ requirements.
Nevertheless, to design a custom chip, additional information like size, power consumption and input charge range have to be set according to the MVD requirements and constraints. The main properties of PASTA are summarised in Table 2.1.
The task of the PASTA chip is to read and pre-processed the signal coming from the strip sensors in order to measure the energy loss of the particles in the silicon sensor. It is built with two different kinds of techniques, the full custom design for the analog part and standard-cell modules for the digital part. The analog part consist of a Front End chain, designed to perform Time over Threshold (ToT) measurements, an analog TDC, necessary to increase the

Features	
Process technology	110 nm CMOS
Input clock frequency	160 MHz
Input capacitance	10 pF to 35 pF
Input charge	1 fC to 38 fC (MIP=4fC)
Number of channels	64
Outer dimensions	(3.4 $\times$ 4.5) mm^2
Input pitch	63 μm
Power consumption	$\leq$4 mW/channel
Front End noise	< 600 e^-
Maximum capability	100 kHz/channel
Time binning	50 ps to 400 ps
Charge resolution	8bit (dyn. range)
Radiation tolerance	up to 100 kGy

Table 2.1: Main properties of PASTA [78].

energy resolution and to have a precise time stamp, some drivers and all the bias structures needed for the different architectures. The digital part can be divided into two blocks: the local controller and the global controller. The main task of the first is the configuration of local biasing and the control of all information coming from and to the analog part. It is also connected with the global controller that manages all the information coming from the 64 local controllers. The global controller is also connected to the global bias in order to configure them properly. It assembles all the data and it is the interface between the chip and the external environment through the drivers.

2.2 Measurement concept

As already mentioned, the main task of the MVD is to reconstruct the primary and secondary vertex and to contribute to determine the momentum of charged particles. It is important to have a precise time resolution and a very accurate knowledge of the charge deposited in the sensors, without forgetting the constraints, i.e. maximum size of the chip and acceptable power consumption. Similar requests were at the base of the EndoTOFPET-US project, where the Time of Flight for Positron Electron Tomography (TOFPET) ASIC was developed for the readout system of a multi-pixel photon counters [79]. However, some features do not match the $\overline{P}ANDA$ project as the input capacitance, the input charge, and the absence of radiation hardness protection circuits. The concepts on which the chip is based in interesting anyways.

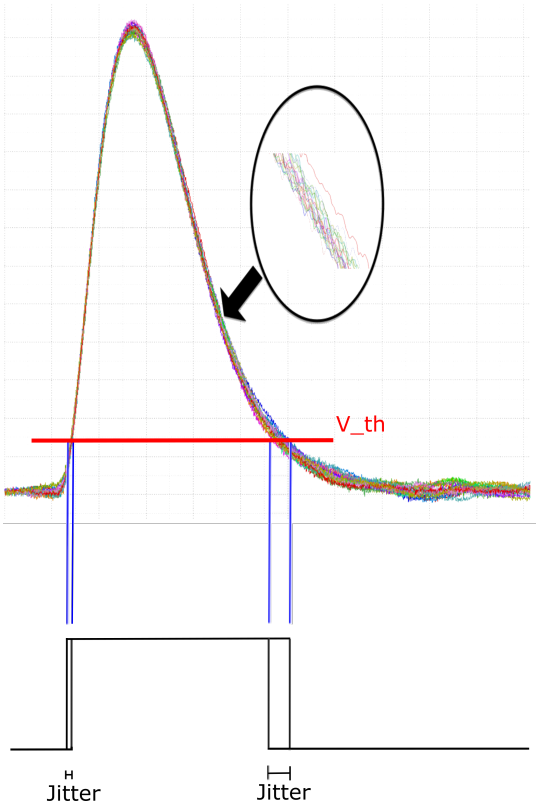


Figure 2.1: Different thresholds problems. In one case the jitter on the trailing edge is much bigger than the second case where the threshold is higher but the time stamp is less precise.

The basic idea is to obtain the charge information and the time stamp through a ToT measurement. The ToT technique is very powerful because it guarantee the linearity even if the signal

is saturated. It permits to handle a large charge range of input signals. In fact the technique works in such way that the charge information is obtained measuring the distance between the leading edge and the trailing edge of the signal forgetting its amplitude, leading to a specific Front End design. At the end of the amplification chain, when the signal has been amplified enough, there is a discriminator which distinguish the signals from the noise. The threshold value is an important parameter for the discriminators. If the threshold value is close to the baseline it is possible to achieve a precise time stamp for the leading edge but it is much more sensitive to noise fluctuations. The noise fluctuation are even more relevant, as it is possible to see in Figure 2.1, on the trailing edge, since its slope $\frac{\triangle V}{\triangle t}$ decrease with the approach of the baseline. On the other hand, if the threshold value is set higher it is possible to significantly reduce the effect of the noise fluctuations in the trailing edge but the precision for the time stamp in the leading edge is decreased.
To solve this problem it has been decided to use two different discriminators with two thresholds. The discriminator featuring the lower threshold is called *Time Discriminator* while the one with the higher threshold is called *Energy Discriminator.* Each discriminators produce a signal which suffer of large jitter, in the falling edge in the first case and in the rising edge in the second case. In order to solve these problems in PASTA, to perform ToT measurements, the rising edge of the first discriminator and the falling edge of the second discriminator are used as shown in Figure 2.2. In this way it is possible to reach a good time resolutions from both edges. Moreover, using this technique it is possible to decrease the sensibility to the noise, in fact the event to be stored must crosses both the thresholds.

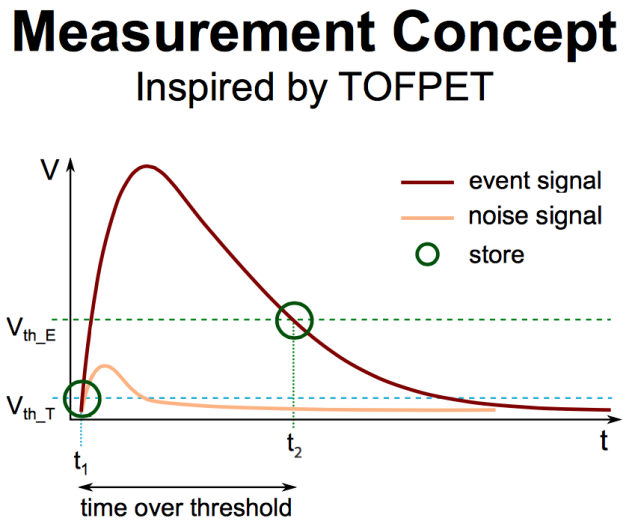


Figure 2.2: In PASTA the ToT is performed using two different threshold: one close to the base line to give a precise time stamp and the other as higher as possible to reduce the jitter in the falling edge of the signal and to be less sensible to the noise [80].

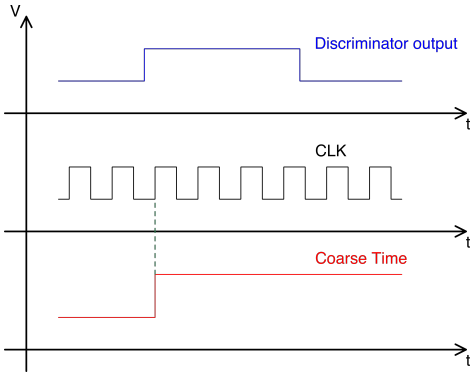


Figure 2.3: A coarse time measuring of an edge of the discriminator output is given by the clock.

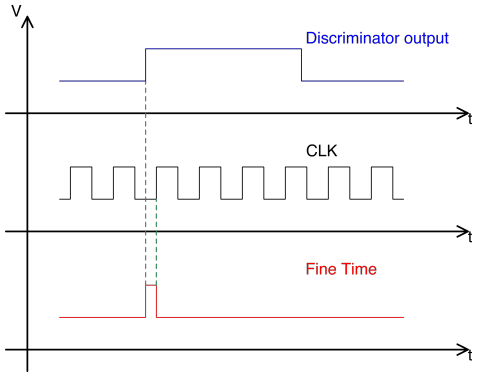


Figure 2.4: Fine time: time distance between the signal edge and the coarse time previously stored.

As already mentioned the chip has an external clock of up to 160 MHz, meaning that the maximum resolution possible is 6.25 ns ($\frac{6.25}{\sqrt{12}}$ rms). Since this resolution is not enough, an additional specific architecture to achieve a more precise time measurements is needed. For this reason, a TDC is implemented. The idea is to use the clock as a coarse time (Figure 2.3) and then use a TDC to measure, with an high resolution, the time between the leading (trailing) edge of the time (energy) discriminator output and the clock (Figure 2.4). Notice that the leading edge of the signal comes before the rising edge of the clock.
It was decided to use an analog TDC because this solution is compact, low power and has enough precision to fulfil the requests. Another solution could be to locally increase the clock frequency in order to achieve the needed resolution. The problem of this technique is the power consumption which increases a lot with the frequency and it is impossible to reach the needed resolution without crossing the limit given by the constraints. With the structure that was chosen it is possible to stretch the fine time in order to be able to measure it with the main clock without increasing the needed power. The details of the working principle are given in 2.3.1.2 while the implementation this structure is described in 3.2.

2.3 Structure

Since the chip is connected to a strip detector in the MVD, two important geometrical constraints have been set, one is the maximum dimensions of the chip that is $(5 \times 5)\ mm^2$ and the second one is the position of the connections that must be only two opposite edges. As can be seen in Figure 2.5, the final dimensions of the chip are $(3.4 \times 4.5)\ mm^2$. On the left of the chip

there are the pads for the communication to the sensors and on the right of the chip there are pads that will be connected to the external electrical line. Some additional pads are placed in the bottom pads are probing pads needed for the first prototype.
The picture also shows how the several circuits are placed in the ASIC. The region above the channel 0 is reserved for the bias needed by the analog structures and for a calibration circuit. The least generates a pulse, with a programmable amplitude, that is send to the input of one or more Front Ends in order to test one or more channels. In between the analog TDC and the local controller there are about 400 μm of free space in order to keep the digital and the analog environment separate. The 64 channels are then connected to the global controller which in turn is connected to 10 LVDS drivers (6 inputs and 4 outputs).

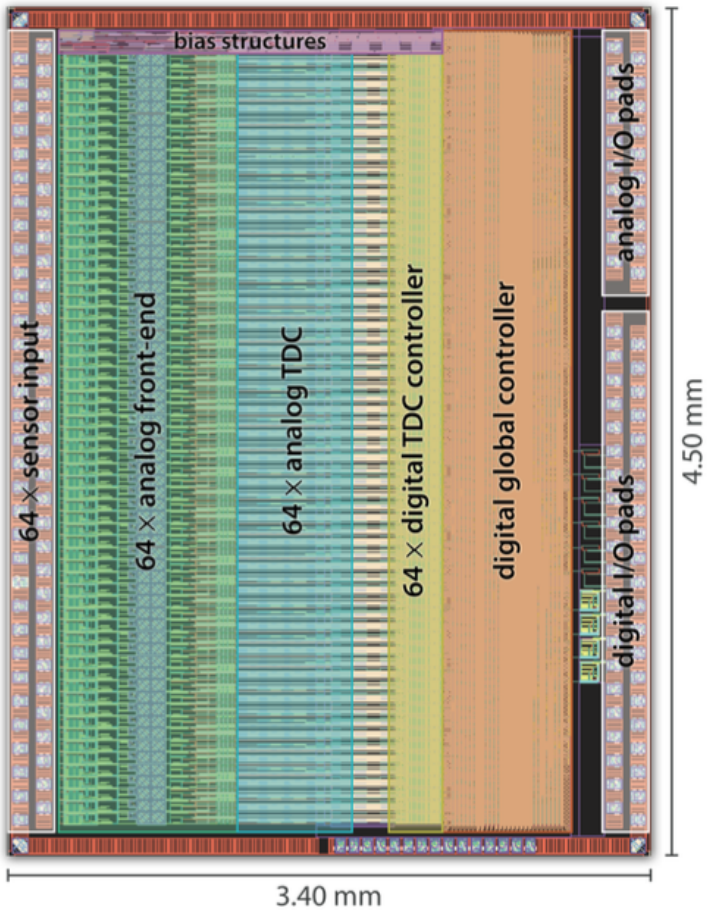


Figure 2.5: The several structures that compose the PASTA chip [80].

2.3.1 Channel structure

As described in the previous pages there are two different kinds of building blocks: in one group there are the structures that are independent for each channel while in the second group there are the structures unique for the whole chip. A channel, as shown in Figure 2.6, consists of the Front End, the TDC and the Local controller. The behaviour of these structures is explained in the following pages.

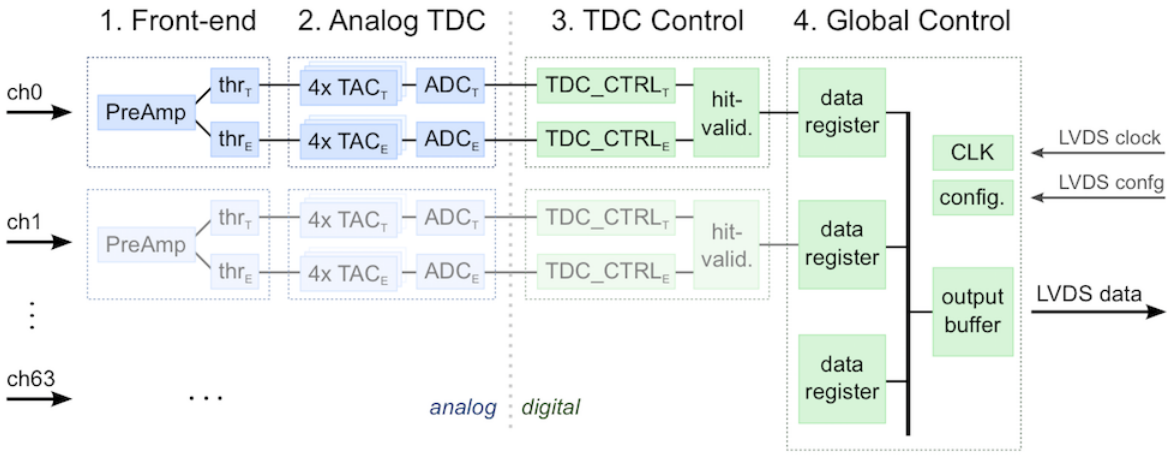


Figure 2.6: Building blocks for the PASTA core, in blue it is represented the analog environment while in green the digital domain [78].

2.3.1.1 Front-End chain

There are several Front-End architectures that can be chosen for a nuclear detector readout chip. Which type of structure has to be implemented depends on which features are requested. As already mentioned in Section 2.2, the features of the MVD demand a Front End based on a ToT measurement. Generally, to perform this measurement the structure used is quite simple, it is composed of an amplification stage and a comparator. As shown in Figure 2.7, the amplification stage is composed of a capacitor C_f in the feedback loop of a high-gain amplifier. In this way, the current signal input from the detector is integrated on the capacitor. Due to the constant current generator I_f, placed in parallel, the capacitor is then discharged in a time equal to Q_{in}/I_f.

The signal at the output of this stage, that is fed to a comparator, has a triangular shape. The time that this signal spends above the threshold V_{th} is linearly proportional to Q_{in}. The technique of the ToT is shown in Figure 2.8. Another remarkable thing is that for different value

of the feedback capacitor the duration of the ToT doesn't change because the peak amplitude is given by the ratio Q_{in}/C_f while the discharging slope depends on the ratio between I_f/C_f. Therefore, if for example the value of the feedback capacitor increase leading to a smaller amplitude the signal is compensated by a lower slope during the discharging phase [81].

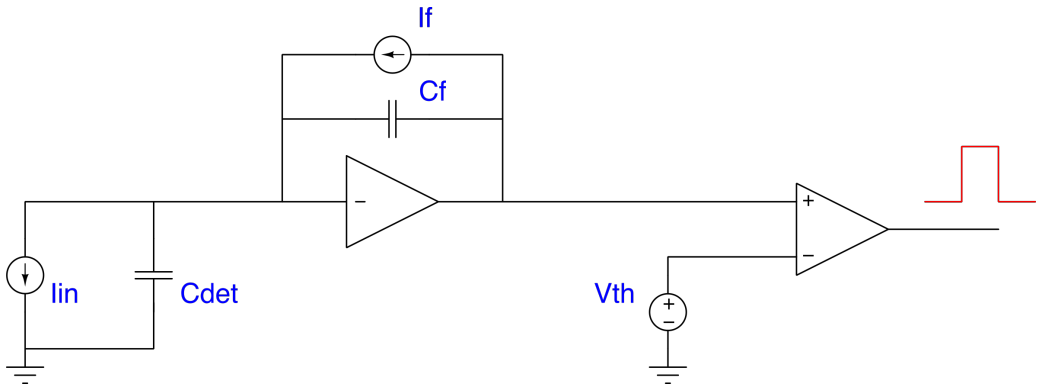


Figure 2.7: General Front End based on a ToT measurement, composed by an amplifier and a comparator.

One of the most important characteristics of the ToT architecture is that the signal can saturate the amplifier without losing the linearity of the measurement. When the amplifier is saturated its DC gain drops, leading to a situation where the approximation of the virtual ground at the input is not valid anymore. In this case, the extra charge that causes the saturation is integrated on the input node losing the linearity of the signal amplitude. However, the extra charge is removed by I_f, leaving Q_{in}/I_f unchanged (green signal in Figure 2.8). The linearity is maintained until the input signal is not high enough to push the structure used to generate the constant current out of the working region. In this case, if there is a significant capacitance between adjacent channels of the sensor , it is possible to incur on cross-talk problems between the channels [81].
The PASTA Front End has to be connected to the MVD strips that have a capacitance between 10pF and 35pF. This range excludes the possibility to have a ToT architecture connected directly to the strips without incur into the cross-talk between channels. However this technique suits the requirements needed for the application in the MVD very well. The only possible way for this chip to implement a ToT architecture is to use another amplification stage between it and the double-sided micro-strips. With this solution, the pre-amplification stage, connected to the sensors, must have a gain factor tuned in order to avoid saturation by the input signals. The structure used is based on a Charge Sensitive Amplifier (CSA) since it is a low power and low noise amplifier.

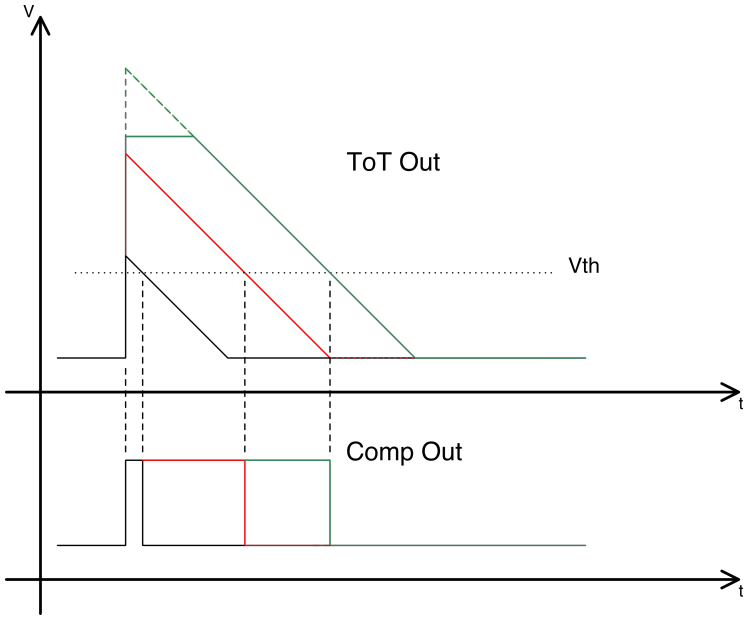


Figure 2.8: In the upper part there is the output signal of the ToT stage while in the lower graph is represented how the ToT is performed. Notice that the output of the comparator is proportional only to the length of the signals.

The Front End chain is then composed of two stages: a pre-amplification stage and a ToT stage. It is important that the output impedance of the first stage matches with the input impedance of the second one since it is hard to achieve with the chosen structure. A structure called Current Buffer has been placed between the two stages. This circuit has two tasks: the first one is to adjust the impedances between the two stages while the second one is to provide a further amplification. The amplification is needed since the second stage works better in the saturation region but the first stage cannot have a gain too high. With this structure in the middle, it is possible to have the best conditions for both the circuits in a wider range.
In general in circuits which implement the ToT technique the last stage is a comparator. However, in PASTA to perform the ToT measurement as show in Figure 2.2 two comparators, each with a different threshold, have to be implemented. From this point to the end of the TDC the channel is divided into two branches, one called time branch, that refers to the output of the comparator with the lower threshold and the second one called energy branch characterised by the higher threshold. In order to distinguish the two outputs of the comparators, they are named Discriminator Output Energy branch (DOE) and Discriminator Output Time branch (DOT).
The resulting Front End chain is made of four building blocks, as shown in Figure 2.9, which are discussed in more detail in section 3.1.

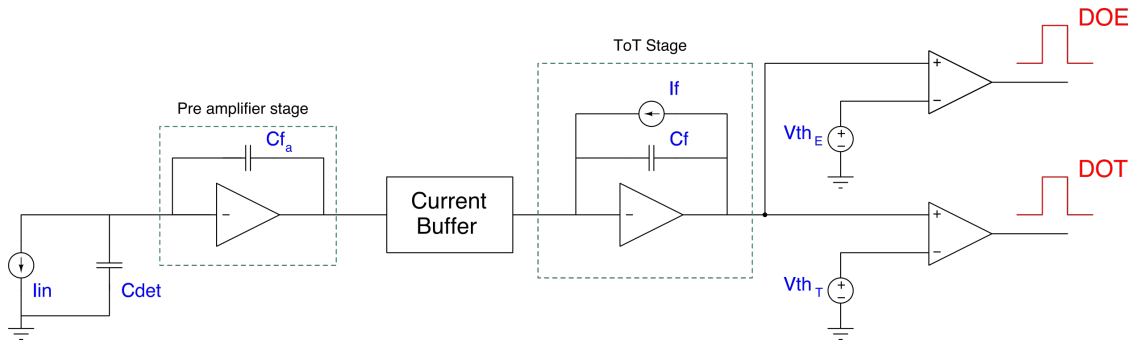


Figure 2.9: Schematic of the Front End chain used in PASTA, made by three stages and the comparators where the two different thresholds are applied.

2.3.1.2 Analog TDC

The second block is the analog TDC. As already mentioned there are two TDCs for each channel but the working principle and the structure are exactly the same for both branches. It consists of three building blocks: a current generator, a Time to Amplitude Converter (TAC) and a latched comparator, as shown in Figure 2.10.

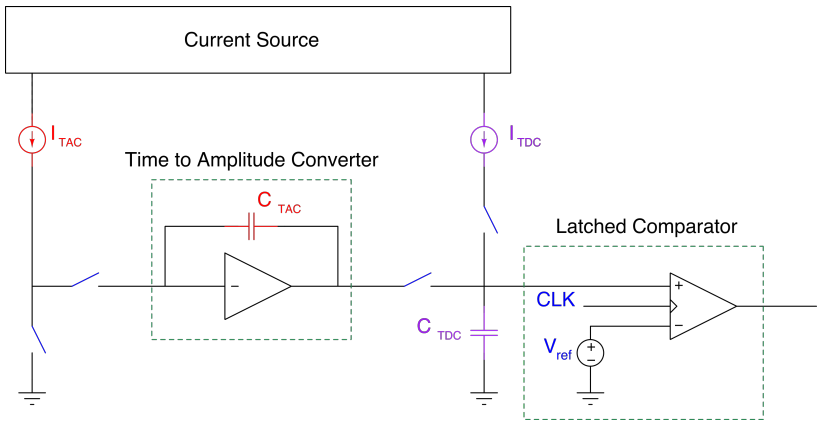


Figure 2.10: TDC building blocks.

The current generator is the structure used to provide two different constant currents each TDC. One of the most important parameters is the current ratio that must be fixed as precisely as possible. The second building block is the TAC that is the core of the entire architecture. Its task is to move the fine time information from the time domain to the analog domain, this is done by one of the two currents provided by the current generator that discharges the capacitance C_{TAC} . The voltage level reached by the capacitor is proportional to the time that the

current flows through the TAC amplifier. The most important parameter for this block is the amplification linearity. The last block consists of the second current, a capacitor called C_{TDC} and a latched comparator. These three structures, all together, constitute a Wilkinson Analog to Digital Converter (ADC), that converts the analog information stored into the capacitor into a digital information. The resolution of this conversion is given by the clock.

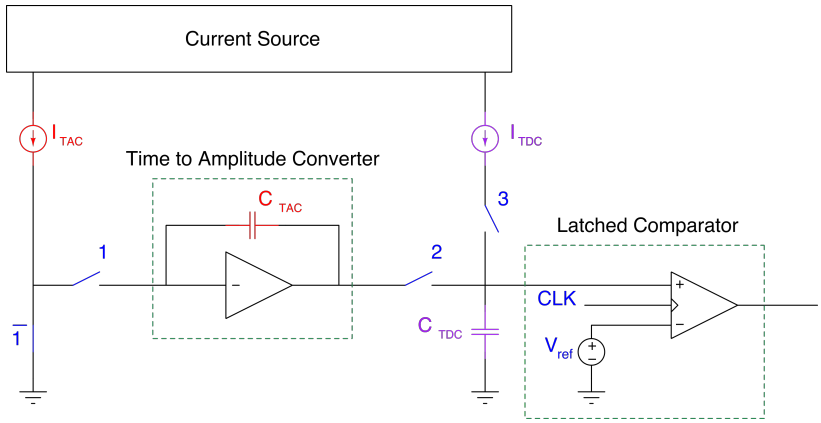


Figure 2.11: Representation of the switch positioning at the TDC starting phase.

To achieve the measurement of the fine time, the TDC works in four different phases.At the starting point the situation is the one described in Figure 2.11, where the switches 2 and 3 are open and switch 1 is set in order to have the current I_{TAC} that flows to ground. When the signal coming from the Front End comparator goes to "1" (for the time branch) or "0" (for the energy branch), the Local controller moves switch 1.

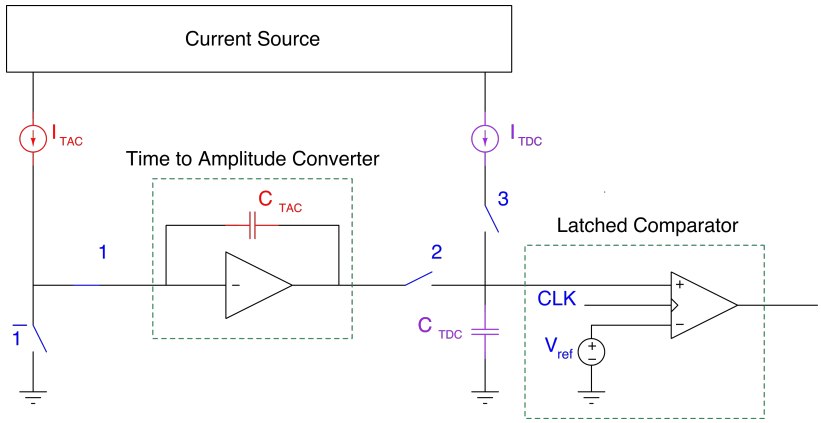


Figure 2.12: During the discharging phase of TDC the value of the switch number 1 is changed .

The setting is then the one shown in Figure 2.12, and it stays in this configuration until the next rising edge of the clock.
This time interval is exactly the fine time that is to be measured. The constant current I_{TAC}, in this phase, linearly discharges the capacitor C_{TAC} and the voltage value reached by this capacitor is proportional to the time that the switch number 1 is in this position and thus is proportional to the fine time as shown in Figure 2.13.

Figure 2.13: Voltage level of C_{TAC} during the discharging phase.

After the clock edge mentioned above, the switch configuration resets. In this moment the fine time information is stored on the capacitor C_{TAC} and the measurement of fine time begins with the third phase. This operation is called "charge sharing" because, closing only switch 2, the two capacitors C_{TAC} and C_{TDC} are connected. After a certain time the voltage value of the capacitor C_{TDC} reaches the same value stored in C_{TAC}. The most important thing in this phase is that the C_{TDC} is four times bigger than the C_{TAC}, leading on the first stretch of the time. The two voltages are shown in Figure 2.14, where the red line is the C_{TAC} potential while the violet one is the C_{TDC}.

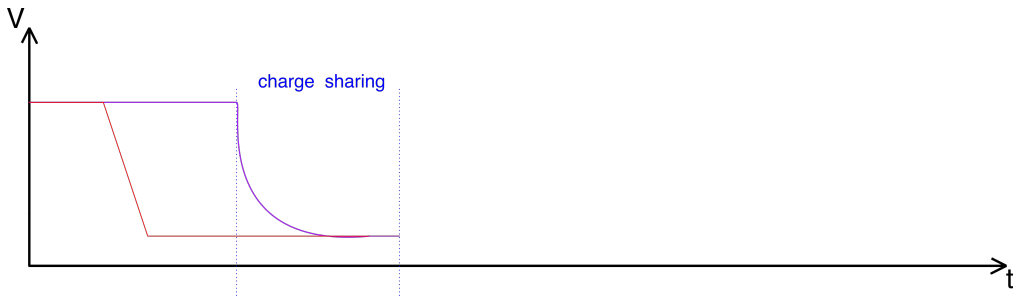


Figure 2.14: Voltage value for the C_{TAC} (red) and for the C_{TDC} (violet), after a certain time the two voltage value are equal.

The last part of the process is the recharging phase, the TDC switches are configured as shown in Figure 2.15.

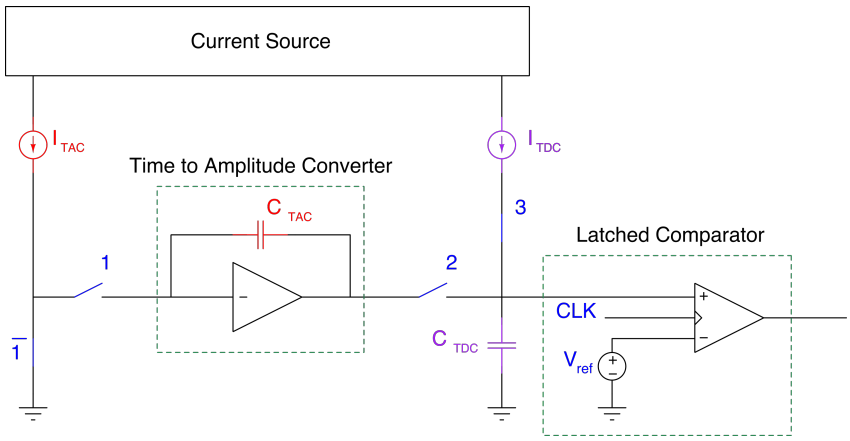


Figure 2.15: In the recharging phase the switch number 3 is close in order to recharge C_{TDC} with the current I_{TDC}.

When the Local controller closes the switch number 3 the second current starts immediately to recharge the capacitor C_{TDC}. This signal that close the switch is called Start Of Conversion (SOC). The end of the recharging operation is managed by the latched comparator. It has two inputs, the first one is the reference voltage, called V_{ref}, while the second one is the capacitor. When the voltage value of C_{TDC} is equal to V_{ref} the latched comparator changes the position of switch 3, with a signal called End Of Conversion (EOC). At this point the TDC is set back to the default situation and the recharging process is ended, as shown in Figure 2.16.

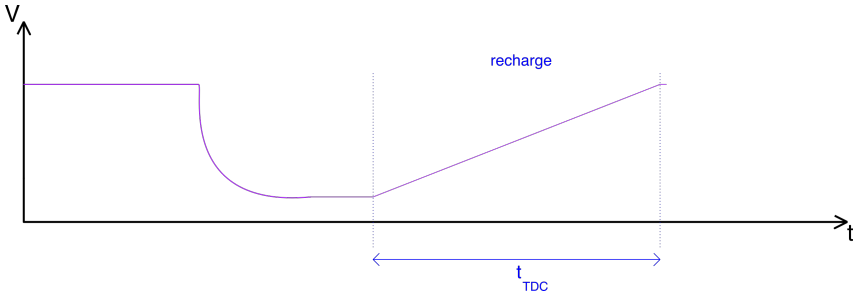


Figure 2.16: Voltage level of C_{TDC} during the recharging process.

From the Figure 2.17, that summarised the entire process, it is possible to see that the recharging ramp takes more time than the discharging ramp, obtaining the time dilation useful to measure the fine time with the main clock.

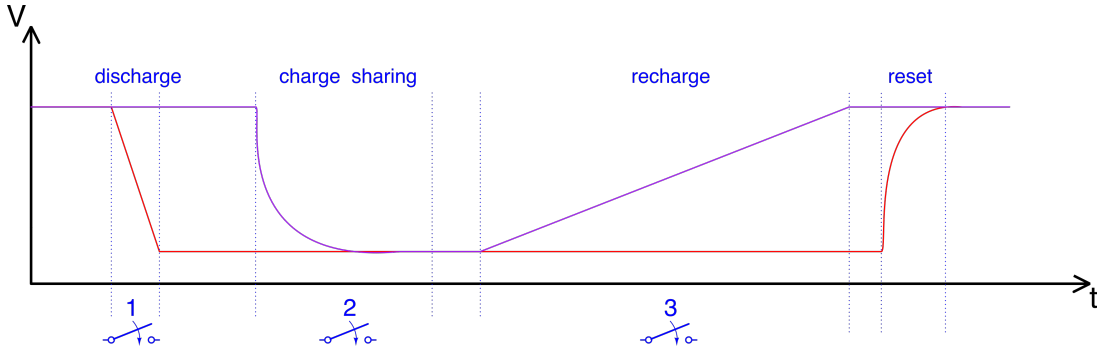


Figure 2.17: Complete process for the TDC, in red is reported the voltage value on the capacitor C_{TAC} while in violet on the capacitor C_{TDC}.

This effect is due to the fact that the capacitor C_{TDC} is four times bigger than the capacitor C_{TAC} and moreover the recharging current I_{TDC} is 32 times smaller than the current I_{TAC}. The relationship between the charge into a capacitor and a constant current is

$$Q = C \cdot V = I \cdot t \tag{2.1}$$

Since the voltage of the two capacitors is the same, because they were in connection for a certain period during the second phase, it is possible to have the following relationship

$$V_{TAC} = \frac{I_{TAC} \cdot t_{TAC}}{C_{TAC}} = V_{TDC} = \frac{I_{TDC} \cdot t_{TDC}}{C_{TDC}} \tag{2.2}$$

Thus the recharging time t_{TDC} is:

$$t_{TDC} = t_{TAC} \cdot \frac{I_{TAC}}{I_{TDC}} \cdot \frac{C_{TDC}}{C_{TAC}} = t_{TAC} \cdot \frac{32 \cdot I_{TDC}}{I_{TDC}} \cdot \frac{4 \cdot C_{TAC}}{C_{TAC}} = t_{TAC} \cdot 128 \tag{2.3}$$

That means that the recharging time is 128 times the discharging one, as shown in the Formula 2.3.

The resolution with which it is possible to measure the fine time depends on the clock period, in our case 6.25 ns, and on the precision of the ratio between the two capacitors (C_{TAC} and C_{TDC}) and the two currents (I_{TAC} and I_{TDC}). Therefore with the nominal values the minimum resolution achievable is

$$\frac{6.25ns}{128} = 48.8\, ps \tag{2.4}$$

The drawback of this technique is that it takes a long time to complete the second and third phase. During this time it is not possible to process any event. The maximum dead time

estimated is in the order of $4\mu s$. This is a problem considering that the maximum input rate of the chip is in the order of 100kHz. To avoid this problem it is necessary to increase the number of TACs with a negligible increasing of the power consumption. In this way it is possible to store the informations on different C_{TAC} and wait that the recharging process is ended without losing events. It is possible to calculate, with equation 2.5, the probability that one TAC is in the dead time when a new event arrives.

$$P = \frac{(r \cdot \triangle t)^n \, e^{-r \cdot \triangle t}}{n!} \tag{2.5}$$

r represents the rate of the chip, $\triangle t$ is the dead time while with n is the number of TACs. The results are reported in Table 2.2 where in the last column there is the probability to lose an event is given.

n	P	$1 - \sum_{i=0}^{n} P_i$
0	-	100%
1	67.03%	32.97%
2	26.81%	6.16%
3	5.36%	0.79%
4	0.71%	0.08%

Table 2.2: Calculation of the minimum number of TACs. In the first column there is the index n that represent the TAC number. In the second column there is the probability that the nth TAC is busy when a new event arrives. In the last column is reproted the probability to lose and event using n numeber of TAC

Table 2.2 shows that with three different TACs the probability to lose an event is less than 1% but it is close to it. Therefore as can be seen from Figure 2.6 it was decided to use four different TACs in order to have a probability close to 1‰ and to be sure to lose as little event as possible.

2.3.1.3 Local Controller

The Local controller is the last structure of each channel but it works like the core of the chip. It is connected with every part in the channel, both the Front End and the TDC, and it is also connected to the global controller.
Its first task is to analyse the two output signals of the Front End, the latter is combined with the clock in order to store the coarse times and the fine times. Once this information is saved, the local controller is ready to process the next event from the Front End. At the same time it

sends the needed signals to the TDC, leading it into the different phases. Even if there are two different branches in the channel the Local controller is unique. It sets the discharging phase separately for each TDC because the fine times, in most cases, are different for the two branches. The sharing phase and the SOC are the same for both branches while, due to the fact that the fine times are different, there are two EOCs. In order to be able to reconstruct the precise time measured by the two branches, five information have to be stored, the two coarse times, the SOC and the two EOCs.

Another important task for the local controller is the management of the TACs. In particular, since there are four amplifiers, it is important that a new event doesn't overwrite an old one. It is therefore important to have a structure, called TAC selector, that knows the ID of each TAC and checks in which phase it is. When a new event is detected and the first TAC is busy, the TAC selector chooses the next one to store the information, increasing the ID by one. When the TAC ends the measurement, it sends a signal to the Local controller which sends back a reset signal in order to clean the information stored in the C_{TAC}. If after the first four events the first TAC has not finished yet, the selector starts increasing the ID one by one until it finds the first that is rested.

In fact to perform the measurement precisely it is important that, at the begin of the discharging phase, the voltage value on C_{TAC} is exactly V_{ref}. The problem is that, when the TAC is waiting for a new event, the capacitor C_{TAC} is only connected to the amplifier, as shown in Figure 2.11. That means that C_{TAC} is slowly discharged by the leakage current that flows into the amplifier. If the waiting time is not that long it is possible to neglect the discharge effect, otherwise there is an important offset introduced to the fine time. This offset is hard to fix because it depends on the waiting time that is random and unknown. For this reason, in order to avoid this kind of problem, there is the possibility to set a maximum time in the Local controller after which the capacitor is connected to V_{ref} in order to refresh the nominal value. There is a 4 bits DAC that gives the possibility to have a refresh every 25.6μs with the configuration "0001" or every 419ms with "1111".

The use of the leading edge of the DOT to measure the time stamp and the falling edge of the DOE to measure the energy is not the only possible configuration. In Table 2.3 all the possibility are reported. The column named Time (Energy) Trigger shows which signal edge is measured with the TDC in the time (energy) branch.

Since the experiment and therefore the readout system is trigger-less, the ASIC works in continuos mode, sending data out constantly. For this reason it is necessary, in the Local controller, to have particular processes that determine if the signals stored match with a possible real event or not.

Mode	*Setting*		**Time Trigger**	**Energy Trigger**
	Test	Trigger		
Normal	0	00	rising edge of DOT	falling edge of DOE
slew rate	0	01	rising edge of DOT	rising edge of DOE
DOT only	0	10	rising edge of DOT	falling edge of DOT
DOE only	0	11	rising edge of DOE	falling edge of DOE
test 1	1	10	rising edge of test pulse	falling edge of test pulse
test 2	1	11	rising edge of test pulse	rising edge of test pulse

Table 2.3: Different modes to start the fine time measurement. There are two main cases, one where the TDC use the output signals of the discriminators in the Front End, the second where the Front End is ignored and it is used to trigger the TDC a test pulse instead of the discriminator outputs [78].

Event validation

The main check done is a hit validation. Since the chip has two thresholds it is possible that, due to the noise, a signal cross the lower threshold but not the higher one. This is what is called an invalid event. If the chip is in this condition, most of the architecture is disabled. How the validation signal is activated depends on which operation mode the chip is set. There are four different validations: Synchronous mode, Prediction mode, Deactivated Validation, and Test mode.

Synchronous mode

In this operation mode PASTA the signals DOT and DOE are evaluated as they come out form the comparator, meaning the DOT as first and the DOE as second. In the Front-End signal doesn't cross the higher threshold there is no DOE and the event is considered not valid and then it is discarded.

Due to the nature of this mode there both sequential and combinatorial structures are needed. The validation check performed by sequential structures while the measurement starts with the combinational logic. The presence of these two different type of logic can lead to a stability problem. The combinatorial circuits are made of logic gates like NOT, OR, AND, featuring operation time of few ps. On the other hands, the sequential circuits involve also buffer structure like Flip-Flop memory in which the output is updated every clock cycle. Indeed, every time that one information has to change the domain, from the combinational to the sequential or vice-versa, the time constraints have to match. For example, if an asynchronous signal, used by

a combinatorial logic, is used as input of a sequential one it is possibly to incur on metastability problems. How this problem is solved in PASTA it is explained later.

Prediction mode
In this particular case, the validation check is done only with the DOE signal. In fact, if the comparator of the energy branch fires, it means that Front End signals have crossed both time and energy thresholds. The drawback of this strategy is the resolution of the time because evaluating only the DOE, the time stamp is much more sensitive to time walk. In order to avoid this problem, it is necessary to measure also the DOT. Since the DOE refers to the highest threshold there isn't any case where it can fire before the DOT. For this reason to process first the DOE it is introduced delay line between the time discriminator output and the local controller. This is the reason why this mode is called prediction: when the ASIC measures the time information the energy one is already predicted.
With this technique, there are two main advantages with respect to the synchronous mode. The first one regards the information stored, in fact, if there is no valid event, the time branch is ignored. The second one is related to the hardware. In contrast to the synchronous mode in the prediction mode, the measurements are done only with combinational structures, avoiding possible metastability of the system.

Deactivated Validation
The ASIC also has the possibility to be set in a configuration in which the hit validation is switched off. In this mode either the DOT or DOE signals can activate the following structure. This configuration is quite similar to the prediction one because it is possible to process signals independently with the further possibility to have the measurement of the DOT without the energy information. If this happens, it is possible to recognise this situation form the fine time value. For the time branch if a certain value of the fine time is stored means that the signal crosses its threshold, however, if the fine time in the energy branch is zero, meaning that SOC and EOC fires at the same time and thus that the signal doesn't crosses the energy threshold.

Test mode
Since this is the first prototype, it is also planned to have a Test mode. In this configuration the local controller and the TDC can be tested while the Front End is ignored. Instead of using the DOE and the DOT, a test pulse is used according to the trigger configuration shown in Table 2.3.

From the validation mode "synchronous" it is clear that every time that an asynchronous signal has to be managed by a sequential circuit it is possible to run into problems. In general, every

time that an asynchronous signal is an input of a clocked structure and it arrives in a time window around the clock edge, the output of the structure is not well defined. Figure 2.18 shows an example of this problem for a Flip-Flop architecture. These kinds of problems are called metastability. This issue doesn't only affect the behaviour of the structure that has the asynchronous input but also the following chains. Therefore this undefined output, in most of the cases, is an input of one or more architectures. This means that it can be interpreted, for example, as a "0" for all the structures instead of "1" or, even worse, some architecture may interpret the output as "1" while others as "0".

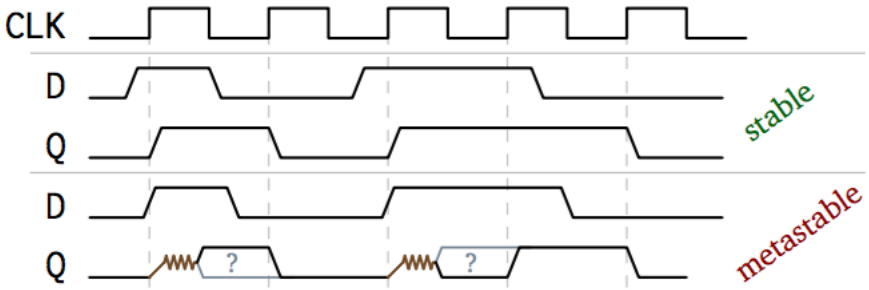


Figure 2.18: Representation of a Flip-Flop output in two cases: in first one the input is sufficiently far form the leading edge of the clock while in the second one is contemporaneous leading to an output that is metastable [78].

To avoid this problem in the local controller, two different countermeasures are applied. First of all, a cascaded Flip-Flop chain called synchronisation chain is inserted. This structure is the most used architecture to avoid metastability problems [82], in particular, every Flip-Flop reduces exponentially the probability of having an uncertainty on the output line. The right part of the Figure 2.19 reports the Flip-Flop chain present in the local controller. It is interesting to see that there is a multiplexer that selects at which point of the chain the output is taken. Since this is the first prototype and every Flip-Flop introduces a certain delay, the multiplexer is needed to optimise the times to avoid metastability problems.
The second architecture used is the one shown in the left part of Figure 2.19. The purpose of this structure is to have certainty to not lose events, using two Flip-Flops which update their output with a different phase of the clock. In this way, if the asynchronous signal arrives close to the rising edge of the clock and the first Flip-Flop is not able to recognise it, the second one will do so. Combining the two outputs with an OR, there is the certainty that if one event occurs, this structure is able to detect it.

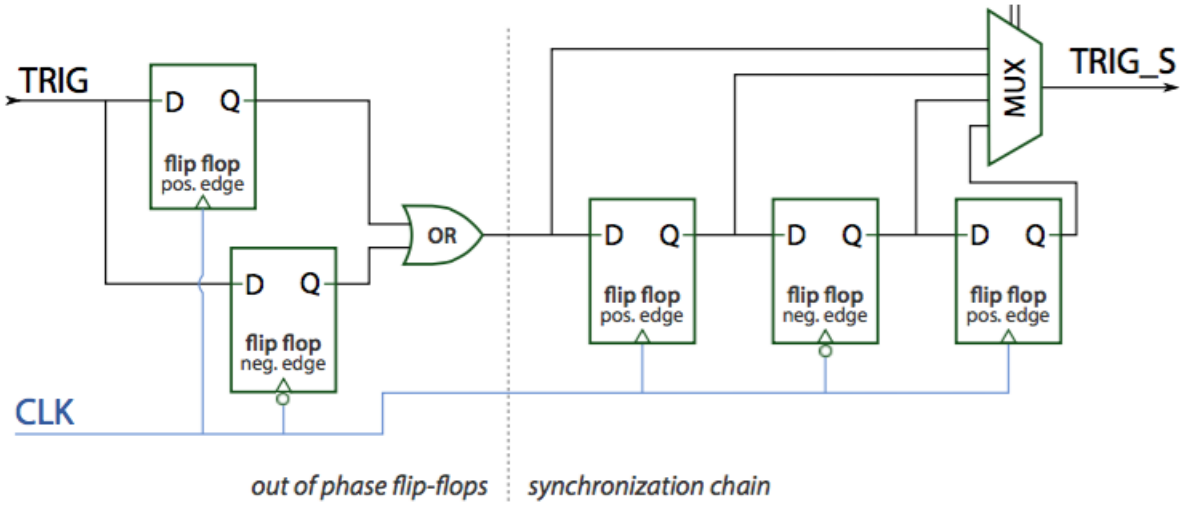


Figure 2.19: The first part is necessary to be sure to don't lose any asynchronous event while the second block is the structure implemented to avoid the metastability [83].

2.3.2 Global structures

The global structures present in the chip can be divided in three groups: global controller, biasing region, I/O circuits.

2.3.2.1 Global Controller

The PASTA global controller is the digital block that connects all 64 channels and combines their information. It manages the connections, and thus the configurations, of all global bias, handles the formatting of the data and the transmission. Its tasks can be grouped in five main blocks: *Control interface*, *Clock distribution*, *Test pulse generation* and *Data handling*. In the next pages, an overview of the tasks of the Global controller is given. For more detail about the Local and Global controller, see [78].

Control Interface

The settings in PASTA are fully digital and are split into local and global parts. Both configuration types affect analog, digital and test sections. The configuration that refers to the analog part consists of a modification of different DACs in order to adjust several parameters. The configuration of the digital part can activate or deactivate different processes, or set different time intervals, while for the test section it is possible to define different types of tests to check the behaviour and to calibrate the chip or the single channel.

In order to manage this large amount of information, there is a dedicated module that is directly connected to the interface of the chip through four lines. The first one is the Serial CLocK (SCLK) that is 10 MHz signal is used during the configuration process. There is also the Chip Select (CS) needed in presence of more than one chip connected to the same configuration lines. Then there is the Serial Data Input (SDI), where the configuration bits are sent, and Serial Data Output (SDO) where it is possible to see if the sending process is ended without problems or where it is possible to read the configuration registers values into the chip. The configuration sequence is sent to the chip through the SDI and it features a general structure that can contain four different fields. As seen in Figure 2.20 the first field is a command, a four bits sequence with which the global controller understands which is the operation that it has to do. The second field is the channel address (7 bits), the third one is the command data that doesn't have a specific length but depends on which command is inserted. The last field is the Cyclic Redundancy Check (CRC) (8 bits) that are used to be sure that the data has not been corrupted during the transfer of the configuration words between the PC and the chip. Depending on which type of command is sent the address field can be omitted, i.e. command for writing the bias global configuration is used to configure structures that are not related to a specific channel.

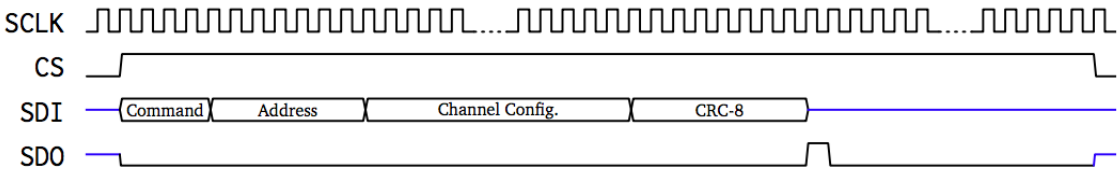


Figure 2.20: SDIstructure for a channel configuration [78].

Clock distribution

Since there are a lot of different structures in PASTA it is necessary to have three different clock values as shown in Figure 2.21.
$\overline{P}ANDA$ distributes to all sub-detectors a clock of 160MHz therefore also to the input clock of the ASIC. It is therefore important that the data output sent through TX0 and TX1 are transmitted with this frequency. However, within the chip, it is not mandatory to use the full clock but there is a module called clock divider that distributes the internal clock to the rest of the chip. This structure gives the possibility to reduce the clock frequency by a factor 2, 4 or 8. Having the possibility to reduce the clock frequency leads to the possibility of a reduced power consumption. As already mentioned, the control interface module has its own clock that is used only inside of this block. It is designed to be at 10MHz, which is considerably slower than

the main clock, to reduce power consumption for this operation and moreover to reduce the possibility of errors during the configuration data transmission.

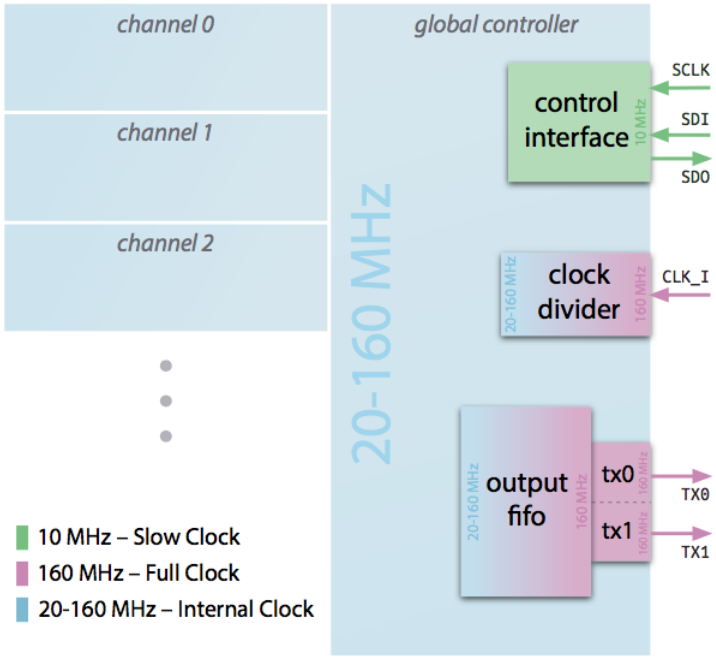


Figure 2.21: Distribution of the three possible clocks in PASTA [78].

Test Pulse generator

In the global controller, there is a module that can generate a customised pulse called internal test pulse. The output of the test pulse module can be modified in three parameters. The first one is a 10 bit word labeled N. Depending on which value is set, the module generates N+1 pulses. The second setting parameter is a 8 bit word called L. It defines how many clock cycles is the length of a single pulse. The minimum length is 1 clock cycle. The last parameter is the space between the pulses, tuned using a 8 bit word S, setting the pulse-space to $128 \cdot (S + 1)$ clock cycles.

Thus the generated internal test pulse can be used in two different ways. The first one is to test the TDC, the Local controller, and the global controller, the internal test pulses are then used by the local controller instead of the DOE and DOT. The second way uses the internal test pulses as a trigger for a circuit that generates current signals every test pulse. The current signal feeds directly to the input of the Front End. This procedure is one of the most comprehensive tests that is possible to do because every part of the chip is involved.

Data handling

Since the chip is trigger-less, the data events, as long as there is at least one TAC free, are continuously processed, so the data collection and transmission is a complex procedure. The collection phase starts in the local controller which, as mentioned in 2.3.1.3, stores five times in five buffer modules. In the global controller, there is an internal clock counter with 42 bits used to measure the times. When a flag that controls, for example, the SOC goes high the SOC buffer is connected to the internal clock counter and the last 10 bits are stored. Since the channels' time stamps are asynchronous, using a standard decimal counter can lead to counting errors. For this reason, the internal clock counter uses the Gray encoding.
The difference with respect to standard digital counting is that every number differs from the previous number by only one bit. For example, if a counter has to update one value from 1 to 2 it doesn't change the last two bits from "01" to "10" but from "01" to "11". In doing so, only the value of one bit is changed instead of both. This is particularly helpful for counters with a high number of bits. In case of PASTA, if the asynchronous signal that begins the storing comes during the Most Significant Bit (MSB) transitions, the mismatch between the real value and the stored one can be half of the dynamic range. However using the Gray encoding the maximum error can only be one Least Significant Bit (LSB).
Only when all five time stamps are stored and the event is validated, the buffers send the information to the global controller. Once the latter has read the data, it sets the valid event back to "0" for the involved channel. In this way, multiple transitions for the same data are avoided.

In the global controller, the first operation that is done on the data is the formatting. For this prototype, there is the possibility to have two format modes: full event mode or compact event mode.
The full mode is used for debugging purposes, it contains all the time information needed for the measurements reconstruction. Therefore all the local time information are in Gray encoding. An example of how an event is assembled in this mode is given in Figure 2.22.
For the compact mode, the length of the events is reduced from 80 bits to 40 bits. This is achieved by performing some basic math pre-processing in the global controller. First of all, TAC ID and channel ID are written only once because they are the same both for the energy and the time branch. Then two operations are performed, the first one concerns the coarse energy information which is stored with 10 bits. In fact only the difference $t_{\triangle coarse,E}$, between the coarse energy and coarse time is measured. The result is a 6 bit long word that limits the dynamic range of the pulse length to 2^6 clock cycles, i.e. 400 ns at 160 MHz. The second one is the compression of the informations concerning the fine times. Instead of storing the EOC_t, EOC_e, and two times the SOC only the difference between the SOC and the EOCs are stored.

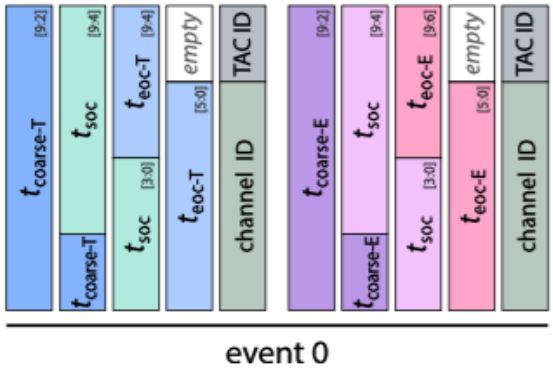


Figure 2.22: Full event mode, useful during the test phase. All the signals coming form the local controller are directly send out with any modifications.

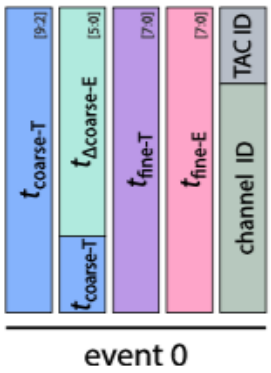


Figure 2.23: Compact event mode, useful during the normal operations. The data are pre-elaborated into the global controller reducing the redundancy.

The resulting signals are t_{fine-E} and t_{fine-T} . In Figure 2.23 is shown how the event looks like in a compact mode.
The form module arranges the data into 40 bit words, according to the mode chosen, and transfers them into the frame buffers where the final format for the data is assembled. Before the event data, 40 bits for the frame ID are placed preceded by 8 bits for the number of events contained. The sequence is terminated with 16 bits for the CRC. An example of a complete frame is shown in Figure 2.24. Once the frame is completed all the data are split in 16 bit words.
In order to speed up the formatting phase, there are two frame buffers, with 128 words of 40 bits each. They are used alternately, so that, while one is read out, the other buffer collects the new data. Every frame contains all the events in a time window of 1024 clock cycles. The maximum number of events that is possible to store is 128 for the compact mode and 64 for the full mode.
The last step are the connection to the two transceiver lines, called TX0 and TX1. In order to be sure that the lines are DC balanced, it uses the 8b/10b encoding. Every 16 bit word is then split into two 8 bit words. If both lines are used, the two words are sent simultaneously, otherwise they are transmitted sequentially on TX0. Another important thing to keep in mind is that there is the possibility that the chip is working with a clock frequency that is lower than the transmission one fixed to 160MHz. To avoid any kind of errors or misunderstanding between the two domains an asynchronous FIFO is inserted between the frame module and the transceiver lines.

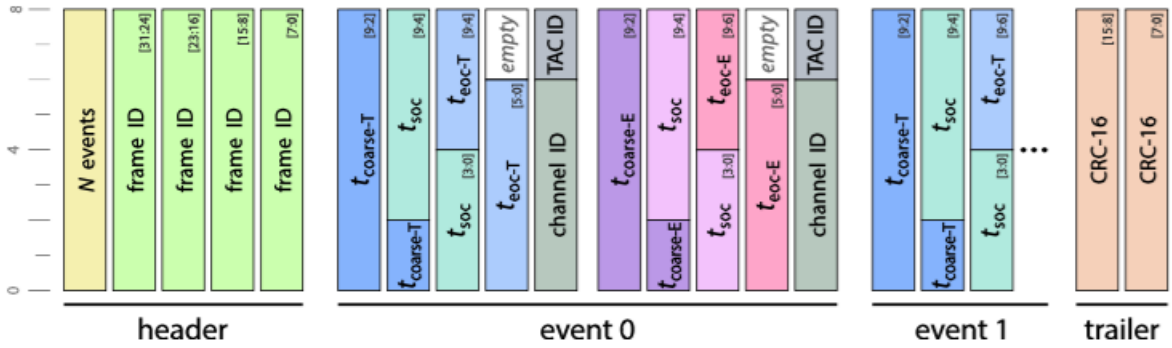


Figure 2.24: Example of a complete output frame in PASTA in the Full event mode [78].

2.3.2.2 Biasing Cells

As already mentioned at the beginning of this chapter, in the analog environment everything is fully custom and, every single architecture needs a different bias in order to be optimised. Moreover, in the ideal case, the biasing cells should be independent for each channel. This solution is clearly not possible for chips that have a lot of channels and stringent constraints in terms of power consumption and area used. For these reasons the common approach is to share biasing blocks between several channels. In PASTA, as shown in Figure 2.5, a region above the channel "0" is reserved for most of the biasing cells. However, few cells are placed individually for each channel in order to have some fine adjustments for the most sensitive parameters.

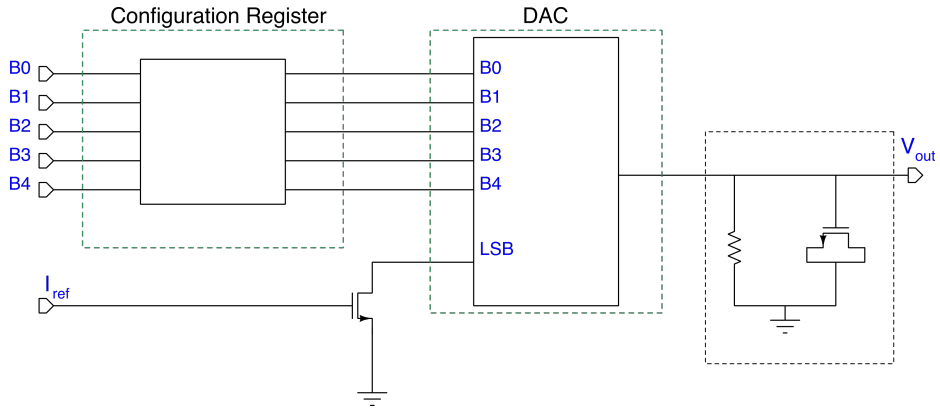


Figure 2.25: General PASTA bias cell schematic made by three structures. A configuration register necessary to buffer the configuration signals coming from the digital part, a DAC that set the needed current that has to be sent to the third group which can vary cell by cell.

The bias region is on the top edge of the chip thus it is important that all the channels, from channel "0" to channel "63", have the same bias values. There are 28 global biasing cells implemented in PASTA and every cell can provide one or two voltage values. Each cell is composed of a structure identical for each channel, comprising a configuration register and a 5 bits DAC, and a structure that varies from bias to bias. One example is shown in Figure 2.25.
The biasing cells are configured by the global controller. For this reason, the first block, that acts as an interface between the DAC and the global controller, is needed. It consists of ten inverters, two for each bit. Its task is to keep the value of the bit lines as stable as possible. The second block takes a reference current called I_{ref} and, due to P-MOS current mirrors, replicates this current in five different branches. Each branch produces a current equal to $2^B \cdot I_{ref}$, B represents which bit is connected to it. In this way, it is possible to have a 5 bit DAC that has the LSB equal to I_{ref}. The output current of this architecture, together with the third block, is used to generate voltage values that have to be sent in the channels. The third structure can be a resistor if the needed voltage is higher than 450mV as shown in Figure 2.25, or can be a series of current mirrors. In case of current mirrors, the output must be the gate-drain connection of a half current mirror, since the second half is placed in the channel. How many transistors are present in this part depends on two factors, the voltage value that must be reached and which kind of transistor, P-MOS or N-MOS, is the one that receives the voltage bias.

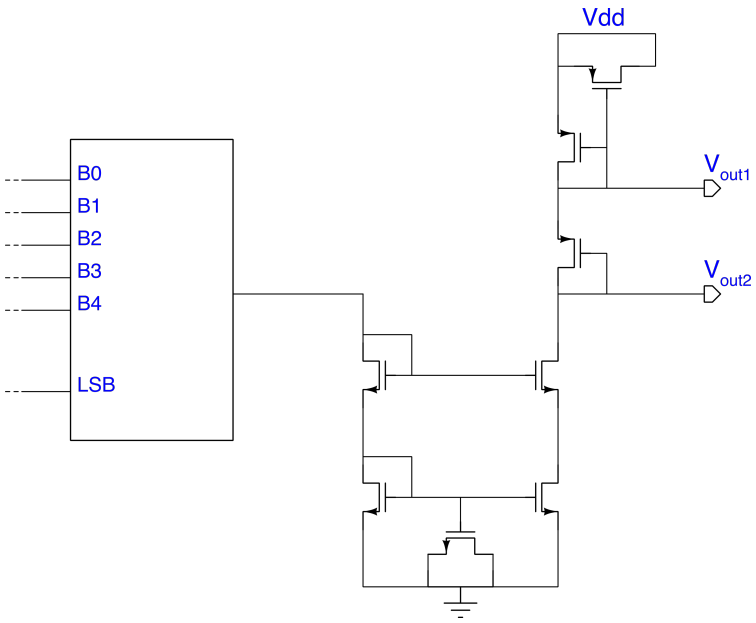


Figure 2.26: Third stage for a P-MOS connection with two voltage outputs.

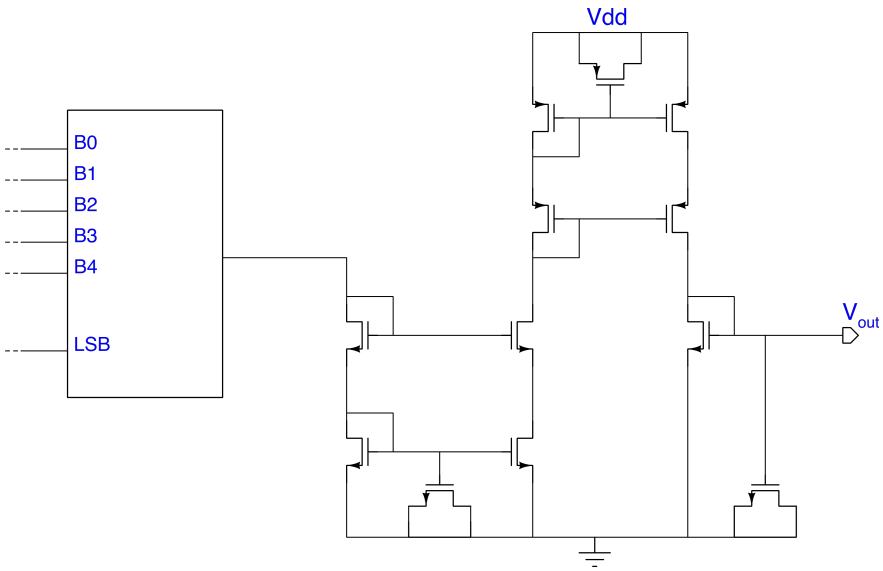


Figure 2.27: Third stage for a N-MOS connection, in this specific case with only voltage output.

The DAC output is always connected to an N-MOS current mirror. For this reason, if this bias is used to regulate a voltage value in a P-MOS gate, it is necessary to add half of a P-MOS current mirror or more, as shown in Figure 2.26. By adding more transistors it is possible to decrease, or if needed increase, the output voltage value. The voltage variation depends on the dimensions ratio between the transistors on the two current mirror branches. In these biasing cells, it is decided to have a low ratio and adding more mirrors in order to achieve more precise values. One example can be found in Figure 2.27. The resulting layout of one single cell is shown in Figure 2.28.

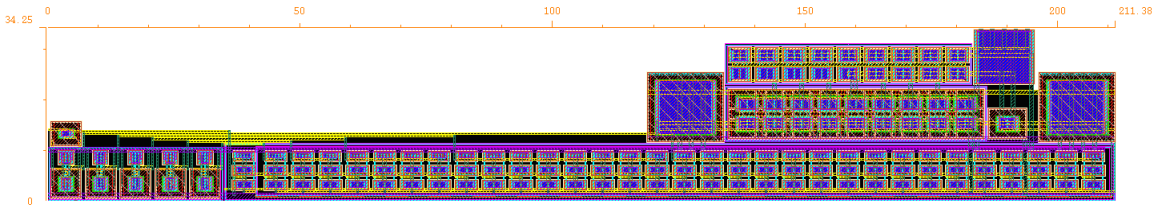


Figure 2.28: Layout of one bias cell, with a height equal to 34.25 μm and a length of 211.38 μm. In the bottom left there is the configuration register, then there is the DAC that cover all the bottom of the structure while in the upper right part there is the final stage.

The output of a biasing cell is a voltage value obtained weighing the current I_{ref} first form a DAC then from the third structure. This means that the value of this current must be as precise as possible. The I_{ref} current is then generated on chip with the circuit shown in Figure

2.29. With an external clean voltage called VBG, it is possible to generate a current that is stable enough to be used by all cells. As for the bias propagated in the channels also the reference current is propagated to all biasing cells in voltage. For this reason, the output of the I_{ref} generator architecture is a diode-connected transistor. For this first prototype, the VBG is provided externally.

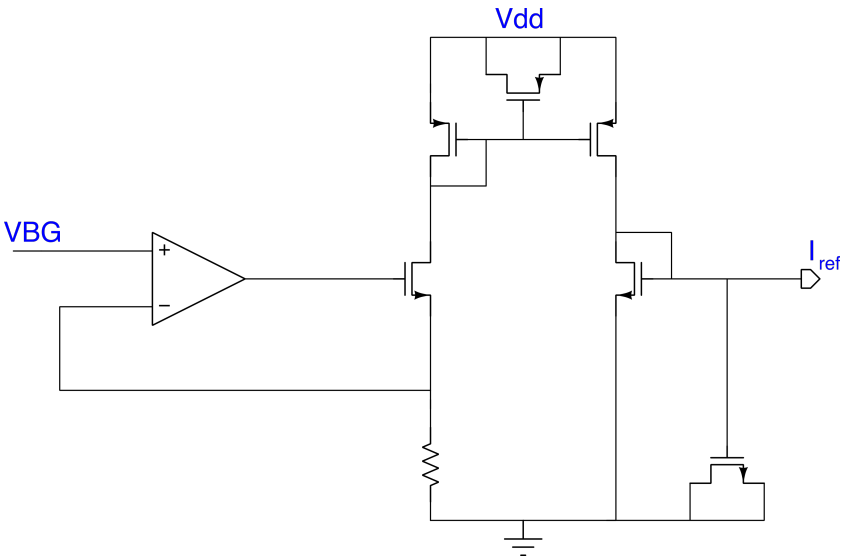


Figure 2.29: Structure that use an external voltage VBG to produce a very stable I_{ref} that is the current used from all the DACs in all the biasing cells.

2.3.2.3 Communications points

All the connections between the chip and the outside are done with a metal line that connects a specific point of the chip to a specific pad. As shown in Figure 2.30 there are several types of signals from the chip or to the chip. It is possible to group them into five groups: Test points, Front End inputs, external references, supplies, drivers I/O.
The first group includes the 15 pads on the bottom side and the first two in the left side. The 15 pads are connected to digital signals. The first 14 are connected to each local controller through a buffer while the last one is connected to the global controller. These signals are summarised in Table 2.4. The second pad on the left side is connected to the Front End output before the comparator, while the first one is the enable for this output. It is possible to directly see the Front End output only for channel "0".

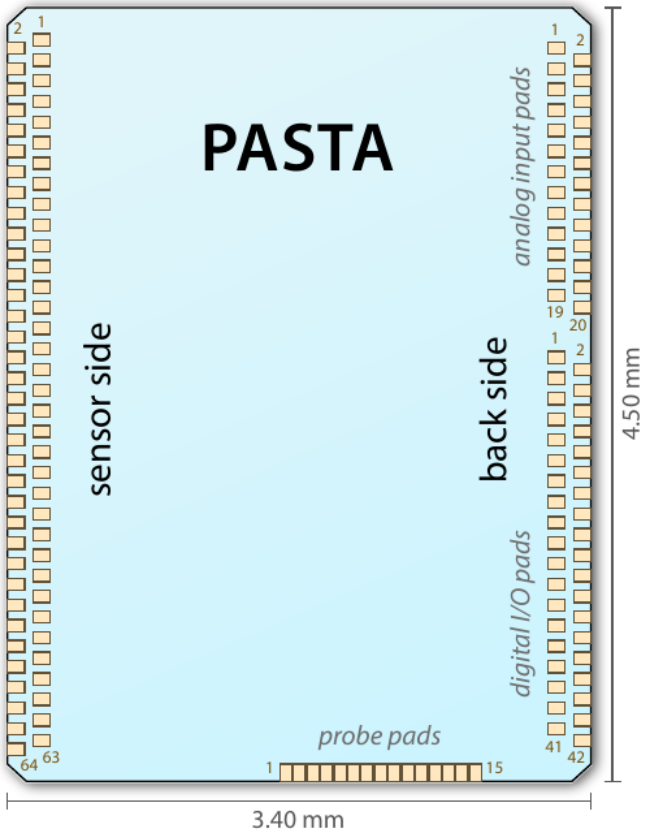


Figure 2.30: Footprint of PASTA.

The second group consists of the remaining pads in the left region. There are 64, one for each channel, because through these pads it is possible to send an input signal to the Front End. The external reference group is located on the right side. The chip is designed to have three different external references for three different reasons. The first one is the already mentioned VBG needed for the biasing cells, the second one is called CSA_{IB2} that is a voltage bias necessary for the Front-End (see section 3.1.1) and the third one is the V_{ref} that is the threshold of the latched comparator in the TDC (see sections 2.3.1.2 and 3.2). These three references are connected to the first three pads on the right side.
The fourth group is composed of 10 different supplies. It is important to notice that there is a separation between the pad number 20 and the pad 21. This break is done in order to keep the analog environment separated from the digital one. In the upper part, there is the analog power supply at 1.2 V, the analog ground level at 0 V and the analog substrate voltage 0 V, each of them have 5 dedicated pads. The last two pads in the analog environment are used to power the pad ring, number 19 is the analog substrate voltage at 0 V, while number 20 is the analog power supply for the pad ring at 1.2 V. A more detailed explanation how the pad ring is built

and how it works is described in section 4.3. Below the break, there are five pads for the power supply of the drivers at 2.5 V and 5 pads for the respective ground levels at 0 V. These 10 pads are also used to power the pad ring in the digital section. The last 12 pads on the right side are used to provide the power to the digital core with three values, the digital substrate voltage 0 V, the digital ground level at 0 V and the digital power supply at 1.2 V. Each of them has 4 dedicated pads.

Pad Number	Pad Name	Type	Description
1	DOT	Digital Out	Front-end comparator output (time branch)
2	DOE	Digital Out	Front-end comparator output (energy branch)
3	Time coarse	Digital Out	Flag for coarse time (time branch)
4	Energy coarse	Digital Out	Flag for coarse time (energy branch)
5	SOC	Digital Out	Flag for start of time to digital conversion
6	EOC_t	Digital Out	Flag for end of time to digital conversion (time branch)
7	EOC_e	Digital Out	Flag for end of time to digital conversion (energy branch)
8	ev_valid	Digital Out	Flag for a valid event
9-12	TAC_status[0:3]	Digital Out	If "0" TAC is free, if "1" TAC is busy
13	Comp_out_T	Digital Out	Latched comparator output (time branch)
14	Comp_out_E	Digital Out	Latched comparator output (energy branch)
15	playload_r	Digital Out	Last bit of the internal control link shift register*

Table 2.4: Pads in the bottom side

The last group of connections is composed of the in-/output signals. They are placed between the power lines of the drivers and the digital power lines. There are 10 signals, 4 output and 6 input, leading to the use of 20 pads because the drivers follow the LVDS standard. Table 2.5 summarises all the connections on the right side.

Pad Number	Pad Name	Type	Description
		Analog Section	
1	VBG	Vbias	External reference voltage for the bias cells (600 mV)
2	CSA_IB2	Vbias	External reference current for the bias for the preamplifier (800μA)
3	Vref	Vbias	External reference voltage to set the latched comparator threshold (850 mV)
4-8	AVDD[0:4]	Power	Analog power supply (1.2 V)
9-13	AGND[0:4]	Ground	Analog ground level (0 V)
14-18	AVSS[0:4]	Substrate	Analog substrate voltage (0 V)
19	AGNDIO	Substrate	Analog substrate voltage for the pad ring (0 V)
20	AVDDIO	Power	Analog power supply for the pad ring(1.2 V)
		Digital Section	
21-25	DVDDIO[0:4]	Power	Digital power supply for pad ring and LVDS (2.5 V)
26-30	DGNDIO[0:4]	Ground	Digital substrate voltage for pad ring and ground level for LVDS (0 V)
31	Test_Pulse -	LVDS In	Input for the external Test Pulse
32	Test_Pulse +	LVDS In	Input for the external Test Pulse
33	SYNC_RST -	LVDS In	Synchronous reset
34	SYNC_RST +	LVDS In	Synchronous reset
35	CLK_I -	LVDS In	Main clock (160 MHz)
36	CLK_I +	LVDS In	Main clock (160 MHz)
37	SDI -	LVDS In	Serial configuration data input
38	SDI +	LVDS In	Serial configuration data input
39	SCLK -	LVDS In	Serial clock (10 MHz)
40	SCLK +	LVDS In	Serial clock (10 MHz)
41	CS -	LVDS In	Chip select for configuration
42	CS +	LVDS In	Chip select for configuration
43	CLK_O -	LVDS Out	Main clock output to synchronize the serial data output
44	CLK_O +	LVDS Out	Main clock output to synchronize the serial data output
45	TX0 -	LVDS Out	Serial serial data output, first line
46	TX0 +	LVDS Out	Serial serial data output, first line
47	TX1 -	LVDS Out	Serial serial data output, second line
48	TX1 +	LVDS Out	Serial serial data output, second line
49	SDO -	LVDS Out	Serial configuration data output
50	SDO +	LVDS Out	Serial configuration data output
51-54	DVSS[0:3]	Substrate	Digital substrate voltage (0 V)
55-58	DGND[0:3]	Ground	Digital ground level (0 V)
59-62	DVDD[0:3]	Power	Digital power supply (1.2 V)

Table 2.5: Pads in the right side

3

CHIP IMPLEMENTATION

In the next pages, a detailed overview of the implementation of the analog structures is given. The chapter is divided into two parts. The first one is dedicated to the Front End architecture where I have participated in the layout phase design during my Ph.D. The second one focuses on a detailed description of the TDC since this represents one of the main tasks of my Ph.D. work.

3.1 Front-End

As already mentioned in section 2.3.1.1, the Front End used in PASTA is based on a ToT measurement and is composed of four different building blocks: a Preamplifier stage, a Current Buffer, ToT stage and two hysteresis comparators.

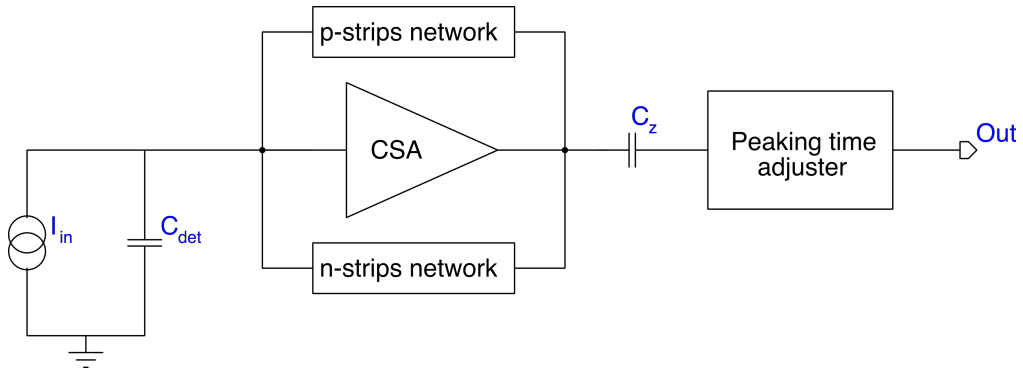


Figure 3.1: Representation of the building blocks of the preamplifier stage.

3.1.1 Preamplifier stage

This structure is the first one in the Front End chain, it is connected to the input pad where the sensor is wire bonded and its main task is to amplify the input charge signals without reaching the saturation of the amplifier, as mentioned in 2.3.1.1. The Figure 3.1 shows that the preamplifier stage comprises three main blocks: a CSA, two feedbacks networks, and a peaking time adjuster.

CSA

The CSA used in PASTA is a telescopic cascode amplifier with split bias currents called CSA_{IB1} and CSA_{IB2}. The output stage of this structure is realised by a buffer connected to the feedback capacitor as shown in Figure 3.2. The main purpose of the splitting of the currents is to reduce the power consumption of this stage without compromising the performance too much. For the first prototype the voltage value CSA_{IB2} is not generated in the chip but provided externally using pad connections.

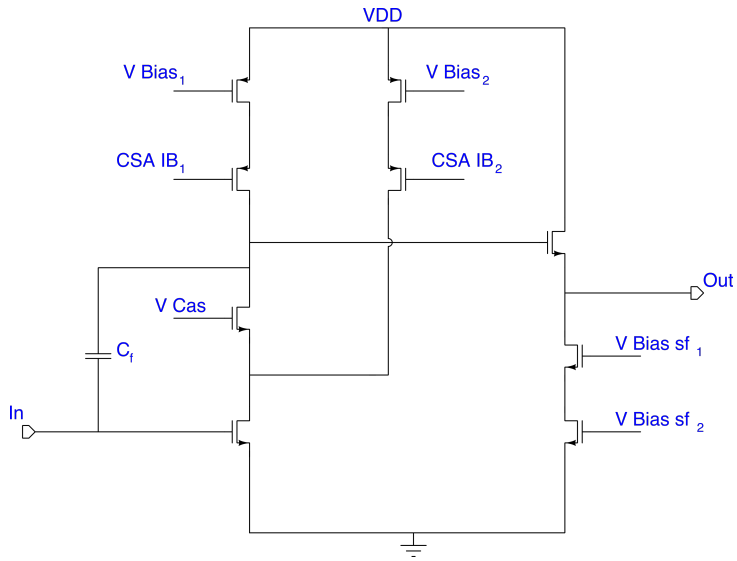


Figure 3.2: Architecture of the CSA implemented in PASTA.

Active feedback network

Since the micro-strips which the Front End is connected to are of two types, the generated signal has a different shape depending on whether it is generated from the p-type or n-type strips. The preamplifier stage in PASTA, thanks to the active feedback network is able to process both

signals and return one that always has a positive polarity independent from the connected strip. This is an important feature because it permits to have the same design for the following architectures. The two different networks can be activated through several switches controlled by the global controller. In this network it is possible to include also the capacitor C_Z that is used for the pole-zero cancellation necessary to determine the shape of the signal.

Peaking time adjuster

The last building block of the preamplifier is the peaking time adjuster that is necessary to modify the peaking time of the signal in order to match the specifications given by the sensor developer. In particular, it is necessary to reach a peaking time of 50 ns in order to reduce the noise foreseen in case of radiation damage.
Figure 3.3 shows the simulated behaviour of the preamplifier. The blue signal is the voltage input for the n-strips, while the red voltage signal is for the p-strips. The resulting outputs, evaluated in current, have the same polarity. The violet signal is the output of the n-strips while the green one is for the p-strips.

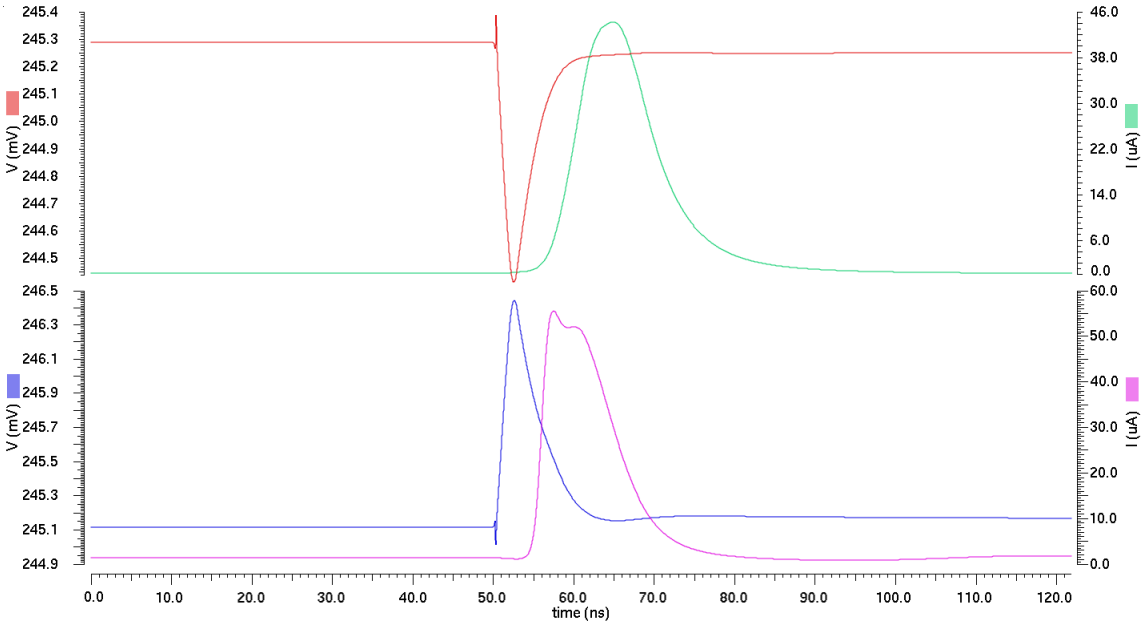


Figure 3.3: The blue line represents the voltage at the input of the preamplifier when a n-strip is connected, while the violet line shows its output current. The voltage signal in red is the input when a p-strip is connected to the preamplifier and the output is represented in green. Notice that the outputs have the same polarity.

3.1.2 Current Buffer

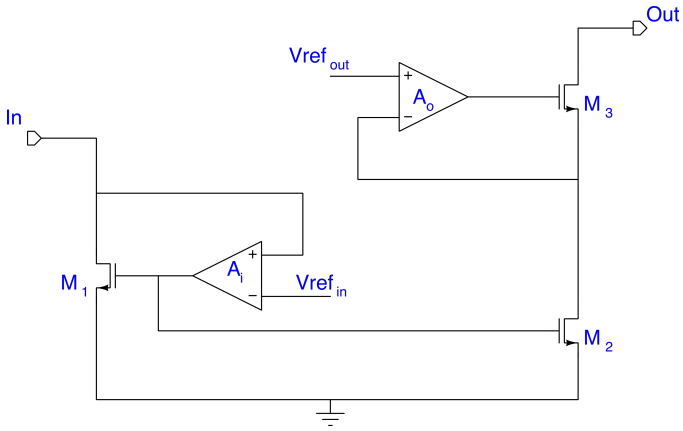


Figure 3.4: Current buffer architecture

The second block of the Front End chain is the current buffer. This structure has two main tasks: amplify the current and thus the charge for the next stage and adjust the impedance between the preamplifier stage and the ToT amplifier stage. It is possible to satisfy these two requests using the structure shown in Figure 3.4.

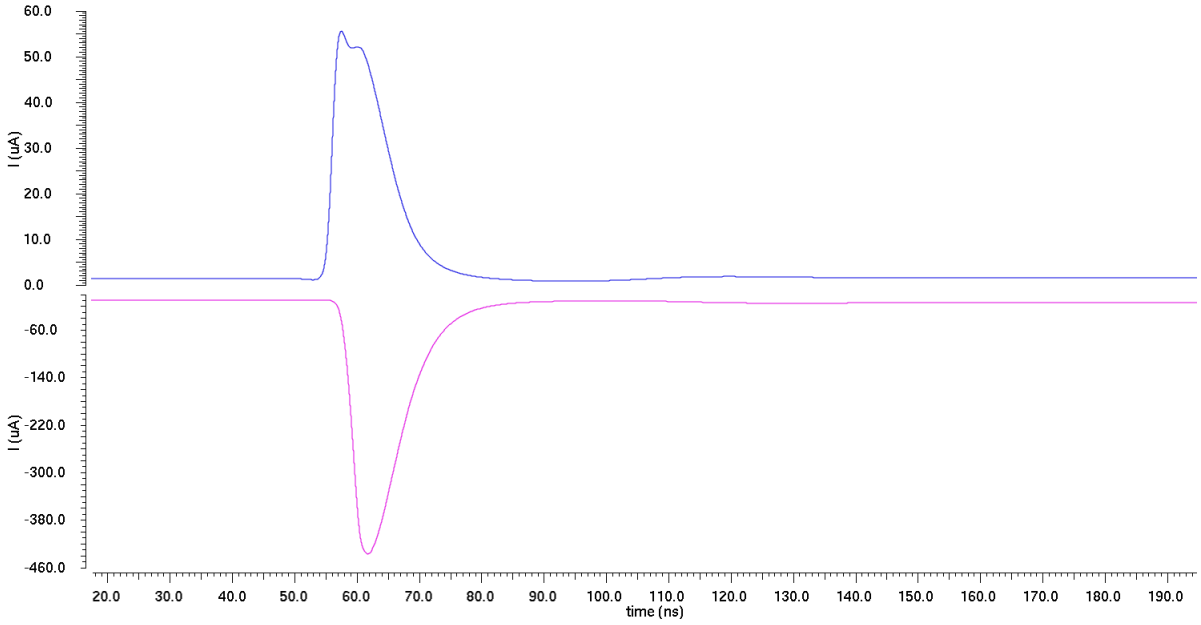


Figure 3.5: The output of the preamplifier stage is injected to the current buffer and is represented by the blue signal. The output of the current buffer is shown in purple.

The technique used for this design is called gm-boosting, in this way it is possible to achieve a small input resistance and large output resistance. The input resistance is given by the inverse of the transconductance of M_1 times the gain A_i, leading to an impedance in the order of hundreds of ohm. The output resistance is given by the gain $A_o g m_3 r_{out\,2} r_{out\,3}$ which is in the order of hundreds of $M\Omega$.
Figure 3.5 shows how the signal coming from the preamplifier stage is modified and presented to the next block. The input signal of the stage is shown in blue while the purple line is the output.

3.1.3 ToT amplifier stage

The ToT amplifier stage is the last architecture before the comparators, it is composed of two blocks: a differential amplifier with a high gain and a baseline restorer. Figure 3.6 shows how this stage is built.

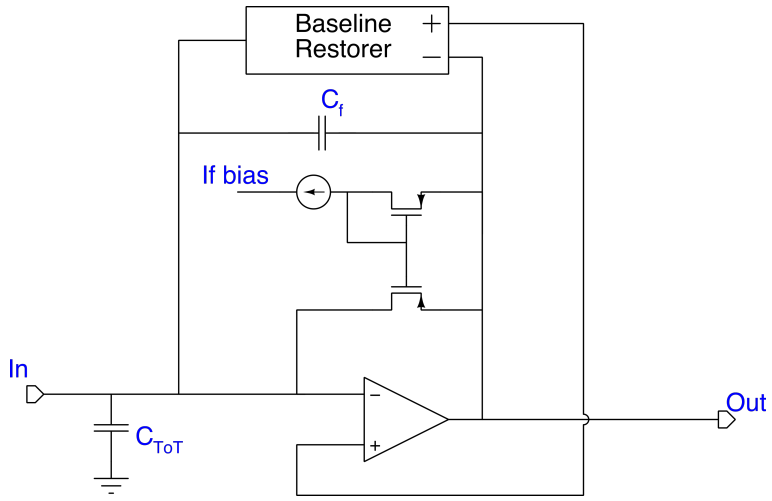


Figure 3.6: ToTamplifier stage made by an amplifier with a high gain with feedback circuits: a constant current generator, a capacitor C_f, and a baseline restorer.

Differential amplifier

The feedback current is generated with a p-mos current mirror instead of a simple resistor because in this way it is possible to fine tune it with a global DAC that varies I_{bias}. This current is delicate since it gives the main contribution to the linearity of the measurement. The core of this stage is a differential amplifier and a common source amplifier, together they create

the ToT amplifier, see Figure 3.6. The choice to have a high gain is due to the requirement to have a good linearity of the ToT measurement. For this reason, it is important that the signals saturate the amplifier as soon as possible in order to reduce the time walk in the comparator. The drawback to having an amplifier saturated is that the virtual ground at the input is not valid anymore. This leads to having an instability on the baseline at the input of this stage. To reduce the voltage swing occurring at the input of the differential amplifier the capacitance C_{ToT} has been included.

Baseline restorer

In order to keep the baseline as stable as possible, the capacitance C_{ToT} is not sufficient. In fact, to increase its value the capacitor size becomes too big. For this reason, it is necessary to use a baseline restorer structure. It is based on a differential amplifier that has as input the output of the amplifier and the nominal baseline value, while the output serves as at the input of the ToT amplifier. The output stage of the baseline restorer is made of two p-mos transistors that have the drain connected together and the gate shorted at their respective source. The first one has the source connected to the differential amplifier inside the baseline restorer and is used to limit its voltage variations. The second one has the source connected to the output stage of the baseline restorer in order, together with an internal capacitor, to have a low pass RC filter. In this way the longest signals can not be clipped avoiding the introduction of non-linearities.

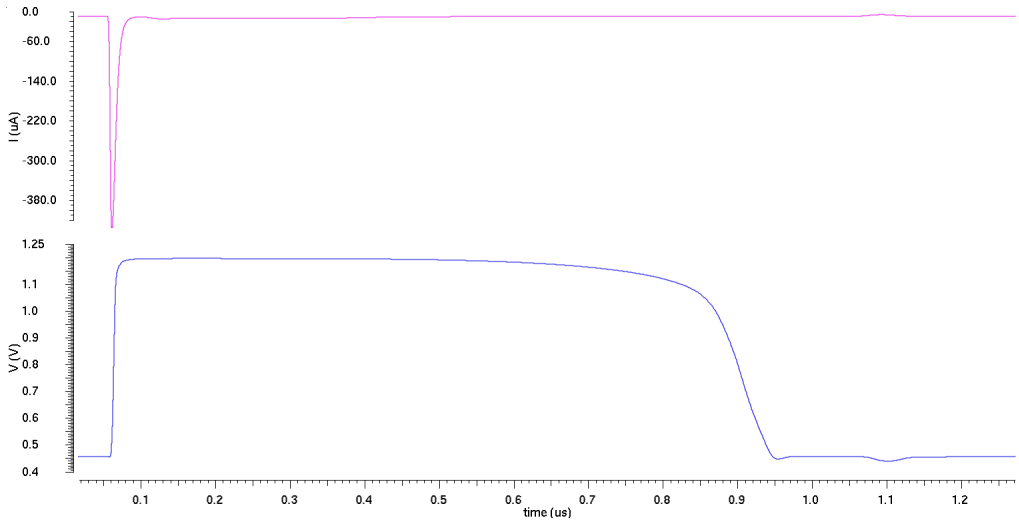


Figure 3.7: The input signal of the ToT amplifier stage is the purple signal while the blue one is the output that has to be processed by the comparators.

In Figure 3.7 in purple the input signal for this stage is shown, in blue the output that has to be evaluated by the comparators. For the channel "0" this output is connected to a source follower which in turn is connected to a pad giving the possibility to observe it on the oscilloscope, for debugging purposes.

3.1.4 Hysteresis comparator

The last structure used in the Front End chain are the two comparators. The architecture used is the same for both, the difference is the value of the applied threshold. As seen in Figure 3.8, the comparator is composed of three stages. The third stage is the one that acts as a comparator, in particular as an hysteresis comparator. This characteristic is given by the cross-coupled transistors $M14$ and $M15$. With this structure the trip point, that is the point when the comparator changes its state, is different if the input signal rises or falls. Figure 3.9 shows the effect of the hysteresis on the output signal. The difference "A" is proportional to the aspect ratio of the cross-coupled transistors. This effect is useful to limiting the multiple firing due to noise. The comparator goes to "1" when the higher threshold is crossed but returns to "0" only if the lower threshold is crossed.

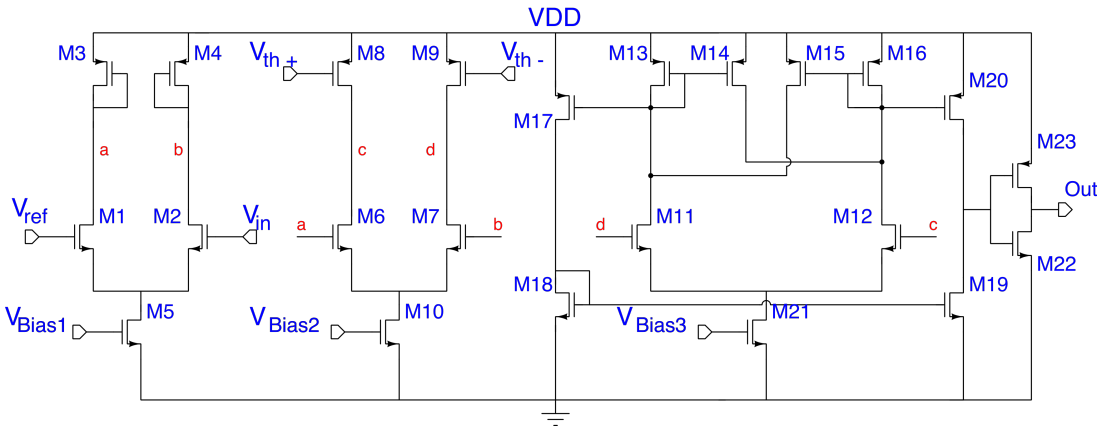


Figure 3.8: Schematic of the hysteresis comparator.

With increasing the voltage on d, lower than the value on c at the beginning of the operations, the trip point is reached only in the following conditions (see Figure 3.9) :

$$\begin{cases} I_{11} = I_{15} \\ I_{12} = I_{16} \end{cases} \tag{3.1}$$

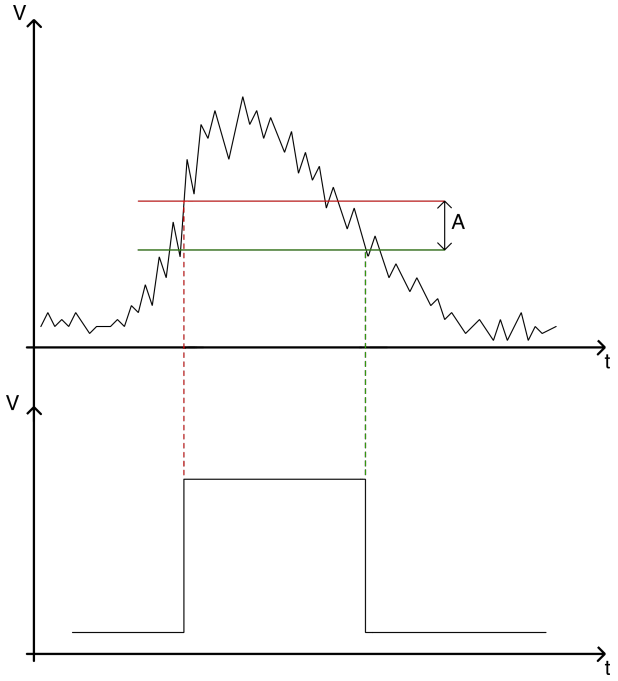


Figure 3.9: The upper graph shows the hypothetical input of the hysteresis comparator, while the lower one is the corresponding output. Notice that, even if the signal crosses every single threshold more than once the output is not effected by multiple firing.

Assuming that the ratio of the dimensions of the transistors $M15$ and $M16$ is J, and equally, on the branch with $M13$ and $M14$, it is possible to write $I_{15} = J\, I_{16} = J\, I_{12}$. Knowing that the entire current for this stage is provided by the transistor $M21$, thus $I_{11} + I_{12} = I_{21}$, it is possible to evaluate the equations 3.1 obtaining:

$$\begin{cases} I_{11} = \frac{J}{1+J}\, I_{21} \\ I_{12} = \frac{1}{1+J}\, I_{21} \end{cases} \tag{3.2}$$

In the opposite case when the voltage value on d is higher than c and it starts to decrease the trip point is:

$$\begin{cases} I_{11} = \frac{1}{1+J}\, I_{21} \\ I_{12} = \frac{J}{1+J}\, I_{21} \end{cases} \tag{3.3}$$

This architecture is particularly helpful with noisy signals, because if the J ratio is tuned properly the multi-firing effect is completely avoided. The comparator, as shown in Figure 3.9, fires only when the signal crosses the red threshold in the rising phase and the green one in the falling phase. The only effect the noise can have in this structure is the variation of the value of

the threshold fed through the comparator. In order to avoid this problem and to be completely insensitive to the noise, the threshold is defined in a differential way. This is the purpose of the second structure made by the transistors $M6$, $M7$, $M8$, $M9$, and $M10$. The effective threshold is given by the difference between Vth_+ and Vth_-. Having a differential threshold, it is necessary to have a differential input signal. Since the input of the hysteresis comparator is the output of the ToT stage, that is single ended, it is necessary to process it. The first stage shown in Figure 3.8 is used, where the input is fed to the transistor $M2$ and a V_{ref}, that corresponds to the baseline voltage of the input signal, on $M1$. In this way, the output of this stage is a differential copy of the signal V_{in} and it is used in the second stage where the differential threshold is applied.

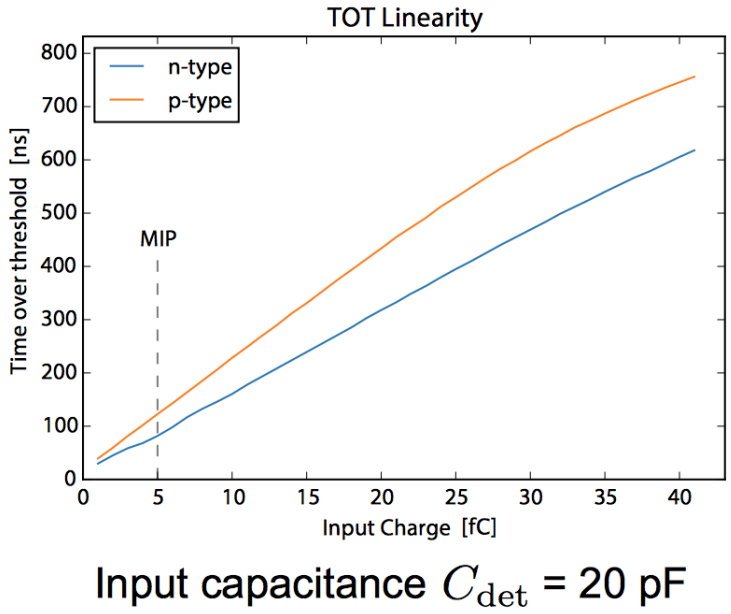


Figure 3.10: Different time duration of the output signal of the Front End chain for different input charge. It shows the expected linearity of the Front End [80].

The two most relevant simulations of the Front End chain are shown in Figure 3.10 and Figure 3.11. In the first one the ToT variation for several input charges is presented. The resulting linearity is pretty good in the minimum ionising particle region for both polarities of the input signal. The second one is the noise expected from this structure that is well below the required maximum ENC of 1000 e^- for a detector capacitance of 25 pF.

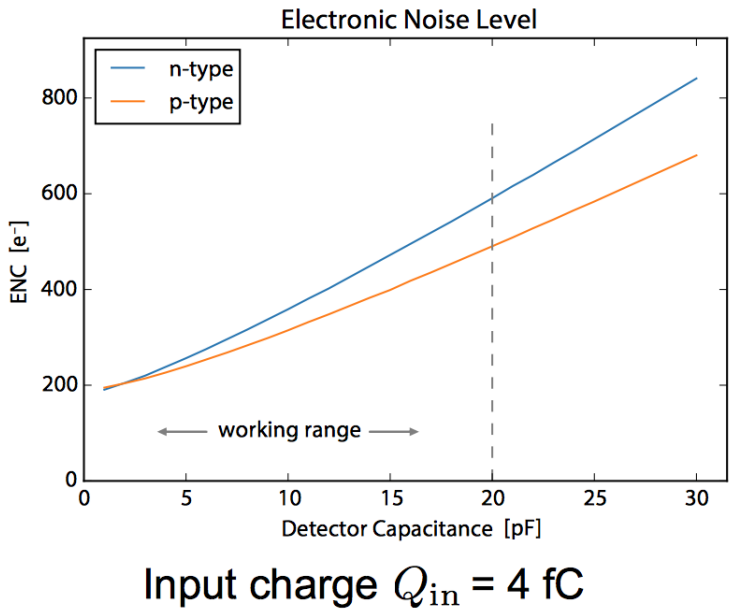


Figure 3.11: Different noise values expressed in terms of ENC for different capacitance with an input charge in the minimum ionising particle region [80].

3.2 Time to Digital Converter

In Chapter 2 is described, along with the reason why a TDC is needed, its working principle. In the next pages, some details about the implementations of each structure of the TDC are reported: Current generator, Time to Amplitude Converter and latched comparator.

3.2.1 Current generator

The purpose of this structure is to generate the two reference currents used both during the discharging and in the recharging processes. These two currents must be as constant as possible when the voltage at the output of the generator changes. Therefore, one important parameter is the output resistance. Another important characteristic is the precision of the ratio between the currents I_{TAC} and I_{TDC} as already mentioned in 2.3.1.2.
There are several possible architectures to design a current generator; it was decided to use the one used in TOFPET [79] as a starting point. The reason that it is a solid structure and the voltage variations at its output are comparable to the variations in PASTA. However, it is necessary to characterise the architecture since the technology used for PASTA is different to the one used for TOFPET.

The architecture is based on current mirrors. In the reference branch flows a certain current that is replicated on others branches. The value of the copied current depends on the ratio between the dimension of the transistors in the reference branch and the one in the evaluated branch. Since it is important to achieve a high output resistance, it has been chosen to implement not a simple current mirror but a double cascoded one. In order to have a better matching between the two currents, only one structure is used to generate them. The complete architecture is shown in Figure 3.12.

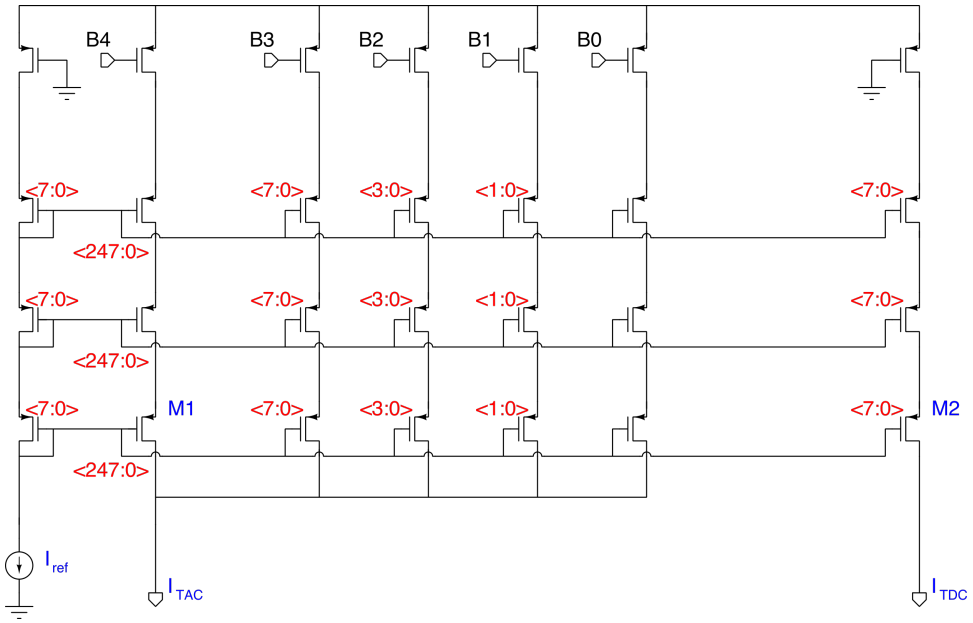


Figure 3.12: Schematic of a double cascoded current source with three branches: reference branch, I_{TAC} branch and I_{TDC} branch. The structure in the middle is a DAC used to tune the current I_{TAC}.

The branch on the far left, with the transistor diode-connected, is used as a reference; the current I_{ref} is sinking from the transistor $M1$. For simplicity, the recharging current, that is the smaller one, is equal to I_{ref}. Using this solution the current I_{TDC} can be copied leading to having the same size for the transistors that generate it. The expected current for this branch is 500 nA. For the discharging current, the structure is a bit different, being composed of the main branch and other four branches that form a DAC. The main branch generates a current of 15 μA since the ratio between the transistors is 31; with the DAC it is possible to adjust the current in order to achieve the needed ratio 32. The introduction of the DAC is helpful also because it is possible to tune the current during the test phase.

The first analysis to be performed is the verification of the generated current; which must stay at the nominal value during the TDC process. During the discharging phase, the voltage at the output of the transistor $M1$ can vary in the expected operation range from 300 mV to 600 mV. This variation is due to the discharging of the capacitor C_{TAC}. The values of the I_{TAC}, given by the simulations, in the range of study are shown as blue points in Figure 3.13.

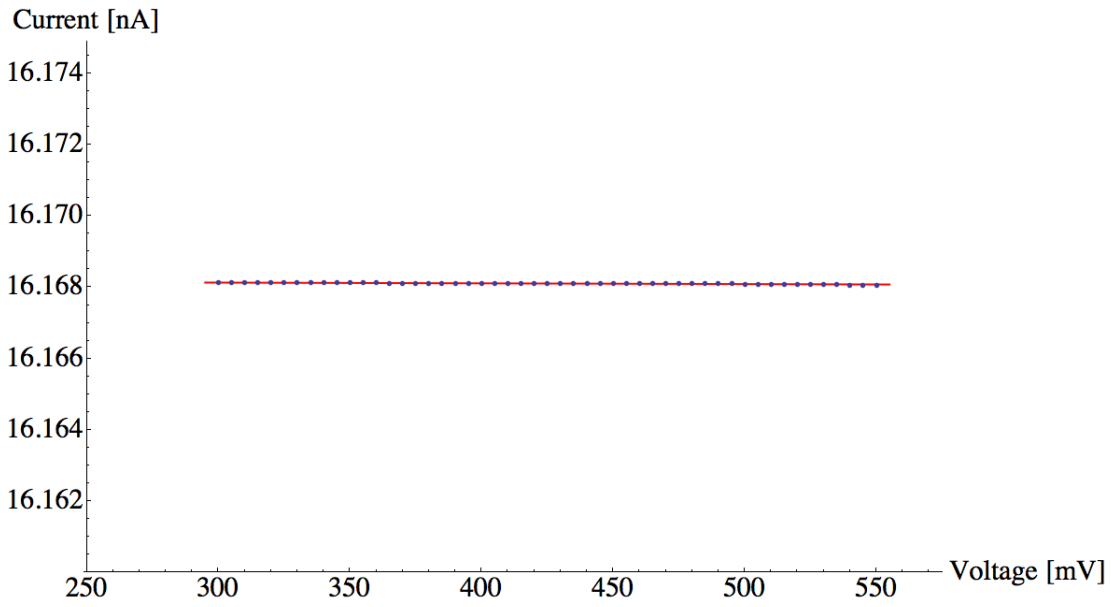


Figure 3.13: In blue the I_{TAC} current values for several voltage values are shown. The voltage range is the expected working region of the I_{TAC} branch. The red line is the best fit for the points.

Since, as already mentioned, the results shown in this chapter come from simulations and not measurements, they have no errors. Therefore, it is not possible to estimate the χ^2 for the plots but only the deviation of the points form the fit. The maximum deviation is given by Formula 3.4 and is equal to 0.00012‰. I_f represent the current given by the fit while the I_s is the data from the simulation.

$$Deviation = Max\left[\left|\frac{(I_f)_i - (I_s)_i}{(I_f)_i}\right|\right] \tag{3.4}$$

The red line is given by $I = 16.1683 - 3.72877\,10^{-7}\,V$; from the inversion of the b coefficient of the fit it is possible to calculate the output resistance. Taking into account that the current is expressed in μA and the voltage in mV the output resistance of the discharging phase becomes:

$$Rout_d = \frac{1}{b} \cdot 10^3 = 2.68\,G\Omega \tag{3.5}$$

The second scan performed is the voltage variation on the output of $M2$ where the current I_{TDC} is generated. In this case, to simulate the recharging phase conditions, the voltage range varies from 250mV, that is the minimum expected from simulations, to 850 mV, that is the value of the threshold of the latched comparator in Figure 2.10. The resulting variation of I_{TDC} in this voltage range is reported in Figure 3.14.

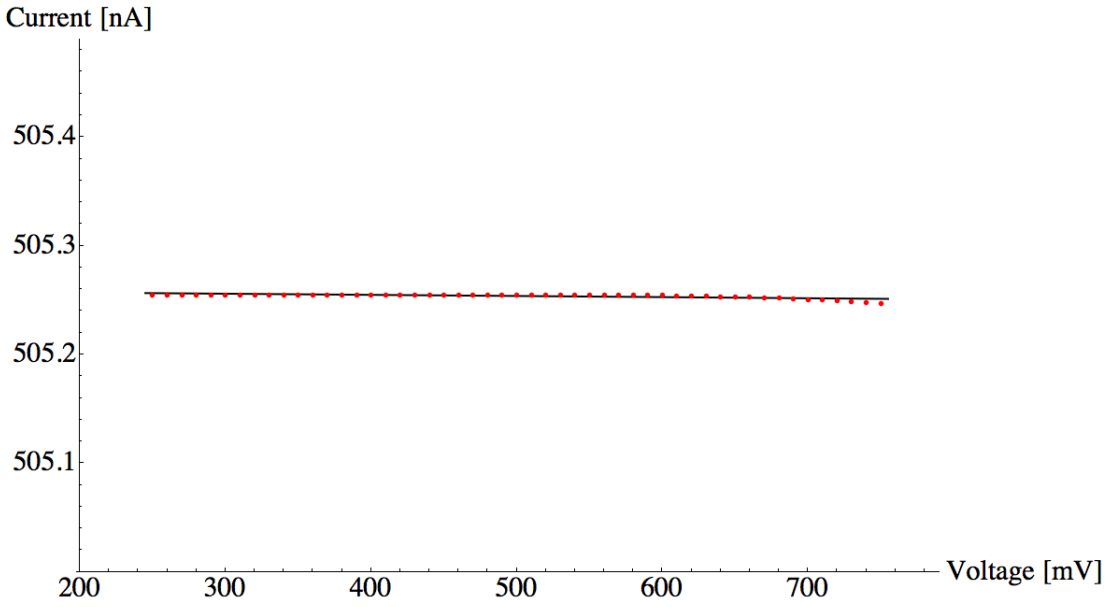


Figure 3.14: The different values of I_{TDC}, in the working region of its branch, are represented by blue dots. The best fit to the points is shown in red

In this case, the maximum deviation from the points to the fit is 0.0957‰. The formula for the red line is $I = 505.273 - 4.16774\,10^{-5}\,V$: taking into account that in this case the current is evaluated in nA the resulting output resistance for the recharging phase is:

$$Rout_r = \frac{1}{b} \cdot 10^6 = 23.99\,G\Omega \tag{3.6}$$

The last analysis to perform is the verification of the ratio between the current I_{TAC} and I_{TDC}. One important thing to keep in mind is that there are several parameters that can be different for each transistor due to the process variations during the production of the chip into the silicon wafer. All these variations of the parameters lead to a slightly different behaviour of the transistor and thus to a different generated current. It is possible to simulate these variations via a Monte Carlo simulations. With this kind of simulations it is possible to check which is the foreseen current distribution and thus which is the expected ratio. The result for an analysis of 1000 points is shown in Figure 3.15.

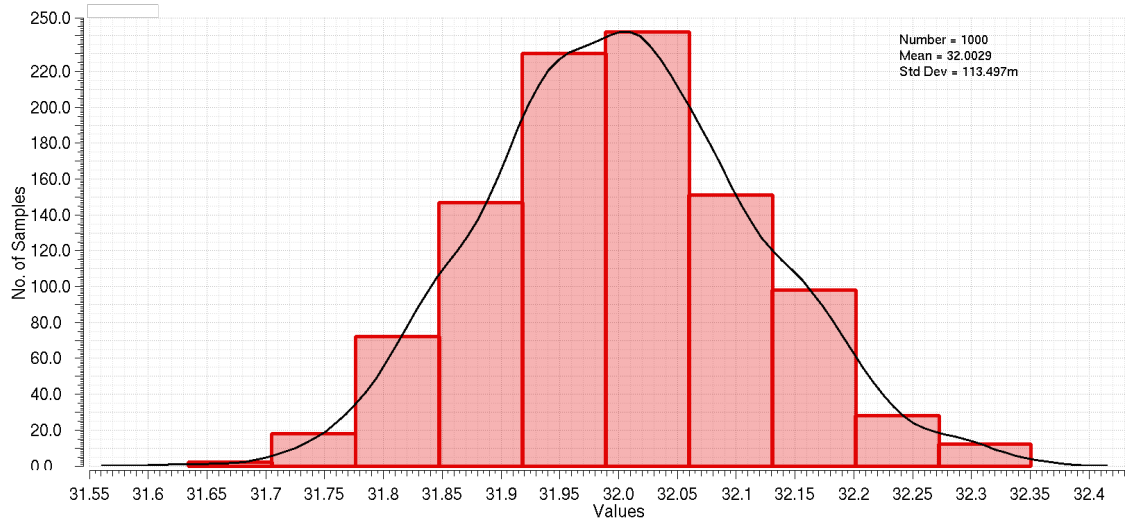


Figure 3.15: Distribution of the ratio of the current I_{TAC}/I_{TDC} due to the process variations.

The performance of this structure is satisfactory, as can be seen from the previous results, the only problem is the DAC. In fact, the DAC used for the current I_{TAC} is a parallel of several currents mirrors. The LSB is made with a branch that has a current 8 times smaller than I_{ref}. The number of transistors needed has grown rapidly, as shown in Figure 3.12, since the reference current branch is already a parallel of 8 single branch. The space needed by this current source structure exceeds there a constraint for PASTA, it can, however, be used as a base to build a smaller one.

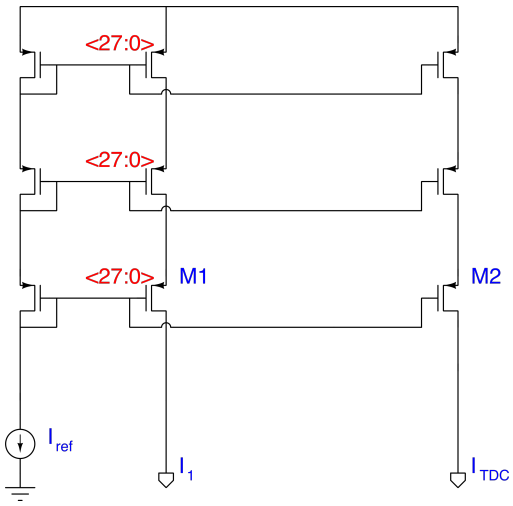


Figure 3.16: Schematic of the new current source based on the old structure.

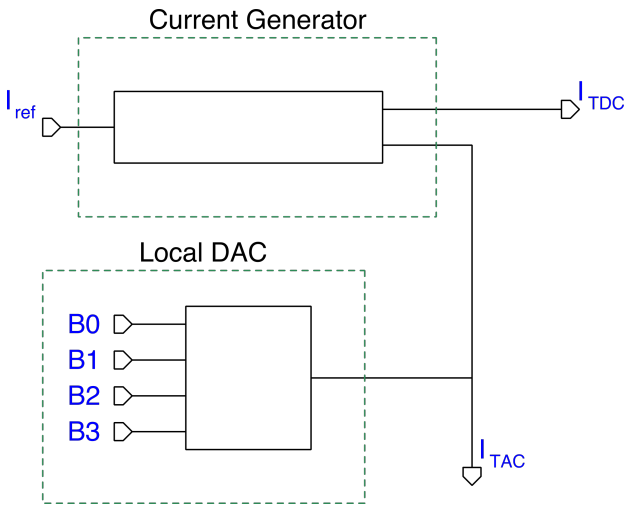


Figure 3.17: Structure needed to have the ratio 32 between the two currents and to tune the current I_{TAC}.

The structure implemented is based on a triple cascoded technique but this time a main branch that is 28 times the reference one is used to generate the current I_{TAC}. A DAC that has a specific reference current is used to achieve the ratio 32. In this way, the number of transistors needed decreases significantly, reducing the area needed by the structure. The design of the current generator is reported in Figure 3.16 while the complete structure used to achieve the needed current I_{TAC} is shown in Figure 3.17.
For this structure the same analysis as for the previous one is performed. It is necessary to understand if the output resistance of the new current source can be considered high, too. The voltage variation range for the current I_{TAC} is again from 300 mV to 600 mV since the working range of the TAC is always the same, the current trend is shown in Figure 3.18. Also in this case it is possible to assert that the data follows a linear trend, the maximum deviation is 0.00019‰. The best fit of the data has the analytic formula $I = 16.1457 - 7.53286\,10^{-7}V$, as for the previous current generator the b factor needs to be inverted and multiplied by a factor that takes into account the value of the current and voltage.

$$Rout_d = \frac{1}{b} \cdot 10^3 = 1.32\,G\Omega \tag{3.7}$$

In the same way, the analysis for the recharge current for a range between 250 mV and 850 mV is performed.

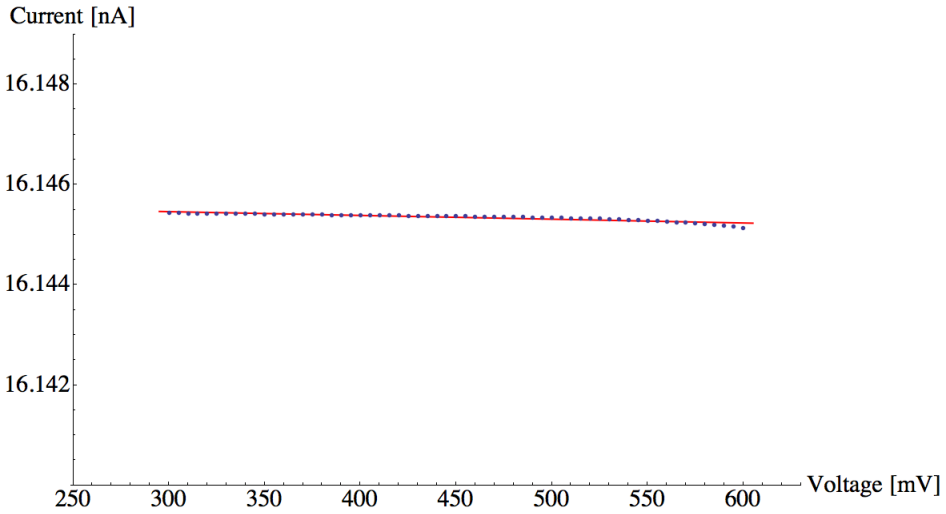


Figure 3.18: Trend current I_{TAC} (blue points) in the expected working region for the new current source.

The trend shown in Figure 3.19 is linear, even if, for the high voltage values the structure starts to deviate from the linearity. The maximum deviation of the points is 0.4302‰. The red line of the fit is represented by the formula $I = 505.104 - 2.13506\,10^{-4}V$. The output resistance in this case is:

$$Rout_r = \frac{1}{b} \cdot 10^6 = 4.684\,G\Omega \tag{3.8}$$

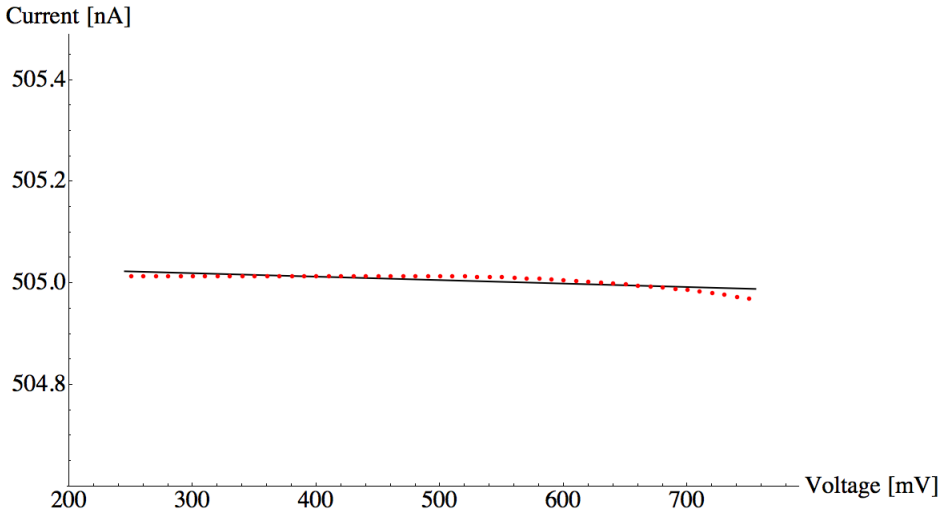


Figure 3.19: Best fit of the I_{TDC} current.

The last simulation that has to be performed is the Monte Carlo simulation. Since the area is significantly smaller than the previous structure, and the mismatch of the currents depends on the square root of the transistors' area, a bigger spread of the currents ratio is expected. Indeed, Figure 3.20 shows that the sigma is bigger with respect to the previous one. At this point, since in the extreme cases the ratio is 28.40 and 36.6, it is important to understand if, using the DAC, it is possible to tune the ratio in order to achieve a value close to 32. The DAC has four bits and the value of its LSB is 300 nA. In this way, in the default configuration, the current source provides around 14 μA while the remaining 2 μA are generated by the DAC. The simulations, shown that in the case of ratio 36.6 it is possible to achieve a ratio equal to 32.40 with a configuration word of the DAC of "0001". In the opposite case with a configuration word of "1110" it is possible to reach a ratio of 32.04.

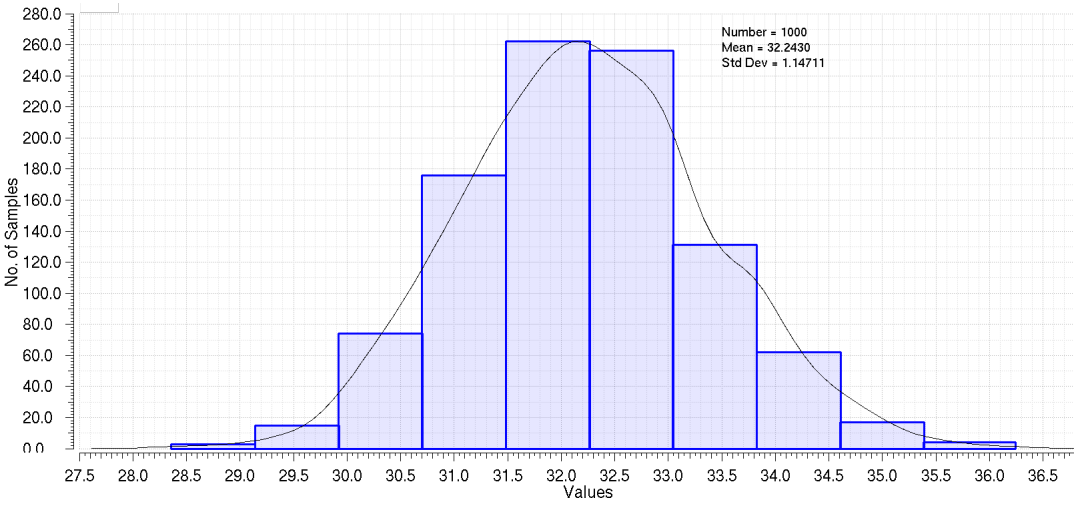


Figure 3.20: Distribution of the ratio of the currents I_{TAC}/I_{TDC} for the new current source.

3.2.2 Time to amplitude converter

This architecture consists of a high gain amplifier and a feedback capacitor. The main purpose of the TAC is, as the name suggests, the translation of information from a time domain into voltage domain. In particular, for the PASTA chip, it is used during the process of measuring the fine time. As mentioned in section 2.3.1.2, the current I_{TAC} discharges the feedback capacitor C_{TAC}. Due to a constant current and to the TAC the voltage value reached by the capacitor is proportional to the time that the current is connected to the amplifier. Therefore, is important to have a good linearity in terms of voltage reached for different times. The second important

parameter is the time, called dead time, that the amplifier needs to reach the starting conditions after a reset signal. The reset signal is necessary to clean the charge information stored in the capacitor C_{TAC}, in order to be able to store new data. The signal must be sent when the sharing phase with the capacitor C_{TDC} is ended, in order to avoid the loss of information.
During the designing phase several architectures have been studied, in the next few pages the two most significant structure are described. The first amplifier is shown in Figure 3.21, a folded cascode amplifier. The current is injected on the gate $M1$ that has its source connected to a voltage value lower than the power supply. The second switch of this structure is used to reset the capacitor C_{TAC}.

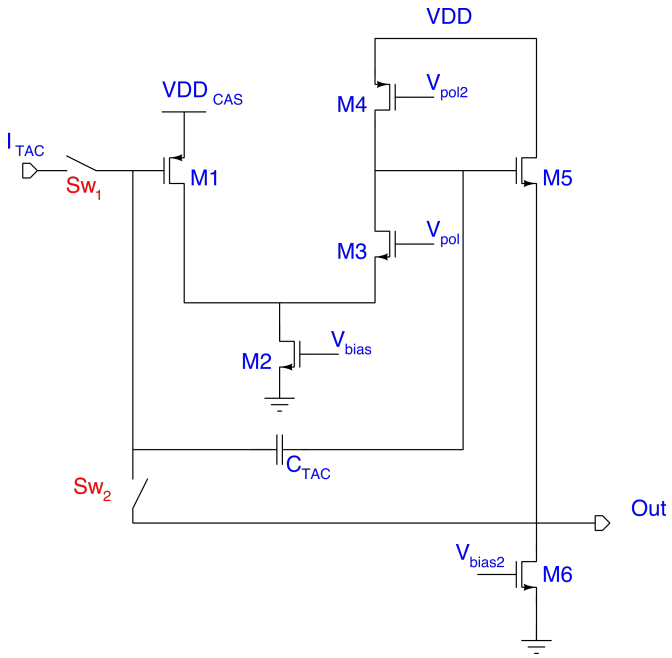


Figure 3.21: Schematic of a folded cascoded amplifier.

In order to understand the behaviour of this structure in terms of linearity, the voltage value at the output of the amplifier is measured for several durations of switch "1" closure. In particular, since the local controller features a range between 0.5 clock cycles and 1.5 clock cycles, the simulation is performed for switch closure times from 3 ns to 10 ns. In Figure 3.22 the voltage output reached for a specific time is shown with blue dots, while the red line is the best linear fit to the simulated points. It is important to highlight that the points are not affected by any errors because they are results from simulations. At this point, it is important to understand the deviation of the blue points from the linear fit. Equation 3.9 is applied for this purpose, where V_f is the voltage value given by the red line and V_s is the voltage value form the simulations.

$$Deviation_i = \left| \frac{(V_f)_i - (V_s)_i}{(V_f)_i} \right| \tag{3.9}$$

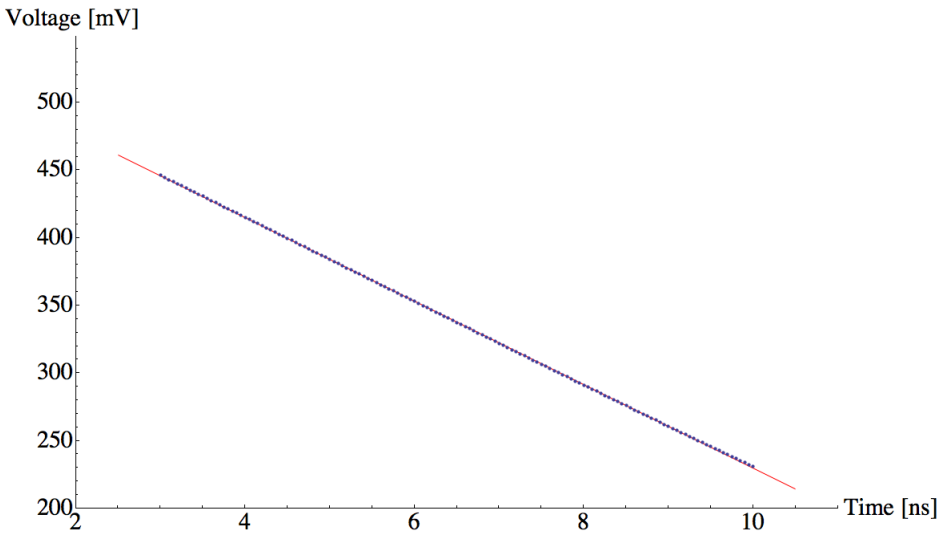


Figure 3.22: Voltage values reached by the folded cascode amplifier for different times (simulations, blue) and best fit to the points (red).

Analysis of this data shows that the maximum deviation of the points from the fit is 4.53‰. With this result it can be asserted that the architecture under study has a linear response in the time range studied. Since that the structure has the desired behaviour, the next step is to understand which are the errors committed. First of all, it is necessary to calculate the times that correspond to the voltage values given by the red line using Equation 3.10. In this equation V_b is the base line of the amplifier, V_C is the voltage given by the best-fit line at a specific time and A is the intercept of the line.

$$T_C = \frac{C_{TAC}}{I_{TAC}}(V_b - V_C - A) \tag{3.10}$$

The difference between the calculated time T_C and the effective time that the switch is closed gives the error for each time. Figure 3.23 shows the time error versus the effective time. There is a minimum value of 53 ps that can be considered as an offset while the maximum error is 114 ps. The violet curve corresponds to a third order polynomial that can be used to correct the times offline.

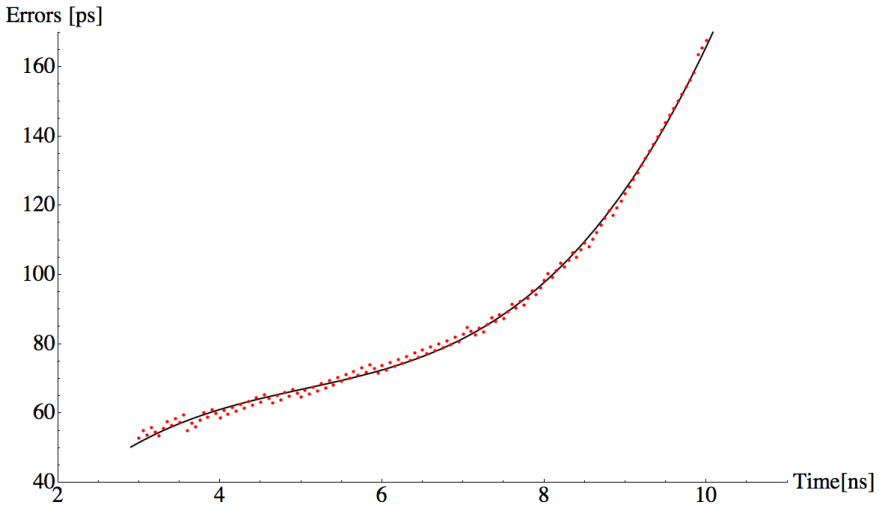


Figure 3.23: Deviation of the times produced by TAC form the fit.

The results from this structure show a good behaviour in terms of linearity. Moreover, it is possible to correct deviations through an offline calibration since they have a specific trend. The last point to check is the time that the amplifier needs to come back to the starting point after a reset signal. This is done by simulating the complete process of discharging phase, sharing phase, and reset operation. Figure 3.24 shows the voltage value at the output of the amplifier during the entire process.

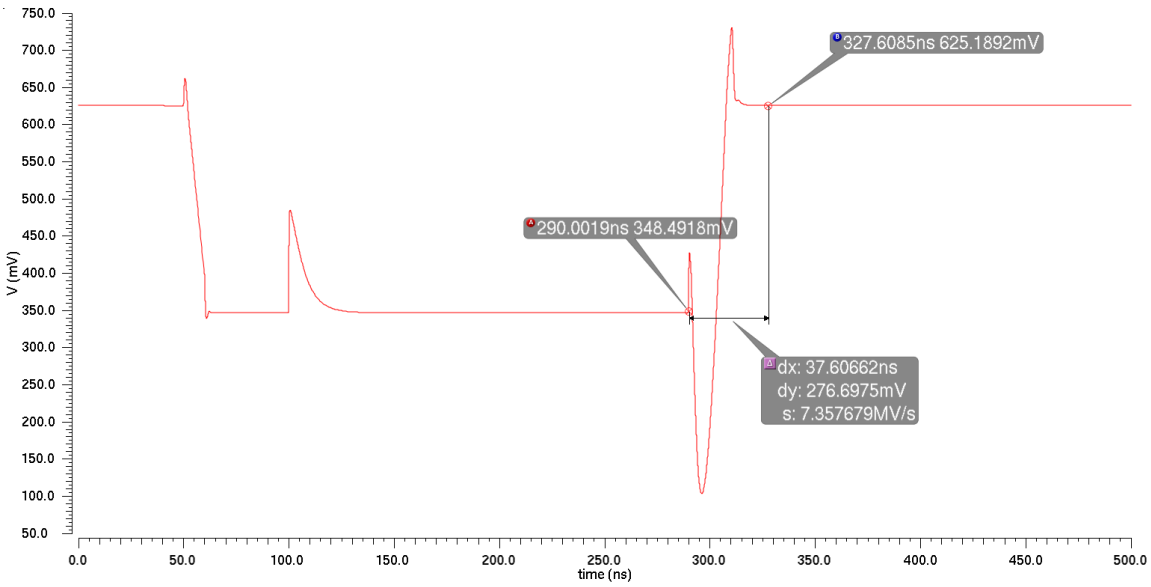


Figure 3.24: Complete process for the folded cascode amplifier.

At the beginning, the voltage value is fixed to the baseline at 625 mV then after 50 ns the discharging process starts, the duration of the discharging phase is 10ns. The voltage value is held until 100 ns when it is shared with the capacitor C_{TDC}. The last step is the reset operation of the capacitor C_{TAC} that starts at 290 ns and ends at 328 ns.
The second architecture is the one shown in Figure 3.25. In this structure, the current is injected into the transistor $M1$ that is the input transistor of a simple common source amplifier. Unlike the previous case, in this architecture a series of switches is needed to reset the voltage on the capacitor C_{TAC} that is represented by the transistors $M5$ to $M8$.

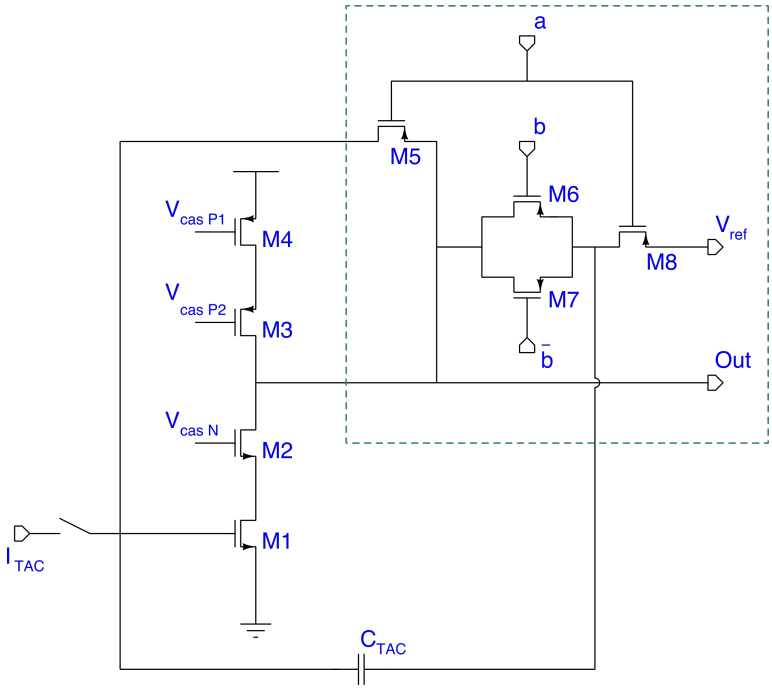


Figure 3.25: Schematic of cascoded amplifier.

Also for the cascoded amplifier, the analysis is performed in order to verify the linearity of the voltage values versus time as shown in Figure 3.26. In this case, the voltage values are different because the baseline voltage value is 845 mV, so the maximum voltage reached is different from the previous architecture. As before the red line represents the best fit to the data and using equation 3.9 the maximum deviation is 0.5‰.

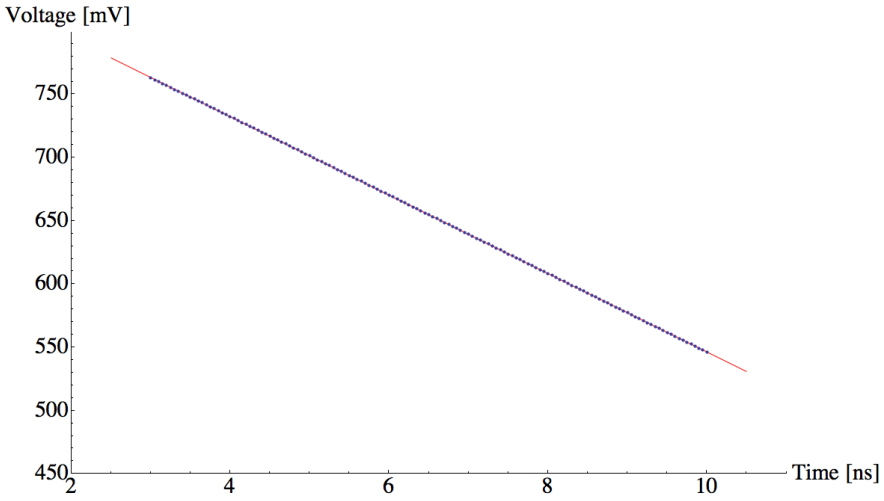


Figure 3.26: Different voltage value reached by the cascode amplifier for different duration of the discharging phase.

The procedure to define the error in time in this architecture follows the same steps used for the previous structure. It is important to take into account that V_b in the Formula 3.10 is now different from the previous architecture. The analysis shows that in this case there is an offset of 127 ps and the maximum error is 256 ps. Even if this value is bigger compared to the folded cascode architecture it is not a problem because, as shown in Figure 3.27, the best fit for these points is a straight line. That means that it is easier to apply the corrections.

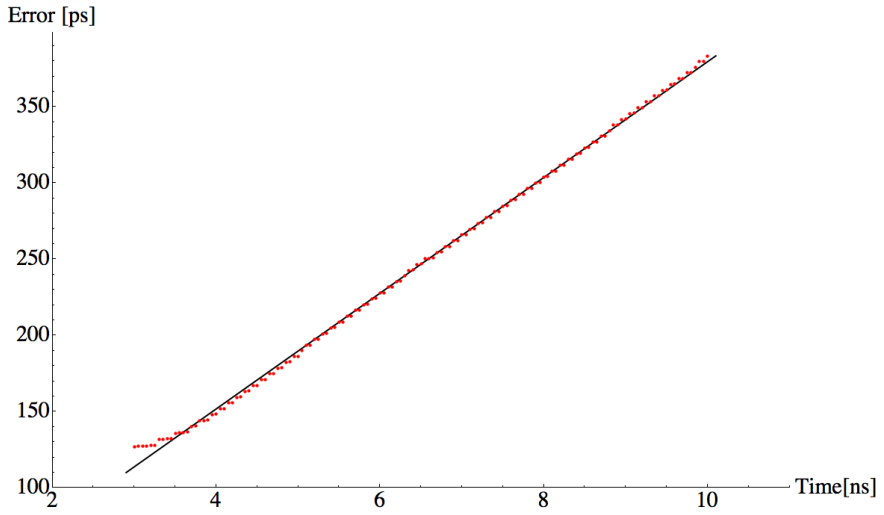


Figure 3.27: Trend of the deviation of time form the fit.

The last behaviour to verify is the reset time. The complete process for the cascoded amplifier is shown in Figure 3.28. The reset of the capacitor C_{TAC} is done in about 20 ns, this is quite a remarkable result because it is half of the time required by the folded cascoded architecture.

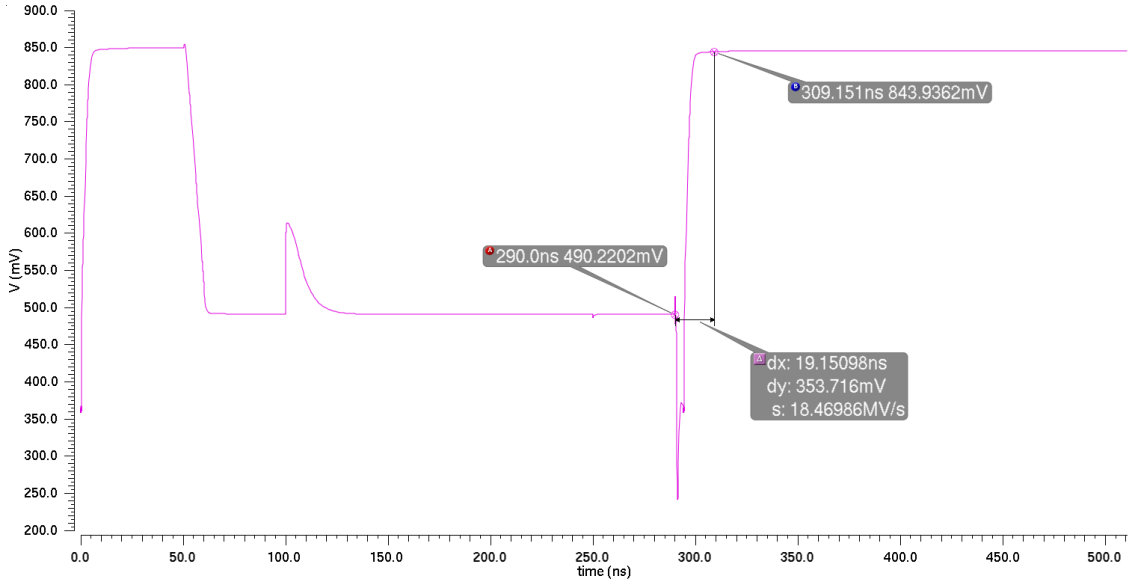


Figure 3.28: Complete process for the cascode amplifier.

In summary, the most important parameters to design a TAC are the linearity of the structure and the time needed to reset the capacitor C_{TAC}. The first parameter is important because it is mandatory to have a precise and clear voltage response for a specific time. A small reset time results in a smaller dead time. This leads, as shown in 2.5, to a smaller number of TACs needed to keep the probability to lose and event below 1 ‰. Since it is important to use as little area as possible, the reset time plays an important role in the structure choice. According to these results the second architecture is more suitable for the project under development (Figure 3.25).

3.2.3 Latched comparator

The third building block is a Wilkinson ADC that is composed of three parts: the recharging current I_{TDC} coming from the current generator, the capacitor C_{TDC} and the latched comparator. The task of this building block is to measure the recharging time that is 128 times bigger than the discharging one. Basically it is possible to connect a counter that counts how many clock cycles elapse between the start and the end of the conversion. This solution was discarded because it introduces a lot of noise and it consumes too much area, so it has been decided to

store the SOC and the EOC separately. The SOC begins with a digital signal coming from the local controller, while EOC is triggered by the latched comparator when the voltage value on C_{TDC} reaches the reference voltage (V_{ref}) applied to the comparator.

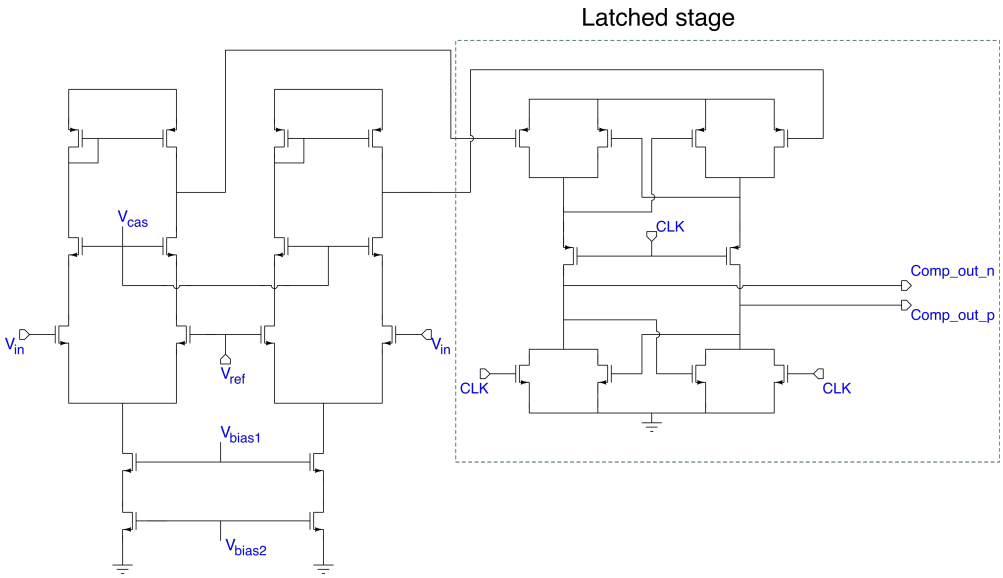


Figure 3.29: Schematic of the latched comparator.

The latched comparator (Figure 3.29) consists of two stages, the first one is a differential amplifier while the second stage is a latch based on positive feedback operating at the clock frequency. The advantage to using a latched comparator with respect to a continuous one is that a differential amplifier with a high gain is not needed because the latch stage changes the outputs drastically given only a small input variation. Figure 3.30 shows the two outputs of the comparator. The red one is the *comparator output p* (positive output) while the blue one is the *comparator output n* (negative output). When the input voltage value is lower than the set threshold the *output p* is fixed to "0" while the *output n* follows the clock.
As soon as the input signal crosses the threshold the output signals are swapped. To drive the digital part only one of these two outputs is used. In particular, it is the *output p*, because the other one introduces too much power consumption and noise since it flips from the powering of the channel to the end of conversion. In order to further reduce the possible instability and the noise a particular trick is employed: the clock is not always sent to the latched comparator but only during the third phase of the TDC operation.

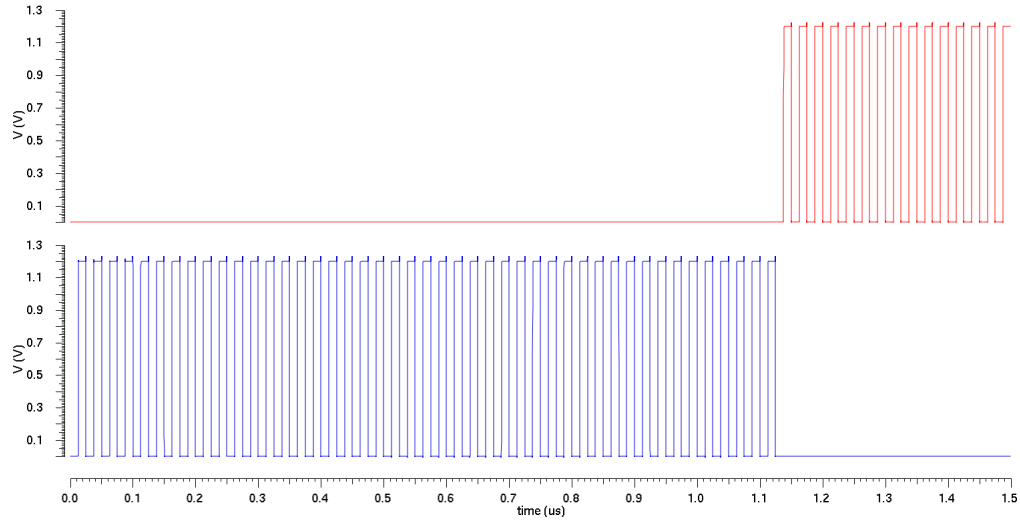


Figure 3.30: Output of the latched comparator (red the positive one, blue the negative one).

This phase starts with the SOC meaning that it is possible to use this signal to activate the clock in the structure. In Figure 3.31 it is shown how the *comparator output n* is fixed at the voltage power supply at the beginning. For the *comparator output p* the procedure is a bit different. When the latched comparator fires, a signal EOC is generated. This signal is used to turn of the clock in the structure. The *comparator output p*, that should follows the clock, in these conditions is maintained at "1". In this way, the comparator architecture is much more stable and doesn't introduce noise generated by these variations in the nearby analog architectures in the same channel.

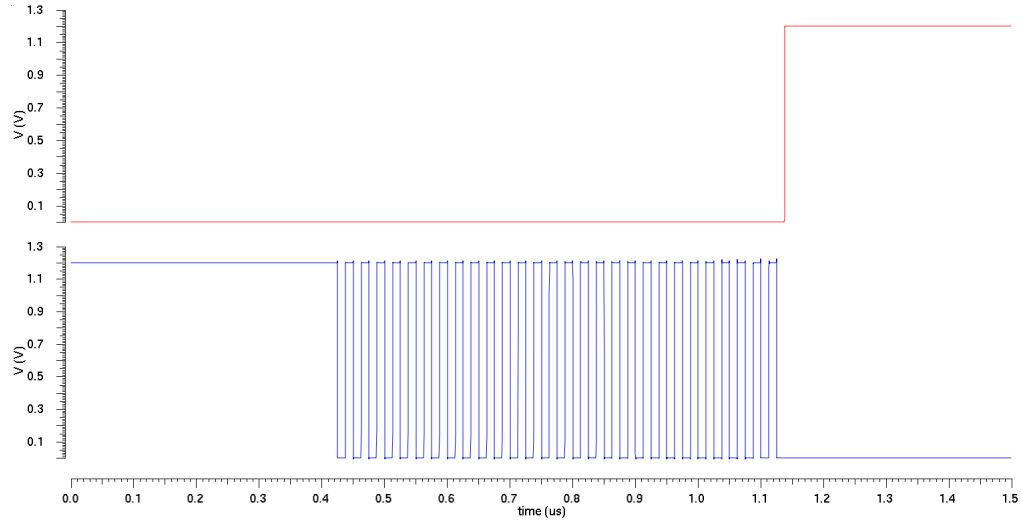


Figure 3.31: Output of the latched comparator using a selective clock.

3.3 Channel test

In order to understand if the TDC works properly it is necessary to perform mixed simulations with both the TDC and the local controller. This is the most important test for the entire channel because the addition of the Front-End doesn't add much information. It doesn't have a lot of interaction with the local controller and doesn't have interactions at all with the TDC. Therefore it can be replaced with an ideal voltage generator to perform the following simulations. The purpose of this test is to verify that the channel logic is able to drive the TDC as programmed and that the analog part reacts as expected from the local controller.

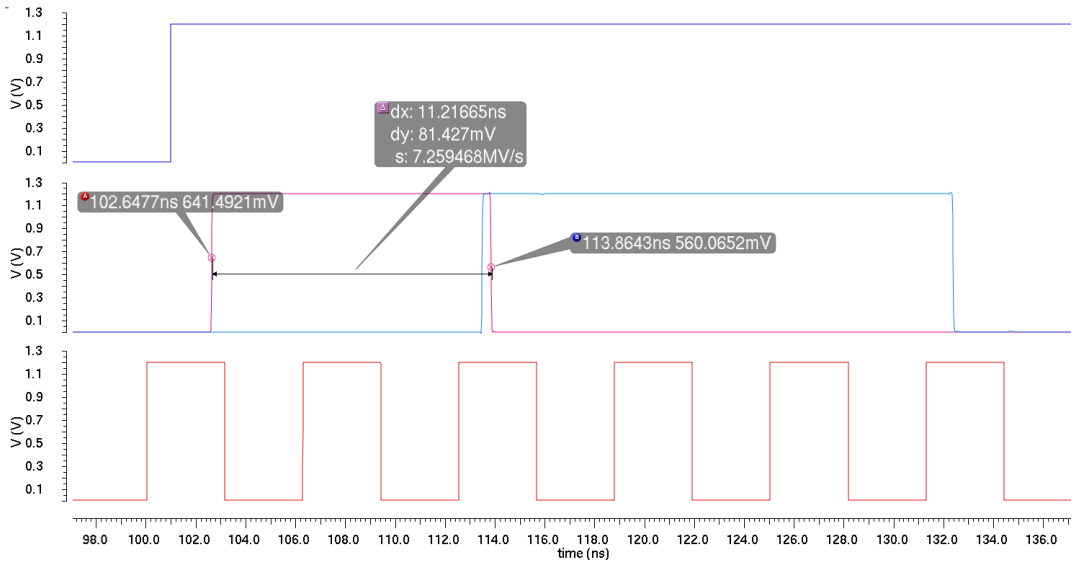


Figure 3.32: Combined simulation of both the local controller and the TDC. The blue signal in the first graph is the DOT, in the second graph the light blue represents the coarse time, the magenta signal is the fine time while the third graph shows the main clock.

A digital signal that simulates the DOT (coming out from the Front-End) is sent to the local controller and is shown in blue in Figure 3.32. The digital part has the task, as mentioned in 2.2, to store the coarse time that is a time stamp corresponding to a leading edge of the clock (light blue signal) and to define a fine time (magenta line). The fine time should start with the leading edge of the DOT and end with the leading edge of the coarse time but, due to logic processing, there is a short delay. However, the processing time that leads to this delay is the same for all

the cases so it is an offset that, once taken into account, doesn't change the performance of the channel. In this case, the fine time corresponds to 11.217 ns. At this point, the control logic guides the TDC through the different phases; the most interesting is the third one that is the recharging process reported in Figure 3.33. The first graph is a zoom out of the previous figure while in the second shows the voltage value on C_{TDC} (red signal) and the *comparator output p* (blue signal). The analog part is managed by the signals in the third graph, the SOC (magenta) and EOC (green signal). It can be seen that the measurement of the fine time trough the TDC works properly. Moreover, it is also possible to verify which is the real multiplication factor introduced by the currents and the capacitors:

$$Ratio = \frac{1.435\,\mu s}{11.217\,ns} = 127.93 \tag{3.11}$$

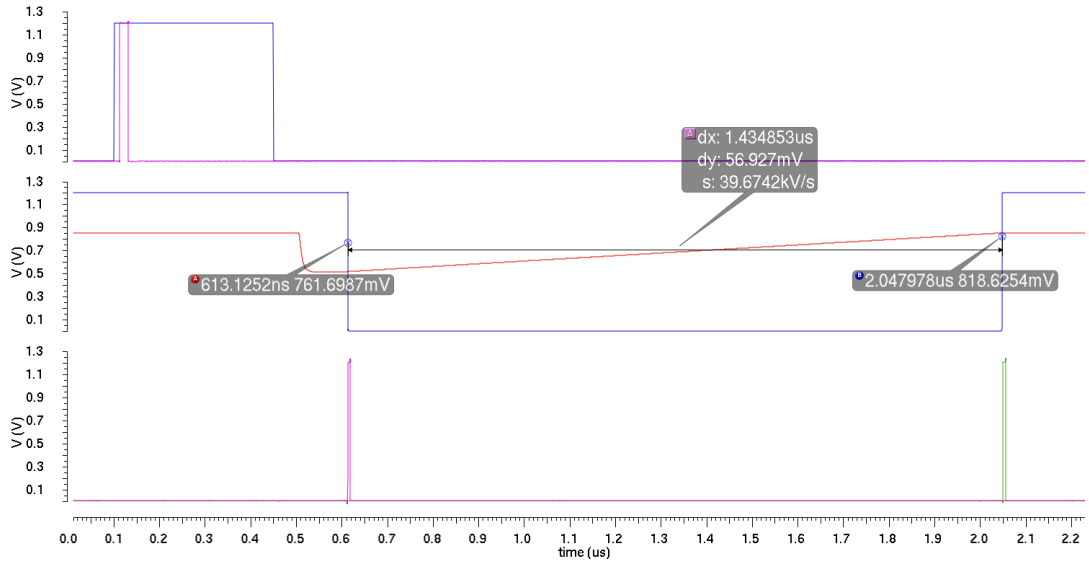


Figure 3.33: The first graph shows the DOT and the coarse time. In the second graph there is the voltage value on the capacitor C_{TDC} in red while the blue signal is the output of the latched comparator. In the third graph the digital signal SOC can be seen in magenta and the EOC in green.

To complete the study it is necessary to verify that also the second TDC, the one that measures the time of the DOE, works properly. This is important not only for the verification that everything is similar in both branches but also to understand if the local controller is able to validate the event. To do so both branches are needed. In Figure 3.34 the entire process is reported: in the first graph, there is the DOE in blue and the fine time in fuchsia. It is important to

notice that the fine time is correctly on the falling edge of the DOE. The second graph is similar to the one in Figure 3.33 while the third one shows all the signals needed for the conversion:

- magenta: SOC (unique for both branches)
- green: EOC (time branch)
- orange: EOC (energy branch)
- red: valid even

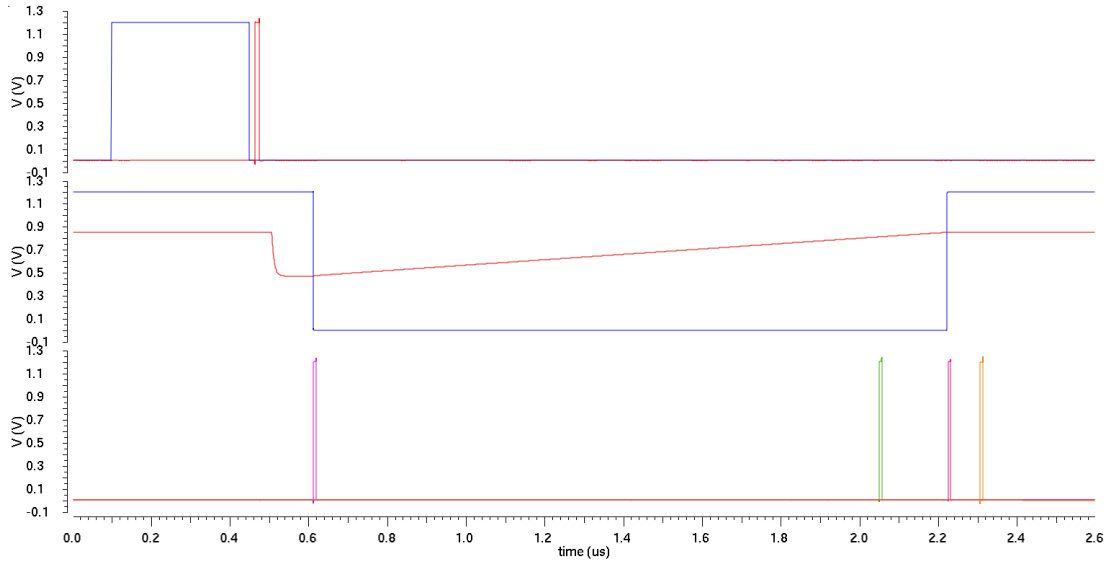


Figure 3.34: Relevant signals for the energy branch. For the definitions of the colours see the text

4

PASTA LAYOUT

This chapter is dedicated to the description of the layout of the chip, starting from an overview of the basic concepts of layout to the final assembly of the full ASIC. In the analog environment everything is custom and, unlike the digital layout, it is not possible to have any automatisation, neither for the placing of the transistors nor for the routing between them.

4.1 General considerations

The layout process is based on the photolithography, it starts from a wafer of silicon where, first of all, the polysilicon that defines the gates is placed. Then all the regions with different doping levels are created with specific masks. After that, the foundry starts to place several metals from the metal 1, which is the closest to the silicon layer, to the upper one. The number of metal layers available changes from technology to technology. The metals are separated with a layer of insulating material, the connections between two metal layers are done with holes in the insulating material that are filled with a conductor. These connections are called vias and are foreseen by the designers.
In modern technologies, one of the most important bottlenecks for the chip performance in terms of speed and precision is the layout, in particular unwanted interaction between different sections or nonidealities in the layout and packaging. From the layout design the foundry creates the masks used during the fabrication process. It is thus important to well define all the areas for each component and each connection used in the design [84]. Figure 4.1 shows how a p-mos transistor from the layout point of view. As can be seen from this figure, it is necessary to adopt a few precautions for a correct design. First of all it is important that the well, the n-well in this case, that contains the device, is bigger than the device itself in order to be sure that the transistor is always surrounded by this region considering all the possible misalignments during fabrication. A similar solution must be adopted also for the active area that physically constitutes the drain and the source of the transistor. These are just two examples of things

that must be taken into account to design a single transistor. However, in most of the cases the complete layout of a single transistor is already implemented into the design tools according to the technology used.

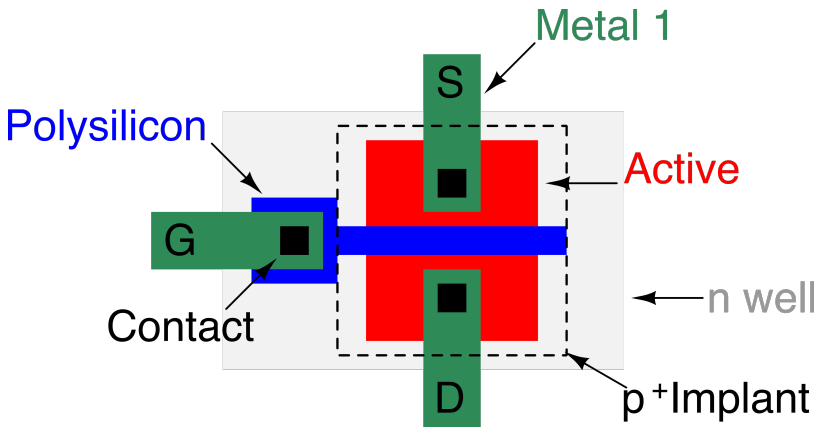


Figure 4.1: Layout of a p-mos transistor.

Even if the dimensions of the transistors have been decided during the schematic design, they must follow certain rules in order to be sure that the simulated behaviour is maintained on silicon. It is also important to follow these rules for all the components and connections because the nominal values, during the fabrication process, are affected by some variations. It is possible to define five groups: minimum enclosure, minimum spacing, minimum extension, minimum width, maximum area.

Minimum enclosure

With this group of rules the minimum space that has to surround a certain region is defined. For example, in Figure 4.1 the p^+ implant region is bigger than the active one. This kind of problem can be extended also to the connections. If they are done without respecting the minimum enclosure, there is the possibility that, during the process, the connection region is much smaller than the one foreseen. This leads to a higher parasitic resistance between two lines, or even worse, the connection is not made at all.

Minimum spacing

All the regions created during the fabrication process, from the implant region to the metal line, are done with a lithography process through masks. Using this kind of process it is not possible to obtain a clean edge. For this reason, one must leave a minimum space between the

metal lines, to avoid undesired shorts, or between the different regions, in order to preserve the previous rule.

Minimum extension

Since the dimension of the transistors is optimised for every specific architecture, it is important that every point of the transistor works properly. In some geometries it is necessary to extend lines or regions beyond the edge of others, in order to be sure that also the edge works properly. One example is shown in Figure 4.2, where the polysilicon line must by longer than the active area.

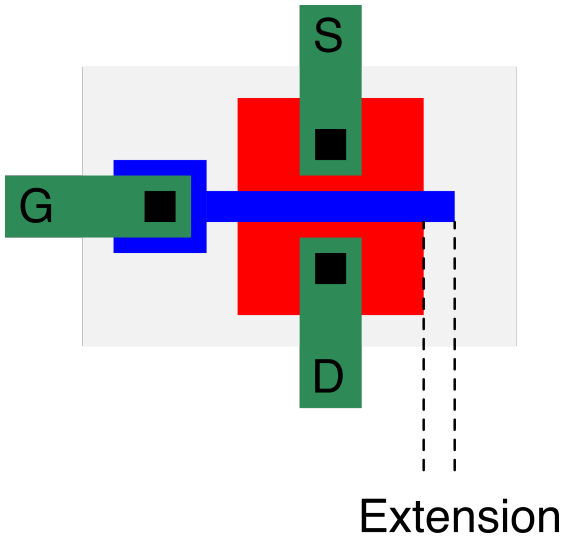


Figure 4.2: Polysilicon line (blue) that exceeds the active area (red).

Minimum width

This group of rules defines a minimum width and length that is bigger than the one imposed by the capability of the technology used. If these rules are ignored there is the possibility that a certain line is too narrow and can introduce a large local resistance or it may break. There is also a relationship between the planar dimensions and the thickness of the lines, the thicker a layer, the greater is the minimum allowable width. The designer has only the possibility to control the planar dimensions so the thickness is automatically modified according to the width chosen.

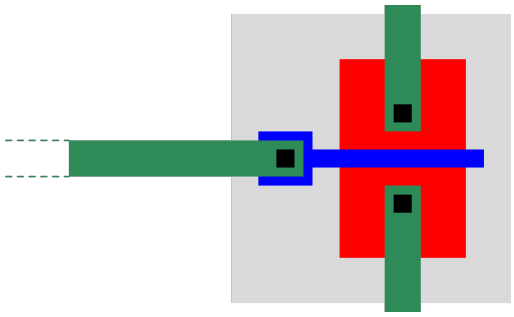


Figure 4.3: Layout with antenna problem.

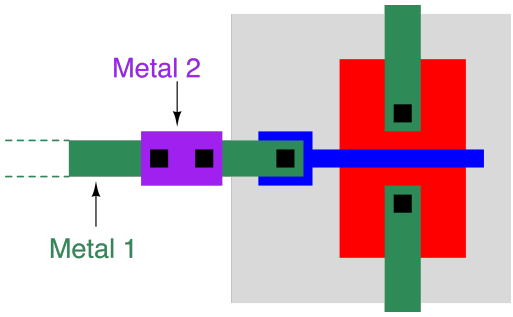


Figure 4.4: Fixed layout.

Maximum area

One of the most critical problems that must be avoided during the production phase is the so-called Antenna. If a transistor has the gate connected to a metal line, as shown in Figure 4.3, the latter is built after the transistor. This leads to the following situations: the gate has a rise of the potential during the etching of metal 1 because it acts as antenna, collecting the ions that surround the metal. If the area of the metal line is too large, there is the possibility that the voltage value on the transistor gate is too high causing the breaking of the gate oxide. If this happens, it is not possible to use the transistor anymore. To avoid this particular problem, the solution shown in Figure 4.4 is adopted. In this way, during the etching of the metal 1, the ions are limited because there is a gap that will be filled with metal 2 in a second step. This solution gives the possibility to connect transistors even if they are not close together.
This solution is used a lot in the chip to connect the bias to the channels, the DAC of the bias to the respective controllers and for each connection between analog parts with the local controller. Figure 4.5 shows an example of how this problem is solved. In order to reduce the antenna effect to a minimum every line has more than one gap.

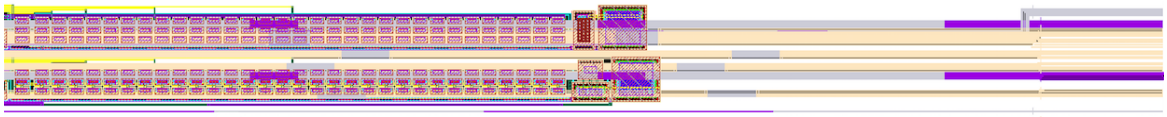


Figure 4.5: Part of a biasing cell and the lines that connect this cell to the global controller. Since the distance is bigger than hundreds μm, it is necessary to make the metal lines in two layers. In this case three different metal layers, that are represented with different colours, are used: grey, violet and yellow.

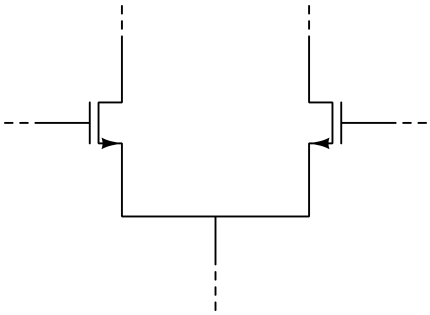


Figure 4.6: General differential input stage.

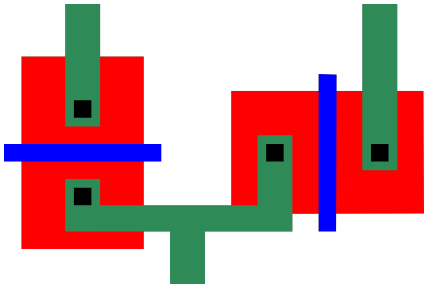


Figure 4.7: Asymmetric layout, that can cause mismatching between the two transistors.

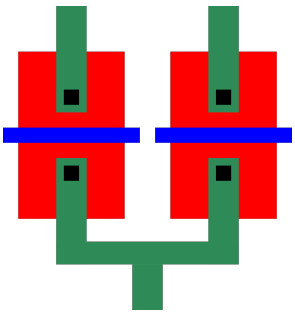


Figure 4.8: Vertical symmetry.

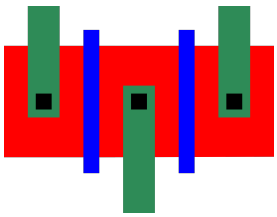


Figure 4.9: Horizontal symmetry.

The rules described above are important to guarantee the function of devices and they are even more important for the digital design, where the dimensions are pushed to the limits. However, for the analog design, usually the minimum dimension is not a big issue, but the most important problems are mismatches, noise, crosstalk, etc. In the PASTA layout, several techniques are used to reduce these undesired effects. One important characteristic, in particular for differential circuits, is the symmetry between transistors. An asymmetry, i.e. in a differential amplifier, means the introduction of an input voltage offset between the input transistors. The bigger the asymmetries, the larger the generated offset with respect the signal to be detected by the structure. An example of an asymmetric layout for the schematic of Figure 4.6 is shown in Figure 4.7.

The possible solutions are shown in Figure 4.8 and Figure 4.9. In the first one, the design has a vertical symmetry leading aligned gates and an almost perfect symmetry in all the transistors parameters. In the second one, the gates are parallel and this reduces the area used but introduces a small asymmetry due to the "gate shadow effect", as reported in Figure 4.10.

The implementation of the drain and the source is done with an inclination of 7° when the gate is already placed. This procedure introduces a narrow region on the drain or source that creates a small asymmetry between drain and source. Taking this effect into account it becomes clear that with a vertical symmetry both transistors are affected by a similar asymmetry with the drain smaller than the source. In the horizontal symmetry, if the drain is bigger than the source, the other has the opposite situation. Summarising, both configurations can be used with the trade-off between area consumption and performance.

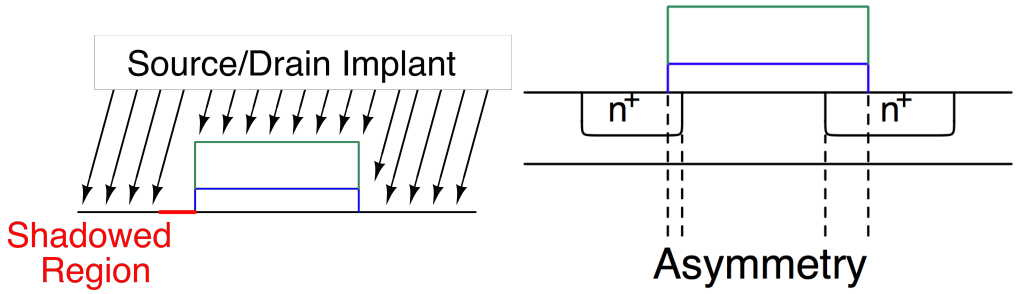


Figure 4.10: Representation of the gate shadow effect.

4.2 Analog channel layout

Using the rules given by the foundry and studying the most important techniques, it is possible to start the design of the layout of each architecture implemented in PASTA. In order to design it properly and to understand which is the best placement to guarantee the right connections between the structures, it is important to keep the area constraints in mind and analyse where PASTA has to be placed. Since in the MVD, the micro-strips are used both in the barrels and on the disks, the layout of the custom chip has to fit the constraints for both applications.
For the chips that have to be placed in the barrels, it is important to have a depth as small as possible in order to have the possibility to put all the cables behind the ASIC, but there is not a strong constraint for the width of the chip. On the other hand for the disks, it is mandatory to have a width that is not more than 5 mm, while for the depth there are no specific limits. Another important constraint, in our case, is the foundry. For a multi-project wafer run the company sells slots of silicon with an area of $5\,mm \times 5\,mm$. This means that i.e. if the chip has a size of $5.1\,mm \times 5.1\,mm$ the cost of the chip is four times bigger with respect to the $5\,mm \times 5\,mm$ version because it occupies four slots.

Merging all the constraints it comes up that the maximum area of the chip is $5\,mm \times 5\,mm$. To match this area it is important to understand if it is possible to have a full size chip as a first prototype, with 64 channels and internal biasing cells, or a reduced scale prototype.
This depends on which is the minimum distance between the channels, in particular which is the minimum space needed to be able to bond the chip to the sensor. Tests done in laboratory show that the minimum distance is $60\,\mu m$ if the pads are staggered, that means that the input pads can not be on the same line but must to be split in two lines. Having 5 mm as maximum width and having the possibility to have a channel pitch of $60\,\mu m$, it is possible to go for a full size chip. Moreover, since there was some free space it was decided to reduce the stress on the pitch going to $63\,\mu m$ in order to keep the layout of the single channel easier and keep $200\,\mu m$ for the biasing cells on the top of the chip.

The layout of a single channel is shown in Figure 4.11 (B). Figure 4.11 (A) shows the Front End with the connections to the Local controller. It start the pre-amplifier with the two feedback networks, then there is the current buffer that is connected to the high gain amplifier, the base line restorer and the structure used to generate the discharging feedback current. This block ends with the two hysteresis comparators. As shown in Figure 4.11 (A) there are a lot of lines that connect the Front End to the local controller. It is possible to group them in two types of lines: the outputs of the Front End and the configuration from the local controller to it.

In Figure 4.11 (C) is shown the layout of the TDC and the local controller with the connections. The first important consideration is that since there are two branches and there is a limitation in terms of space, the TDC has to be designed with a pitch that is less than half of the channel. In this way it is possible to insert both TDCs in the same area, this is important in order to have a good matching between the two structures. It is even clearer why for the TDC the area consumption is such an important parameter. The difference between the layout of the two branches is on the lines that are connected to the local controller, which distinguish the TDC that refers to the time branch from the one referring to the energy branch. The closest structure to the Front End is the current source that has on its right the local DAC used to adjust the discharging current. The middle part comprises the four TACs, each one has the respective C_{TAC} on the left. In order to have the maximum symmetry possible and to have the ratio between the C_{TAC} and C_{TDC} as precise as possible, the capacitor C_{TDC} is divided into four capacitors connected in parallel.

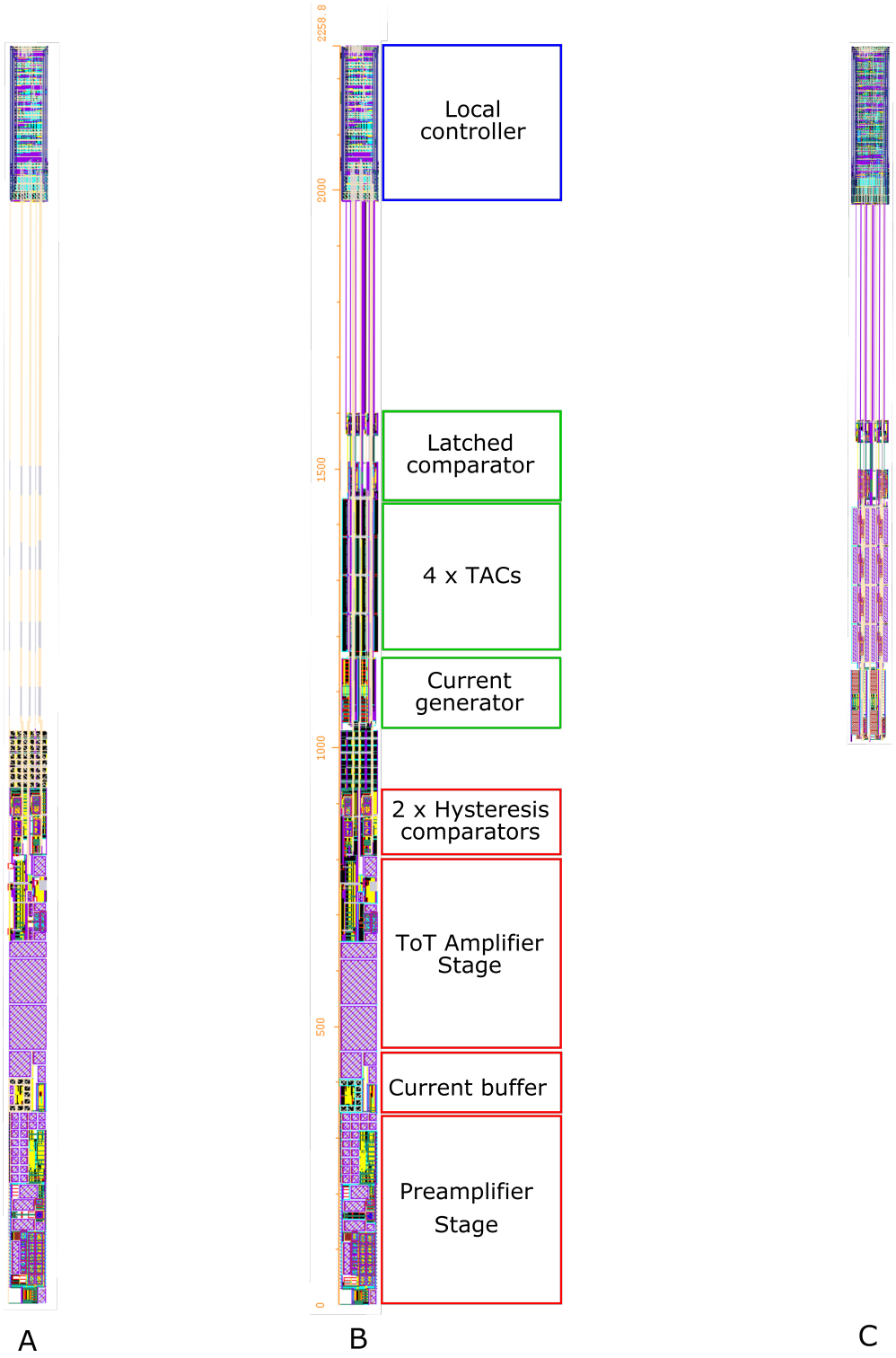


Figure 4.11: In figure B is shown the complete channel layout. The layout of the Front End with the connections to the local controller is shown in Figure A while the TDC and it connections to the local controller is shown in Figure C.

The last block is the latched comparator. The layout consists of two clusters, the first one is the part of the comparator without the clock distributions while in the second one the clock is injected. Some space, in the order of 50 μm, was deliberately left in order to reduce the possible noise introduced by the clock, keeping the clocked part well separated. Since in the chip the analog and digital domains are strictly separated, the Local controller, which has an intense activity when the chip is powered, is placed at a safe distance of about 400μm. This block is more dense with respect to the analog parts because the layout, in this case, is done by a specific algorithm that minimises the space, placing and connecting automatically the transistors.

During the design phase of the layout there are three important steps that have to be done: Design Rules Check (DRC), Layout Vs Schematic (LVS) and Post-layout EXtraction (PEX) simulations. With the first check, the tool used to design the layout controls that all the rules given by the foundry have been complied. For example, this check can fail if two metal lines are too close or if a metal line is too narrow. If the layout passes the DRC, this doesn't mean that it represents the schematic but only that the foundry is able to reproduce on silicon what is designed. Indeed, to understand if a layout corresponds to its schematic, the LVS check is needed. In this case the tool is able to match, one by one, every transistor and every connection between the schematic representation and the layout design. It is a powerful check because, during the design of the layout, it is possible to connect two different lines without realising it. When this check is also passed, the layout represents faithfully the schematic. However, it is not guaranteed that the behaviour of the designed structure is the same as for the schematic one. In the simulations of the schematic the parasitic capacitors and resistors are not taken into account since they can vary a lot with the design of the layout. One example can be the resistance of a certain line that connects two transistors, it can vary a lot if the two transistors are few μm away or hundreds of μm. For this reason the tool has a specific option that evaluates the layout and creates a schematic view with all the parasitic resistances and capacitors. At this point it is possible to run a simulation with the new schematic and when the behaviour of the new simulation matches with the one of the schematic without parasitic contributions, the layout of the structure can be considered finished.
Figure 4.12 shows one interesting result of the PEX simulations. This is done with all the analog channels layout and each component (all the blocks of the Front End, current generator, TACs, and latched comparator) passed the three tests independently. However, when everything is assembled together, in every TAC, after 700 ns a spike is injected in the recharging ramp. The problem was caused by the metal line of the "Reset" signal that passes above all the TACs and it wasn't isolated well enough . It was possible to improve the behaviour by shielding the "Reset" line better, reaching the desired result.

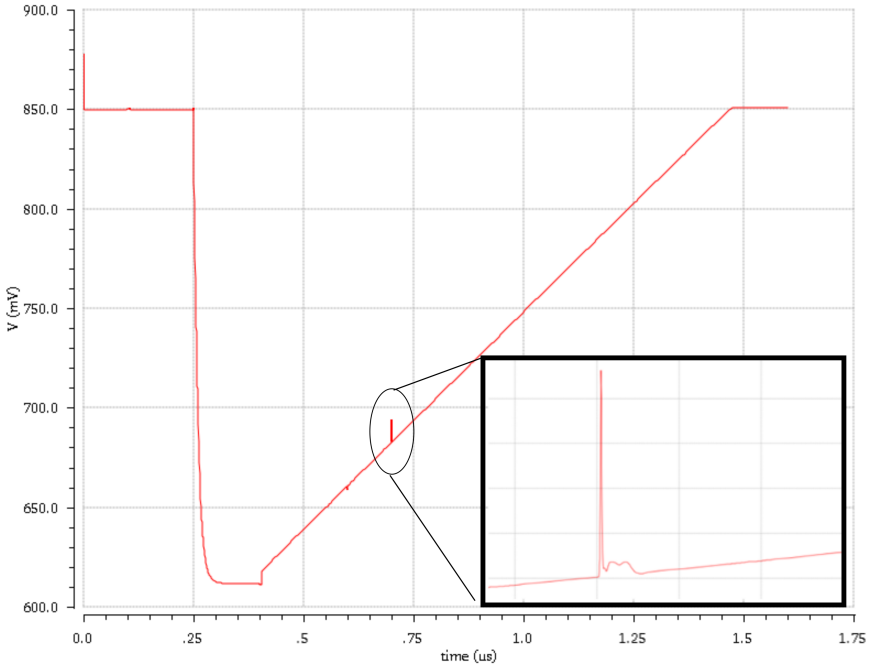


Figure 4.12: Shown in red is the voltage value on C_{TDC} during a simulation with the schematic generated by the PEX. It is possible to see that in the middle of the recharging ramp there is a glitch injected through a parasitic capacitor. On the right there is a zoom of the spike.

The connection between the analog part and the local controller is not that difficult because the only thing that has to be done is to define where the metal lines are and in which metal. This information is inserted into the script that generates the digital layout which creates narrow metal lines in the correct position and metal. The result is shown in Figure 4.13.

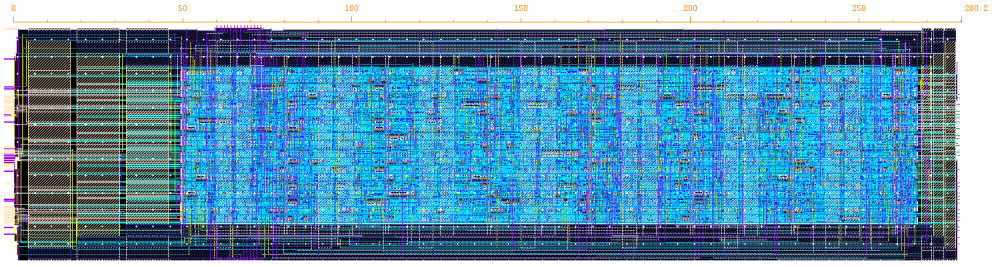


Figure 4.13: Layout of the local controller on which, in the left, there are the metal lines needed for the connections between the analog part of the channel and the local controller.

4.3 Final assembly

Once the layout of a single channel is completed, it is then necessary to replicate it 64 times and connect all to the global controller and to the bias cells. The connection between the global controller and the channels is not that difficult since both are in the digital environment so everything can be done via scripts and then it is possible to just overlap the correct metal lines. For the bias cell, the situation is completely different. Every cell has to be designed and checked and then placed in the dedicated region above the channel "0". The area reserved for the bias is in the order of 150 $\mu m \times 2300\,\mu m$ and contains also a structure called global calibration circuit that can be used during the test phase to send a suitable signal to the input of the pre-amplifier stage. In this group of cells, there are two types of connections, one from the global controller to the cells, necessary to set the DACs values, and one from the biasing cells to each channel. To propagate the bias into the channel, for each voltage value a metal line that goes from the biasing cell to the last channel is used.
The drawback of this design is that between each channel small parasitic resistances, due to the metal lines and the vias, are generated. However, all the bias are voltage propagated, meaning that the outputs of the biasing cells, which are transistors gates, are connected to gates in the channels. Therefore, since there isn't any current flowing, no difference between the voltage injected into the first channel and the last one is expected. This is true for all the bias generated on chip but there are two other quantities that are generated externally and fed to the chip: CSA_{IB2} and V_{ref}. The first one, as already mentioned in section 3.1.1, is the voltage value necessary to set the proper current into the pre-amplifier and this doesn't have any expected variation since also in this case the line is connected to a transistor's gate. However, for the second value, V_{ref}, the situation is a bit different. Also in this case, the line is connected to gates but, when the TDC is not in the recharging phase, the output of the current generator that generates the discharged I_{TDC} is connected to this line. In this case, there is a current that flows in this line that nominally is $500\,nA$ for each TDC. In this case, it is important to calculate the resistance between each channel introduced by the metal line and the vias. It is possible to do so using the documentation that the foundry gives to the users where the resistance per square of each metal is given. With this information and knowing the dimension of the line, a resistance of $20\,\Omega$ between each channel is evaluated.
A simulation was performed by inserting these resistances in order to understand if in the last channel the voltage value is usable or if it is necessary to correct it. The result is shown in Figure 4.14. The blue signal is the variation of the voltage value on the capacitor C_{TDC} for the first channel while the red signal refers to channel "63". The end of the recharging ramp corresponds to the value of V_{ref}. I can be seen that for the channel "63" the voltage value is shorter, and thus the recharging phase smaller, compared to the first channel. This means that

it is possible to use the layout as designed but this offset that increases from top to bottom must be taken into account during the test phase.

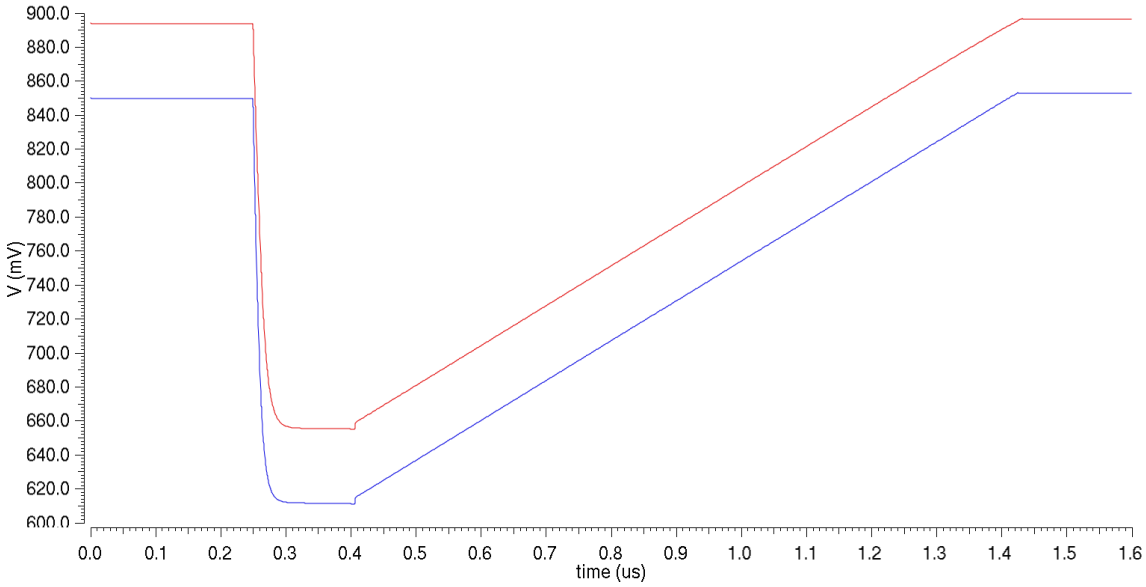


Figure 4.14: Simulated effect of the parasitic resistors between each channel on V_{ref}. The voltage value on the capacitor C_{TDC} in the channel "0" (blue) and in the channel "63" (red) are shown. It can be seen that in the last channel the recharging phase is shorter with respect to the first channel.

Not only the internal bias have to be propagated in the chip but also the voltage power supply, the ground, and the substrate reference. To propagate them, two power grids are used: one for the analog domain and one for the digital one. To assemble the grids, the two metals that are on top of everything and that have different characteristics with respect to the other metal layers have been used.
The minimum size of the lines is much larger and the thickness is higher too, leading to a lower resistivity of these lines. For every analog pad in the PASTA chip, there are 5 lines of metal that horizontally cross the core while for the digital pads the five lines of metal end above the local controller. The second highest metal crosses the core of the chip vertically with a lot of lines making the two power grids. The connections between these two metal layers are done with several vias in order the reduce the resistivity of these connections. Finally, every time it is possible to connect the grid with the lower levels, this is done with several vias in order to have a capillary distribution of these signals.

The last part to design is the pad ring with the seal ring. It i s one of the most important and delicate parts to implement because it acts as a shield for the chip and it is where the chip interfaces with the external environment that can cause one of the most common problems, called ElectroStatic Discharge (ESD). Usually, this effect happens when an external object with a high potential level somehow touches the connections of the circuit. For example the wires that are bonded to the pads or charge in dry air may create potential gradients with respect to ground.
The ESD can cause two types of permanent damage: the first one can happen when the electric field exceeds $10^7\ V/cm$, leading to a breakdown of the gate oxide. This value of electric field can be reached with 2V affected to a gate, with that has an oxide thickness of 20 $\AA$ [84]. The second case is when a large current flows through a source/drain junction diode. It may happen that the junction melts, creating a short in the substrate. It is possible to minimise these effects using specific circuits for ESD protection, one example is shown in Figure 4.15. The diode discharges to ground or Vdd, limiting the possible potential applied to the circuit, and thanks to the resistor the diode is protected from large currents. Even if this kind of structure is needed to preserve the chip, it introduces two main drawbacks: capacitances are inserted between ground and Vdd, reducing the circuit speed, and it may couple noise on the Vdd, thus corrupting the signal.
In addition, a not well designed ESD protection circuit may lead to latch-up when the discharge occurs at the powering of the chip or during normal circuit operations. It is therefore important that the technology chosen for the design of the chip has different ESD structures in order to find the one that suits best.

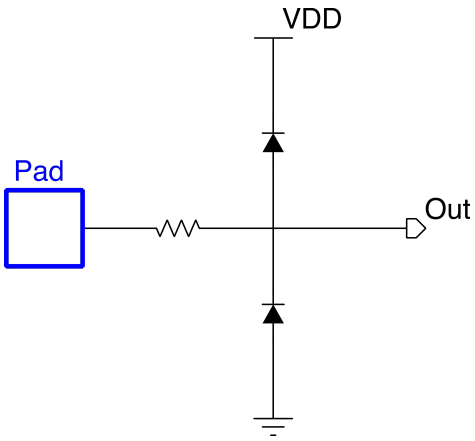


Figure 4.15: Schematic of a simple ESD protection needed by the pads.

Once an agreements is obtained with the foundry for these structures, it is possible to start the design of the pad ring. Two different types of pads are used: one for the signals and one for the powering. In Figure 4.16 the pad ring is shown, where the yellow rectangular regions are the pads while the light blue layers guarantee that the pad ring is at the same voltage level. In the right part and in the bottom part there are two breaks that interrupt the pad ring in order to maintain the separation between the analog and the digital powering. There are four specifics pads that are used to power the two parts of the pad ring. It is surrounded by the seal ring that is a structure needed to protect the pad ring and is connected to the substrate.

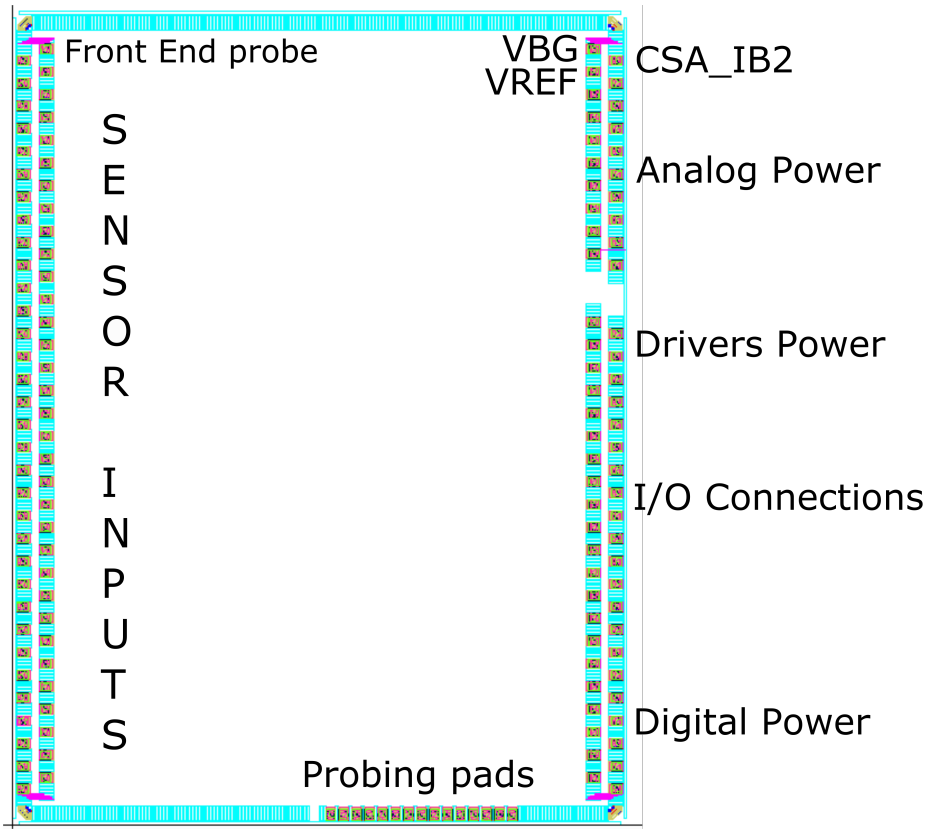


Figure 4.16: Final version of the layout of the pad ring and seal ring, placed on the PASTA edge.

After that everything is connected together and last checks are performed, the complete layout is sent to the foundry for production which usually takes about three months. This period is useful to collect all the informations of the chip in a small user guide that is used during the test phase.

5

EXPERIMENTAL RESULTS

This chapter describes the characterisation of the chip and the experimental setups developed to test it. Moreover, the first results from the PASTA tests are presented in the last section.

5.1 Powering board

As already mentioned in section 4.3, after the submission of the project to the foundry there were few months where it has been possible to work on the documentation (a reduced version of the user guide is in the Appendix A). Meanwhile, a small board that is used to test the bonding scheme and the bias lines of the chip was developed and produced.
The tests done with this board highlight two problems. The first one is the pad size of PASTA shown in Figure 5.1. They are small, resulting in a low yield of the wire bonding between the chip and the board pads. The application of smaller wire, with 17 μm diameter, and the work of very experienced operators recovered the issue. The results of this work is shown in Figure 5.2.

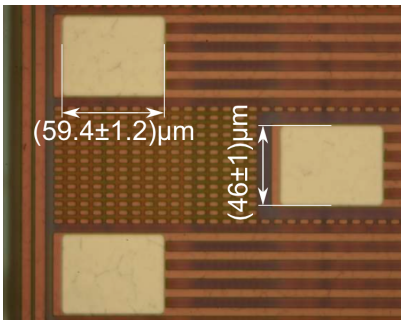


Figure 5.1: High resolution photo of the pads of the chip. The picture is obtained using a microscope [85].

The second problem is a more serious problem and it concerns the chip biasing. The chip needs three voltages to work, provided by the Power Board (PB): AVDD (analog Vdd at 1.2 V), DVDD (digital Vdd at 1.2 V) and DVDDIO (drivers Vdd at 2.5 V). During the design of the ESD protection, a diode was placed with an inverted polarity, leading to a situation where two voltages, the DVDD and DVDDIO, are not independent anymore but they are linked together with a maximum difference of 0.7 V. In this situation, it is thus impossible to apply the nominal voltage values.
To overcome this problem two solutions are possible. The first one is to keep the best working condition for the drivers, biased at 2.5 V, and overpower all the digital circuit at 1.8 V. Alternatively, the digital part of the chip is left at 1.2 V, while the drivers are under-biased at 1.9 V.
The drawback of the first solution is given by a physical limit of the transistors in the digital part. In fact, they are designed to work at 1.2 V meaning that the gate oxide has a specific thickness in order to endure the corresponding electric field. By increasing the bias there is a concrete risk of breaking the transistors' gates. In the second solution, the possible drawback is that the underpowered drivers are not able to handle the input/output signals. In this case, it is not possible to configure the chip and to decode data from PASTA. In order to understand if there is a condition where it is possible to configure the chip without destroying the digital part, simulations with several voltages have been done. The results show that the drivers are able to read the output signals from the external structures and recognise input signals coming from the outside with a voltage power supply of 1.9 V. Therefore, in order to avoid stressing of the digital architectures, it was decided to have the DVDDIO at 1.9 V and the DVDD at 1.2 V.

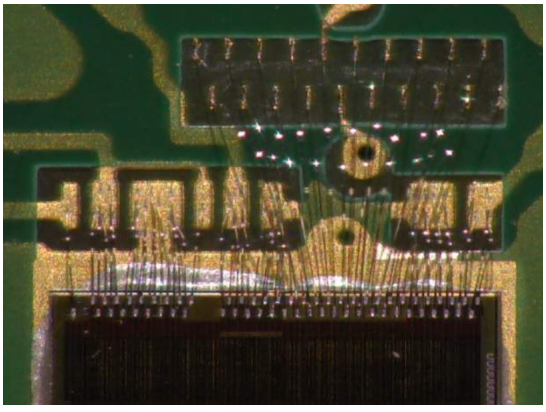


Figure 5.2: Picture of the PASTA wire bonded to the PB with 17 μm diameter wires[85].

5.2 Test board

The PB used for the powering tests is not enough for a complete characterisation of PASTA, therefore, a test readout board of $18 \times 10\,cm^2$ has been designed. The prototype, called Digital Interface for Strip data Handling (DISH), consists of 4 layers: top, ground, power, bottom. All the signals are routed in the external layers (top and bottom), while the power layer contains the five voltage domains needed for this board: the three voltages used by PASTA, a voltage of 3.3V for the services, and 5V for the board biasing. The overview of an assembled board is shown in Figure 5.3, PASTA is wire bonded to the board and placed under the black box. The schematics of the DISH design are reported in Appendix B.

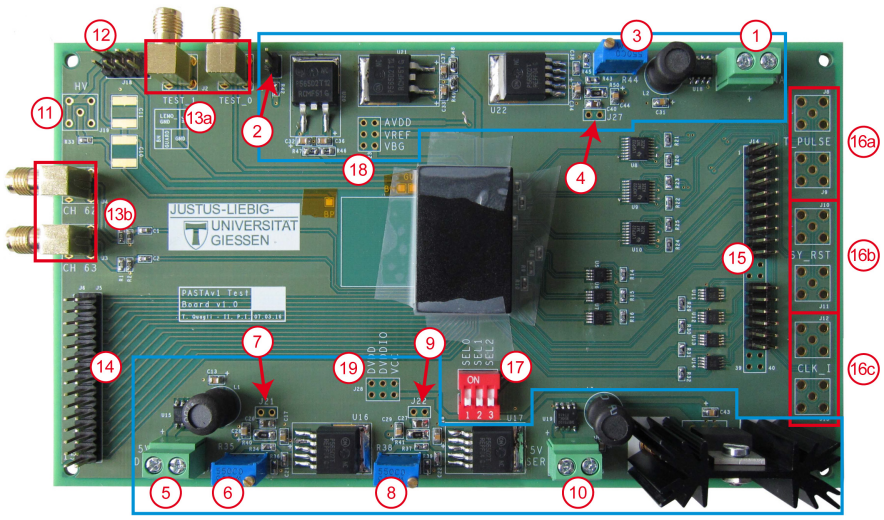


Figure 5.3: Photo of an assembled DISH with PASTA bonded on it. The chip is situated under the black box in the middle of the board. Details see text.

In the following pages a description of the test board is given:

- The powering of the board and the chip is done with an external voltage power supply of 5 V. It is connected to the connectors 1, 5, and 10 in the blue regions in Figure 5.3.

  The first one generates, using three different circuits on the board, AVDD, VBG and Vref. In this region there is also the jumper number 2 where a resistor can be connected. In this way the current CSA_IB2 can be set. However, due to a mistake during the simulations, the maximum current that the board can generate is half of the nominal $800\,\mu A$ even if the jumper acts as a short between the resistor on board and the ground. This problem reduces the performance of the Front End in terms of noise.

The second connector (number 5) provides the DVDD and the DVDDIO while with the third one (labeled 10) a voltage 3.3 V is generated and used for the services of the board. The AVDD, DVDD and DVDDIO can be tuned by using dedicated trimmers.

- The upper left region in Figure 5.3 is reserved for the biasing of the sensor. There is a LEMO connector (not soldered on this board), labeled 11, and a pin header (12) that is connected as shown in Figure 5.4. The typical sensors that will be used for the tests, require at least 70 V on the LEMO connector to be fully depleted.

- The couple of SMA labeled 13a are connected directly to the first two pads of PASTA. The left one is the analog output of the Front End chain before the hysteresis comparators, while the one on the right is an input signal to enable the previous output. The SMAs 13b are connected at the input of the last two channels of PASTA, in this way it is possible to inject an external test signal.

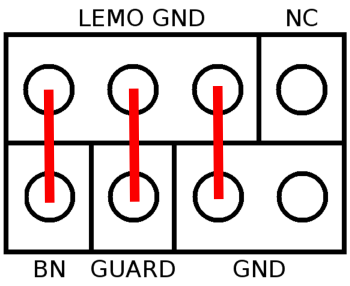


Figure 5.4: Pin header connections to select the biasing of the sensor. The LEMO GND is the ground of the HV used to bias the sensor. It is connected with the n-bulk of the sensor (BN) to the guard ring of the sensor (GUARD) and to the ground of the board (GND).

- The pin header labeled 14 is connected to the probe pads in the bottom part of PASTA. The left column of the pin header is connected to ground while the right column is connected to the pads as shown in Table 5.1.

Pin #	Signal
1	DOT
2	DOE
3	Coarse time (time branch)
4	Coarse time (energy branch)
5	SOC
6	EOC (time branch)
7	EOC (energy branch)
8	Valid event
9	Status of the TAC number 0
10	Status of the TAC number 1
11	Status of the TAC number 2
12	Status of the TAC number 3
13	Comp_Out_ (time branch)
14	Comp_Out_ (energy branch)
15	Payload_R

Table 5.1: Digital test points

Pin #	Signal	Pin #	Signal
1	CLK_I +	2	Sync_Reset+
3	CLK_I -	4	Sync_Reset-
5	-	6	TEST_Pulse+
7	-	8	TEST_Pulse-
9	SDI +	10	-
11	SDI -	12	-
13	SCLK +	14	-
15	SCLK -	16	-
17	CS +	18	-
19	CS -	20	-
25	TX0 -	26	-
27	TX0 +	28	-
29	TX1 -	30	CLK_O+
31	TX1 +	32	CLK_O-
33	SDO -	34	-
35	SDO +	36	-

Table 5.2: Pin header for the communication between PASTA and the evaluation board.

- All the input/output signals of PASTA are connected to the pin header (15), designed in order to match the readout system. PASTA has six inputs and four outputs; for each of them there is a transmitter or a receiver on board. The signals are connected to the pin header as reported in Table 5.2. Moreover, three particular inputs can also be connected to the SMAs connectors (labeled 16): the SMA couple 16a is connected to Test Pulse, the SMA couple 16b to the synchronous reset, and the SMA couple 16c to the Clock. The choice to use SMAs instead of the pin-header is done with the DIP switch labeled 17. If the switch is "on" the chip is connected to the SMA, otherwise it is connected to the pin-header. The switch has three selectors: 1 for the Test pulse, 2 for the synchronous reset and 3 for the clock.

5.3 Experimental setups

The read-out setup used to test PASTA comprises: the DISH readout board, an adapter board, the evaluation board with a Field Programmable Gate Array (FPGA) and a PC with a user interface software and a network link between the PC and the evaluation board.
For the first tests two software variants have been developed. The first one is developed in the LabVIEW environment in Turin while the second one is developed in C++ in Jülich, called Jülich Digital Readout System (JDRS).
The main characteristics of the system developed in Turin and already tested on previous prototypes are: system clock up to 160 MHz, a low rate capability, a standalone analysis. The main characteristics of JDRS are: an integrated compatibility with PANDA Root, leading to an on-line analysis, a high rate capability, system clock up to 80MHz (at present).
Both system are based on the same evaluation board, the ML605, equipped with a Virtex-6[1]. The main advantage using the ML605 board is its flexibility and a lower cost compared to a custom board. Under these conditions the first software is used for the laboratory tests while the second one will be used for the beam tests. During the test phase, two readout systems help a lot to identify and fix bugs that the systems might have.

5.3.1 LabVIEW software

The software is composed of several programs. The one used for the characterisation of a typical channel has an interface with two main tabs: configuration tab and measurement tab.
The first one, shown in Figure 5.5, consists of several blocks. In the "global configuration" box both the analog and the digital global configurations can be modified. In the "global test config" it is possible to enable the global calibration circuit and set the amplitude of the test pulse, enable the probing pads and define which channel is connected to them. In the box "Ex TP out", it is possible to define the parameters of an external test pulse, define a correction of the test pulse phase if needed and some other settings in order to achieve the right synchronisation with the PASTA data outputs.
In this system in the channel configuration can be defined using two boxes, one called "Default channel config" and the other one called "Active channel config". The first one allows to set the configuration for all the channels of the chip. In the second one it is possible to define the configuration bits only for the channel under test. Moreover, with the buttons below these two boxes, it is possible to define if the input of the Front End is connected to the line of the internal test pulse or not.

1 Virtex® is the main Field Programmable Gate Array (FPGA) developed and distributed by Xilinx. The version six was released in 2009 and it is fabricated with a 40 nm process.

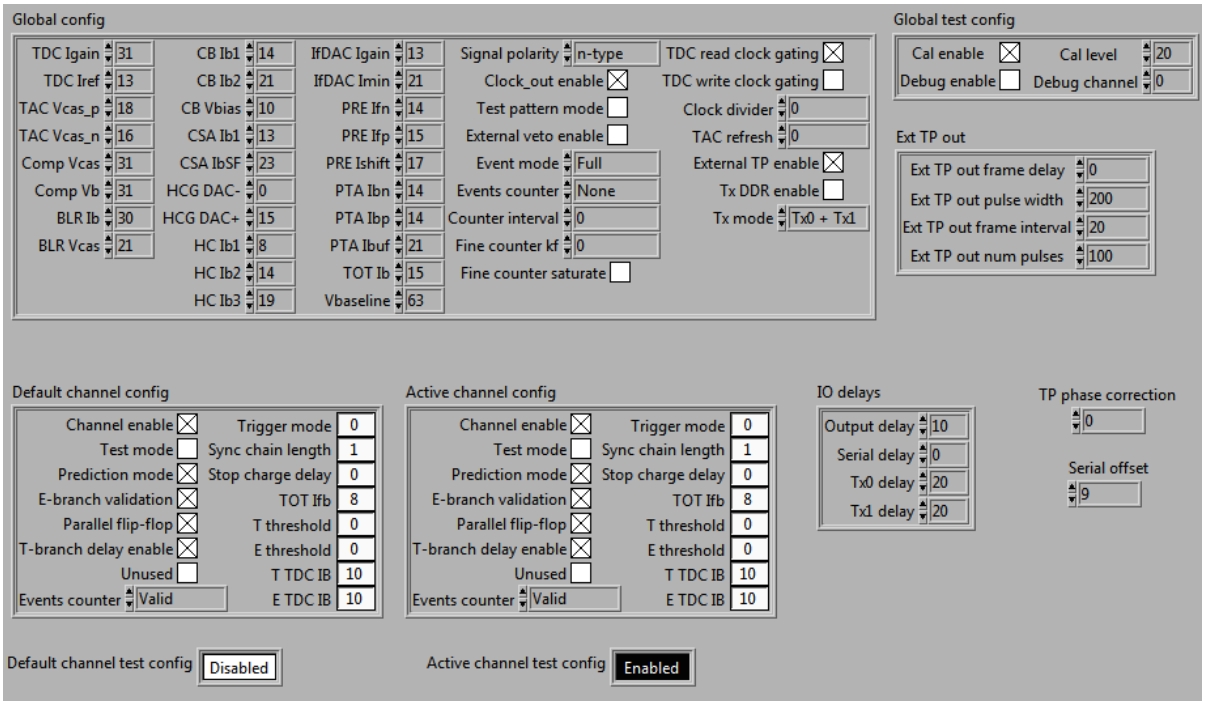


Figure 5.5: Interface for all the configurations in the LabView system developed in Turin.

In Figure 5.6 there is an overview of the measurements tab. It consists of three regions: the measurement parameters highlighted in blue, the scan variables in red and the graphs. In the upper part of the first region, it is possible to check the firmware version and the clock frequency of the system. The second row shows which channel is under test, which is the value of the scan parameters A and B and the FIFO. These values are updated in real time during the data taking. Below this row, there are controllers to specify information like the first and last channel that has to be scanned, how many TACs are to be used and the test pulse configuration.
In the red region, it is possible to choose two settings from the possible PASTA configuration parameters. The measurement will start with the minimum value of the parameters A and B and the program will send n pulses for this configuration. After that the system will increase the value of the parameter A, keeping B at the minimum, sending n pulses for each step until the maximum value. In this case, a scan of the pulse phase from 0° to 720.0° is performed in 32 steps . If there is a second parameter, the program will increase the B value by one step and the scan of the parameter A will start again as before, and a new colour is used for the graphs to distinguish curves for different value of B. When both A and B are scanned, the measurement will be performed for the next channel.

There are two types of graphs: the first two where the x-axes refer to the parameter A and the y-axes indicate the event numbers. The following plots have two y-axes where the unit of measurement for both is the clock cycles. In these graphs, there are two shapes for the dots: the big dots are average values for each specific condition which refers to the left y-axis and the small ones that are the respective standard deviations which refer to the scale on the right.
When the complete scan is ended for one channel the graphs are updated in real time with the value for the new channel. At the end of the entire measurement, it is possible to select different channels and it is also possible to filter the data plotted for a specific value of the parameter B.
The first graph represents all the signal seen by the chip; if there are no errors in the configuration phase they must be equal to "TP num pulse" in the blue region. In the second graph the events connected to the channel under test and its configurations are shown, i.e. if there are 100 pulses only one TAC of the available four is allowed to take data, the selected events should be 25. Usually the first and the second graphs have the same amount of events if the configuration is done properly.
In the third (fourth) graph, the values of the coarse time for the time (energy) branch are reported. Since the SOC signal is unique for the two branches, there is only one graph for it while there are two graphs for the time EOC and the energy EOC. The graph called "T fine" which represents the time difference EOC - SOC is not active for this measurement.

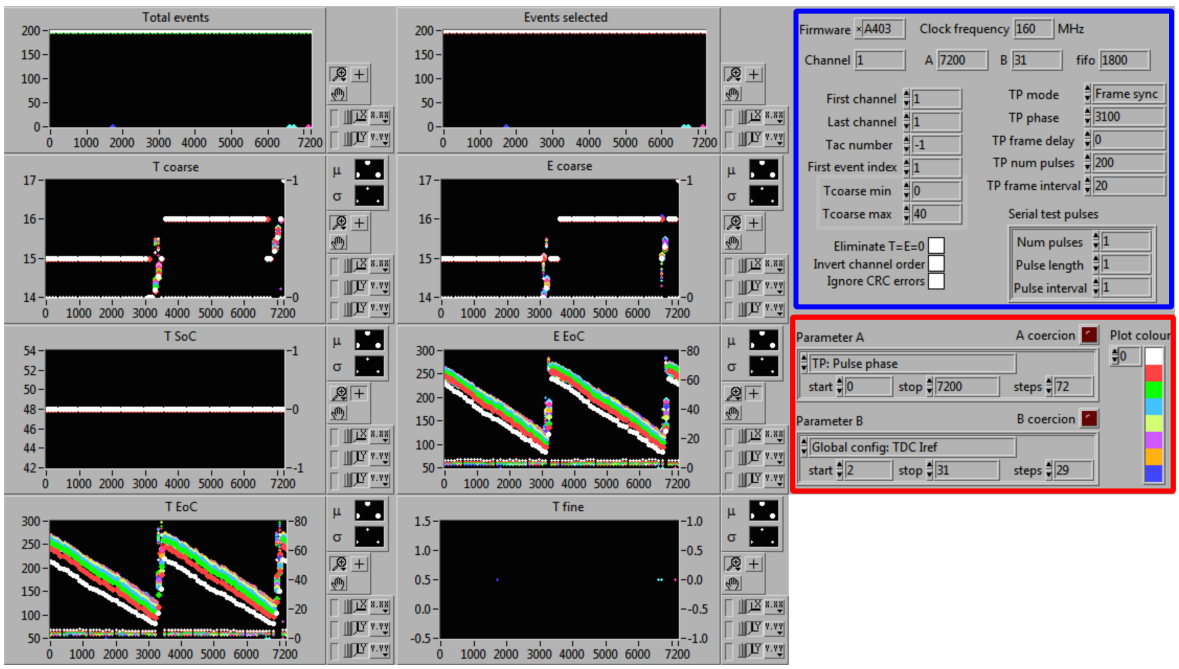


Figure 5.6: Measurement interface in the LabView system. In blue there is the measurement parameters region, in red is the region where the variables that are to be scanned are defined.

5.3.2 Jülich Digital Readout System (JDRS)

The firmware of the JDRS, developed also for testing of ToPix, is shown in Figure 5.7. It is a modular architecture, it is possible to modify only the Device Under Test (DUT) module to test a new ASCI, as is the case for PASTA. In this way the MVD will have only one readout software for both the readout chips. The JDRS also consists of software with a graphical user interface for ease of use during the testing phase.

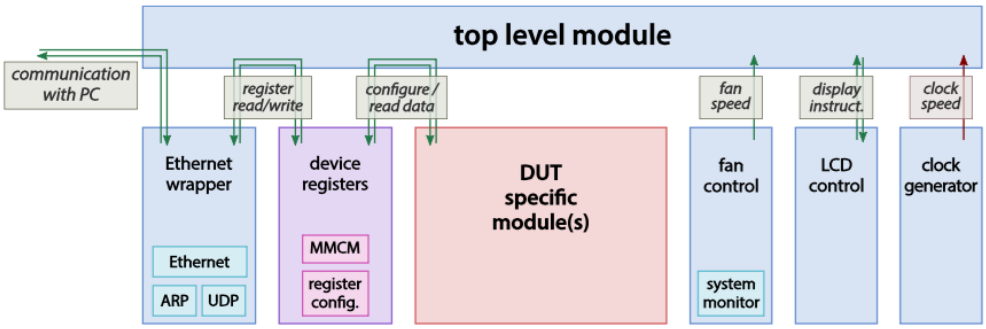


Figure 5.7: Block diagram of the firmware used in the JDRS. The modular structure allows to change only the part of the DUT to test a new ASIC [78].

For PASTA, at the time of writing this thesis, the interface of the software is composed of several windows, the most important are reported and described here. First of all, there is the connections interface, Figure 5.8.

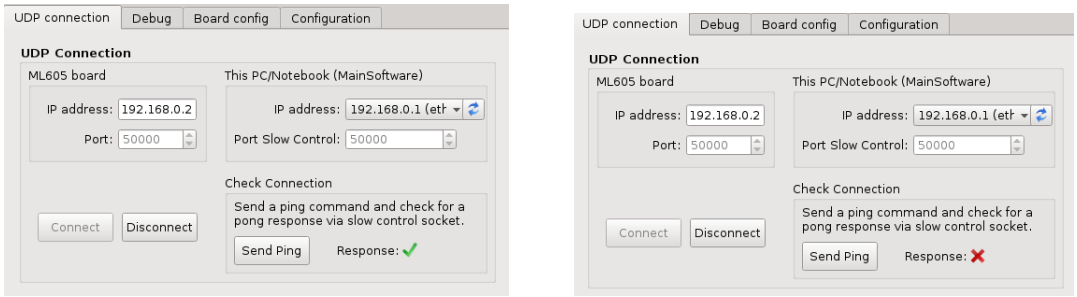


Figure 5.8: Connection interface in the JDRS. In the figure on the left the connection was successful since the response mark is green while on the right figure the mark is red meaning that the connection has failed.

It is the first window that appears when the software starts, in this section it is possible to set the IP of the evaluation board and of the PC and connect the PC to the ML605. In order to check if the connection is done properly, it is possible to send a ping command and if a green mark appears the FPGA board is connected to the PC. If it is red there isn't any connection.
The second important tab for the user is the "Configuration" window. It contains five different sub-windows: Global, Global expert, Channel (Expert) I, Channel (Expert) II and Test Pulse.
The first one, "Global" in Figure 5.9, is divided into two sections, the first one contains all the digital configuration and second one is dedicated to the analog part. The one labeled " Global expert" shows a table where it is possible to modify each global configuration bit.

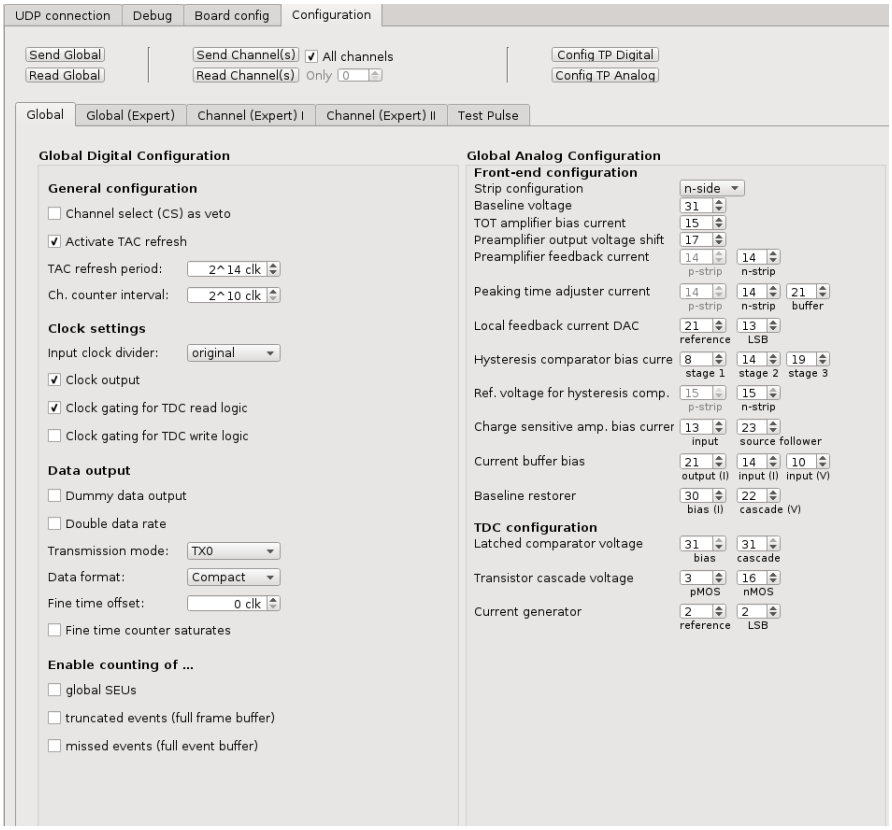
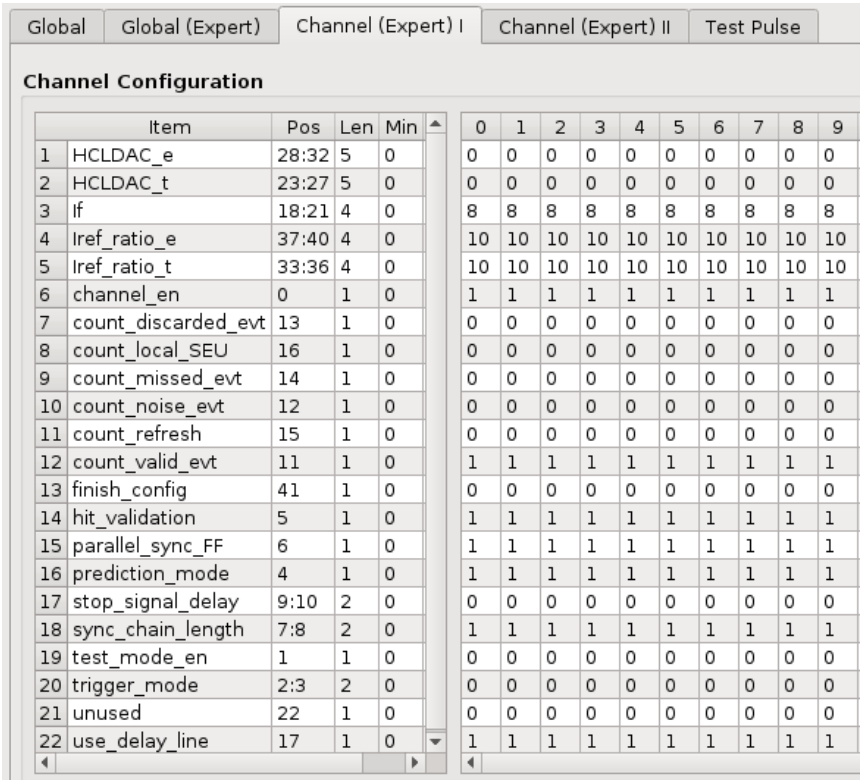


Figure 5.9: Global configuration interface for typical users.

The third window named "Channel (Expert) I", dedicated to expert people, shows a table in which it possible to modify the channel configuration, bit by bit (see Figure 5.10).
In the fourth one, "Channel (Expert) II", it is possible to define, channel by channel, the connections between the input Front End and the internal test pulse line.



	Item	Pos	Len	Min	0	1	2	3	4	5	6	7	8	9
1	HCLDAC_e	28:32	5	0	0	0	0	0	0	0	0	0	0	0
2	HCLDAC_t	23:27	5	0	0	0	0	0	0	0	0	0	0	0
3	If	18:21	4	0	8	8	8	8	8	8	8	8	8	8
4	Iref_ratio_e	37:40	4	0	10	10	10	10	10	10	10	10	10	10
5	Iref_ratio_t	33:36	4	0	10	10	10	10	10	10	10	10	10	10
6	channel_en	0	1	0	1	1	1	1	1	1	1	1	1	1
7	count_discarded_evt	13	1	0	0	0	0	0	0	0	0	0	0	0
8	count_local_SEU	16	1	0	0	0	0	0	0	0	0	0	0	0
9	count_missed_evt	14	1	0	0	0	0	0	0	0	0	0	0	0
10	count_noise_evt	12	1	0	0	0	0	0	0	0	0	0	0	0
11	count_refresh	15	1	0	0	0	0	0	0	0	0	0	0	0
12	count_valid_evt	11	1	0	1	1	1	1	1	1	1	1	1	1
13	finish_config	41	1	0	0	0	0	0	0	0	0	0	0	0
14	hit_validation	5	1	0	1	1	1	1	1	1	1	1	1	1
15	parallel_sync_FF	6	1	0	1	1	1	1	1	1	1	1	1	1
16	prediction_mode	4	1	0	1	1	1	1	1	1	1	1	1	1
17	stop_signal_delay	9:10	2	0	0	0	0	0	0	0	0	0	0	0
18	sync_chain_length	7:8	2	0	1	1	1	1	1	1	1	1	1	1
19	test_mode_en	1	1	0	0	0	0	0	0	0	0	0	0	0
20	trigger_mode	2:3	2	0	0	0	0	0	0	0	0	0	0	0
21	unused	22	1	0	0	0	0	0	0	0	0	0	0	0
22	use_delay_line	17	1	0	1	1	1	1	1	1	1	1	1	1

Figure 5.10: Channel configuration interface for expert users, there is a column for each channel.

The last sub-window, shown in Figure 5.11, features four fields: Configure Digital Test Pulse, Configure Analog Test Pulse, DAQ FIFO data, and Channel Scanner. The first one defines the parameters for the internal test pulse (see more details in Appendix A.3.2). The second field is dedicated to enable the probing pads and select the channel connected to them. There are two more options for the global calibration circuit, one to define the amplitude of the signal injected to the Front End and the second one to enable the global calibration circuit.
The DAQ FIFO data box is used to define where and how the program generates a file where output data from PASTA are written. The last box is used to perform the scan of all the parameters. It is possible to select the channel number, which parameters have to be changed, and in which range.

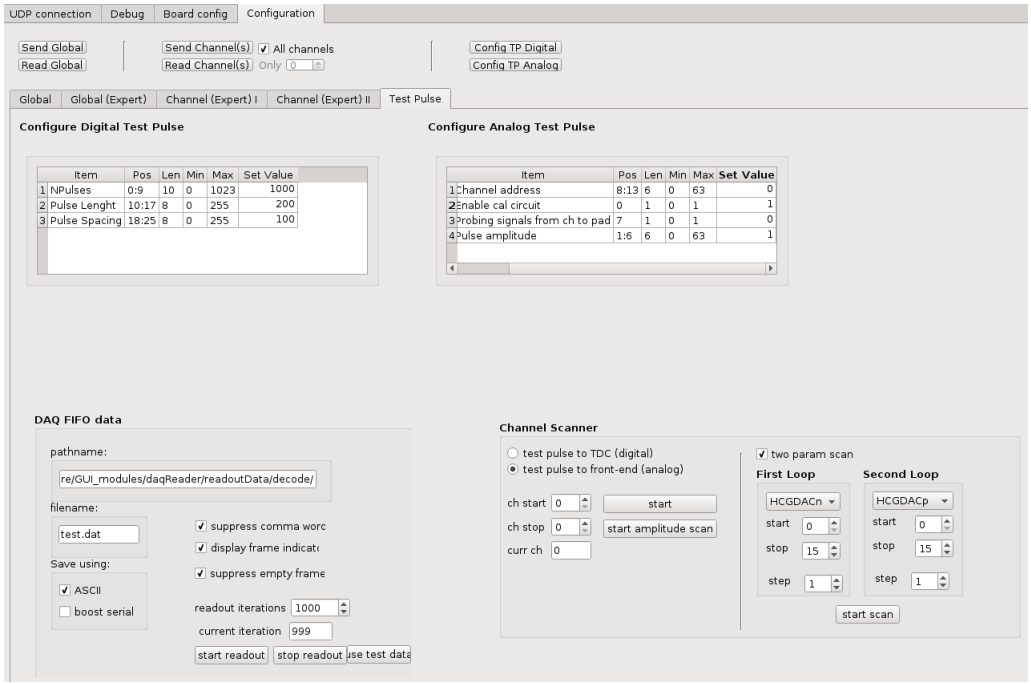


Figure 5.11: Tests configuration interface. In "Configure Digital Test Pulse" there are the parameters for a digital test pulse. In "Configure Analog Test Pulse" it is possible to define the amplitude of the test signal injected into the Front End, to enable the calibration circuit that generates the test pulse and chose which channel is connected to the probing pads. In "DAQ FIFO data" it is defined how and where the data are saved. Finally, in "Channel Scanner" it is possible to choose which parameter is to be scanned and in which range.

5.4 Test setup and results

The complete setup of Torino used for the tests is shown in Figure 5.12, DISH (1), the evaluation board (2) and the breakout board (3). Morevoer, to power the board, a voltage generator with at least two channels is used, while an oscilloscope is present for debugging purposes. Since time for the tests was an issue it was decided to perform the most important characterisation for a typical channel.

5.4.1 Configuration of the chip

The first step to do is the the configuration of the chip though the user interface. Using the oscilloscope it is possible to verify that each sent command shows the right structure (more details in the subsection 2.3.2.1). In Figure 5.13 two signals are shown, the blue one is the SDI

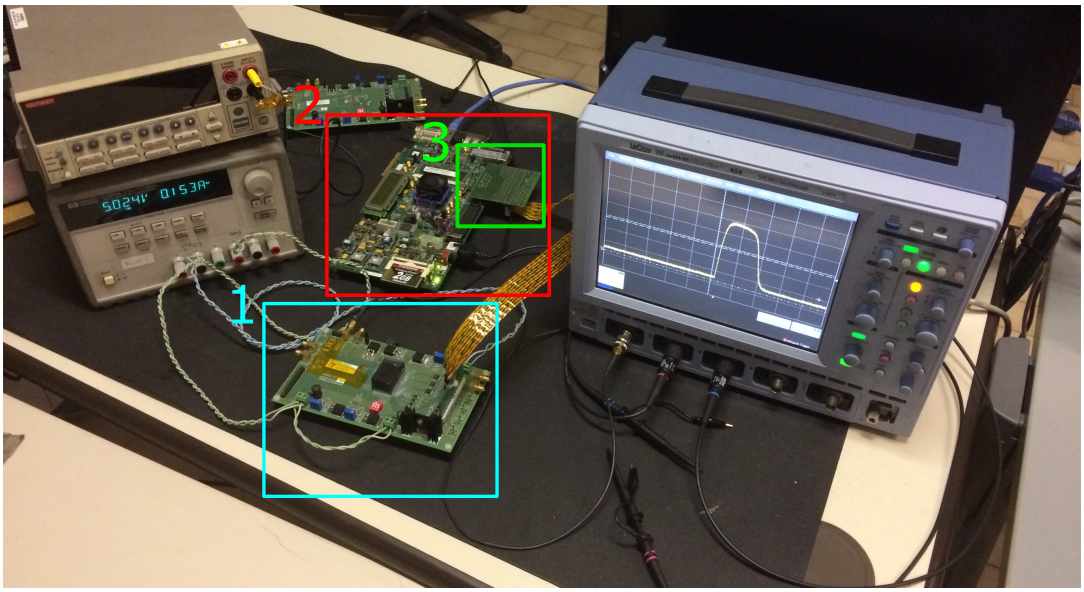


Figure 5.12: Photo of the laboratory setup used during the tests of PASTA. The DISH (azure box), the evaluation board (red box) and the breakout board (green box)

while the magenta represents the SDO. In the left picture, the SDI contains the information for the command "Write channel configuration": command bits, channel address, configuration data and CRC (more information about this command is given in Section A.3).

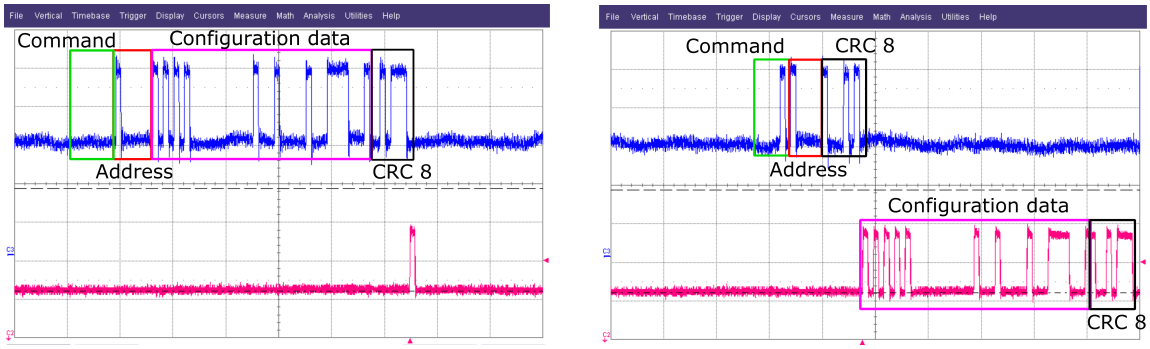


Figure 5.13: The left picture shows the SDI (blue) and the SDO (magenta) when the command "Write channel configuration" is sent to the chip. In the right picture the SDI and SDO are shown when the command "Read channel configuration" is sent.

The SDO for this command is "0" and goes to "1" only when all the bits in the SDI reached the chip and the CRC is checked. The picture on the right in the Figure 5.13 corresponds to the command "Read channel configuration" sent after the "Write channel configuration". This is a common procedure to check if the registers in the chip have store the received values. As before the blue signal is the SDI where the instruction for PASTA is defined and the magenta

one is the SDO. In this case, the SDO contains the configuration data stored in the chip and the CRC.
Before the characterisation of a typical channel, it is important to define how the structure in PASTA can be tested. Figure 5.14 shows the calibration circuit scheme for PASTA.
The test pulse can be injected into the chip from the SMA or the FPGA if the bit "External pulse enable" is "1", otherwise it can be generated internally with the command "Configure internal test pulse" (see subsection A.3.2). Whatever the way, digital test pulses, with the characteristics decided by the user, go out from the global controller and are fed into two different lines. One is connected to the global calibration circuit through switch 1. The global calibration circuit uses the pulses as triggers to generate a series of analog signals. Each signal corresponds to a digital trigger and features an amplitude set using a DAC with a range from 0 to 63. The analog signals thus created represent the charge signals from the sensor and are propagated with a metal line from the channel "0" to the channel "63". For each Front End, there is the possibility to connect its input to this line. In this way, it is possible to test the Front End chain. The TDC can be tested in two configurations using switch number 3. If it is set to "0", the local controller uses the output of the Front End comparators to perform the measurement triggering the TDCs. If it is set to "1", the local controller takes the digital pulses coming from the global controller directly instead of the Front End output. This is the best configuration in order to test the behaviour of the TDC plus the local controller. Switch 3 can be set independently for each channel. Enabling switch 5, it is possible to connect some signals from the local controller to the probing pads. Using switch 4, only one channel at a time can be connected to the pads.

5.4.2 TDC characterisation

As previously mentioned, for the test of the TDC architecture a digital test pulse is needed instead of the output of the hysteresis comparator. In this way, it is easier to measure the key parameters needed for the calibrations. The TDC has to measure the fine time, that is the distance between the leading edge of the test pulse and the clock. For this reason, to analyse its behaviour, it is necessary to perform a phase scan test where several test pulses are sent to the local controller with a specific phase with respect to the clock. The phase of the test pulses is then varied from 0 degrees to 720 degrees, in 10 degree steps. Figure 5.15 shows the measurement interface at the end of a phase scan. The channel is configured in a way that both branches are triggered with the leading edges of the test pulses.
From the first two graphs it can be seen that for each phase 200 pulses are sent to the channel under test. Since the two branches (time and energy) are triggered in the same way, the description of the next part is done only for the time branch but can be applied also to the energy

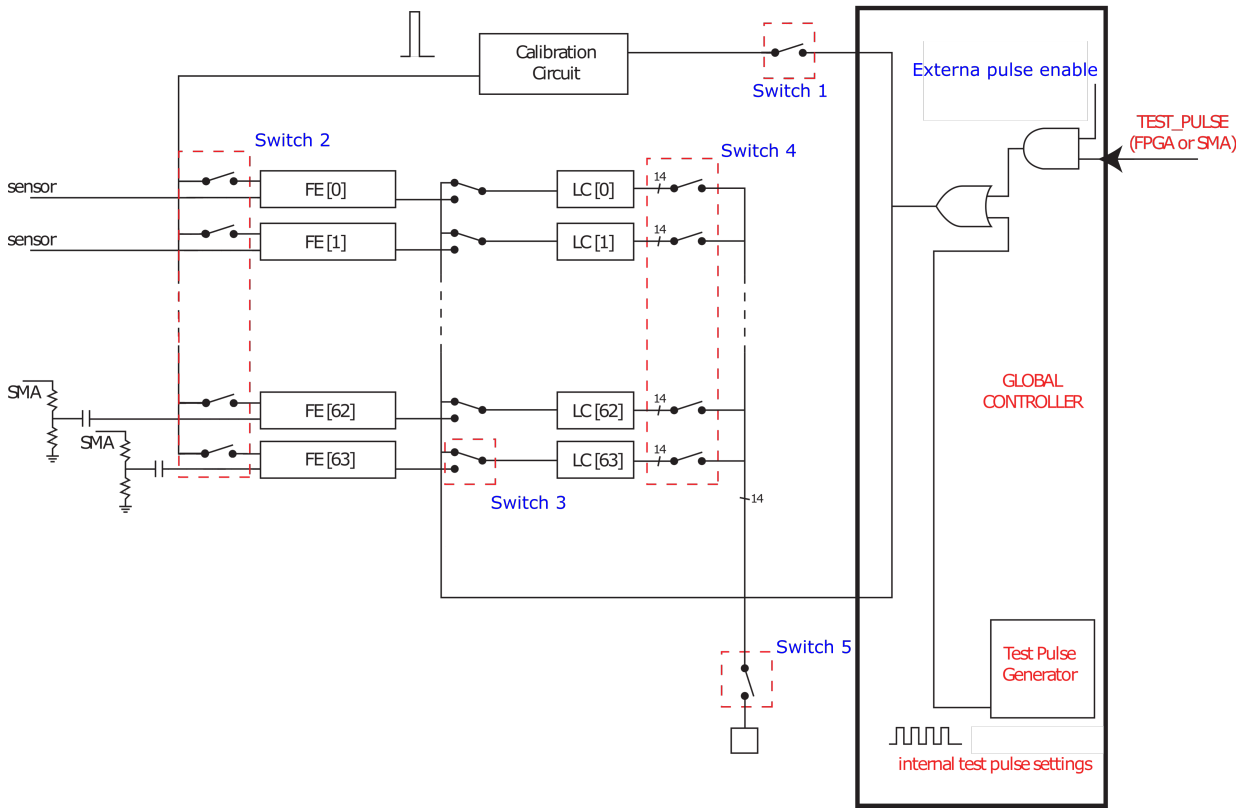


Figure 5.14: Schematic of the all possible test configurations in PASTA.

branch. "T Coarse" stores the time stamp of the main clock for each phase. For the first phases the "T Coarse" counter is fixed to 15 meaning that the leading edge of the test pulses falls into the 15th clock period. However, shifting the edge of the test pulses, it falls into the next clock cycle and the "T Coarse" is increased by one as expected.

"T EoC" measures the distance between the signal edge to the clock edge. According to the "T Coarse" behaviour, when the pulse gets closer and closer to the clock edge, the counts become smaller and smaller until the test pulse's edge crosses the clock edge. When this happens the "T Coarse" is increased by one, while the "T EoC" shows the maximum numbers of counts. Since the SOC is unique for the two branches, it is designed to wait a certain time window after the "E Coarse" before storing the corresponding clock cycles. Therefore, considering that in this configuration the triggering of the two branches is the same and the variation of the E corse is much smaller than expected for the normal operations, the SOC is always at the minimum value 48.

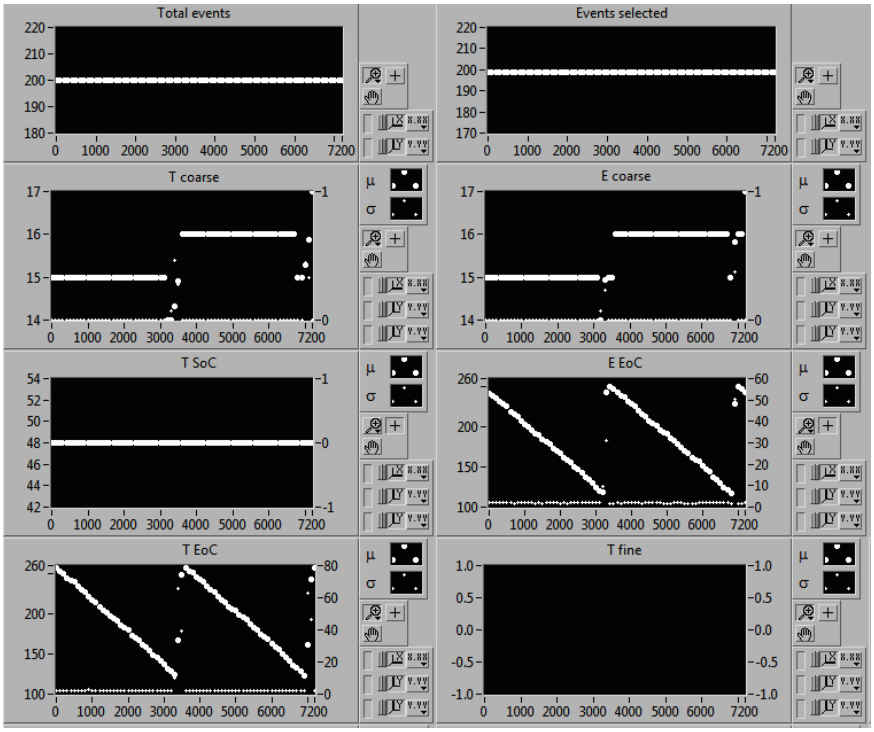


Figure 5.15: Measurement interface during the phase scan tests.

Once the scan is done, the first thing that is possible to analyse is the linearity of the TDC, measuring the linearity of the fine time (EOC-SOC). For the analysis only the data from the second ramp are taken. In this way, the entire TDC working range is scanned leading to a complete result. In Figure 5.16 the red dots represent the mean time measured for 200 pulses with the respective standard deviation, while the fit is the blue line. With a $\chi^2 = 5.95$ can be asserted that the behaviour of the TDC is linear.

From the previous data, it is also possible to measure the effective time bin of the TDC. As shown in Subsection 2.3.1.2, the time binning of the TDC is the ratio between the clock period and the interpolation factor 128, with a clock value of 160 MHz. The nominal value of the resolution is 48.8 ps.

The difference between the maximum time value and the minimum time value of the data reported in Figure 5.16 is the interpolation factor. From these data, it results that the interpolation factor is

130.18 $\pm$ 4.85, leading to a TDC binning of:

$$TDC\,bin = \frac{6.25\,ns}{(130.18 \pm 4.85)} = (48.01 \pm 1.78)\,ps \tag{5.1}$$

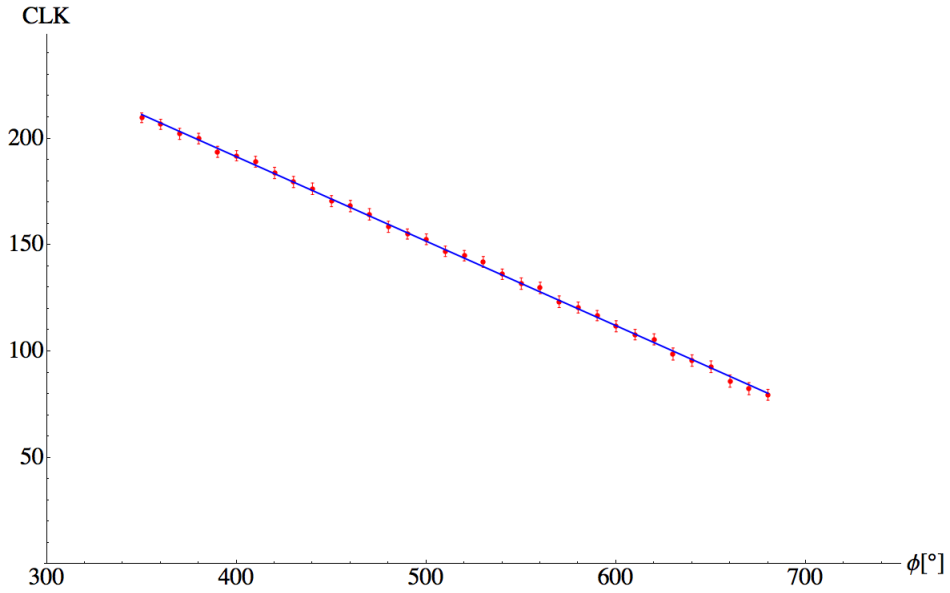


Figure 5.16: Linear fit represented in blue of the T Fine data shown with the red dots.

Using the TDC binning obtained it is possible to measure the quantisation error for each phase value. The quantisation error is given from the product of the TDC binning and the standard deviations of each point of the Figure 5.16. The mean value is $(124.19 \pm 4.63)\ ps$.
The last information obtained form this scan is the Differential NonLinearity (DNL) of the Wilkinson ADC used to determine the EOC. The DNL of each phase value is shown in Figure 5.17 where it can be seen that the maximum error within ± 2.2 LSB.

5.4.3 Front End measurements

For the Front End chain it was possible to perform two types of measurements: the evaluation of the noise and the linearity of the Font End chain. For these measurements the configuration where the test pulse is injected to the Front End and the TDC is connected to the Front End is used.
For the first characterisation it is necessary to perform a scan of the thresholds. As shown in Subsection 3.1.4, since the threshold is differential, it means that its value can be defined by changing the two parameters called "HDCDAC+" and "HDCDAC-". It is decided to keep the "HDCDAC-" at "0" while the positive one is scanned from "0" to "15" using a DAC. By design, the maximum range of the threshold it about $50\,mV$, leading to few difficulties during the S-curve measurement. For example, only the smallest signal can be used, the amplitude of the others is always above the maximum threshold. Moreover, since a hysteresis comparator has

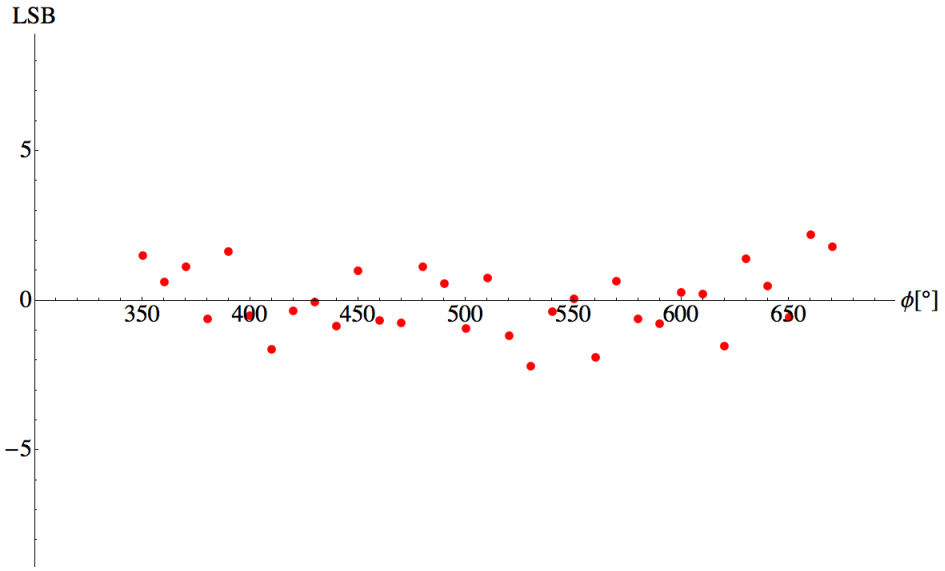


Figure 5.17: Results of the non-linearity of the Wilkinson ADC implemented in the TDC

two different threshold values, (Figure 3.9), if the value chosen for "HDCDAC+" is too close to "HDCDAC-" it is possible that the effective lower threshold is below to the baseline leading to an invalid event. In fact, under these conditions the comparator is not able to return to "0" after it fires when a signal crosses the highest threshold.

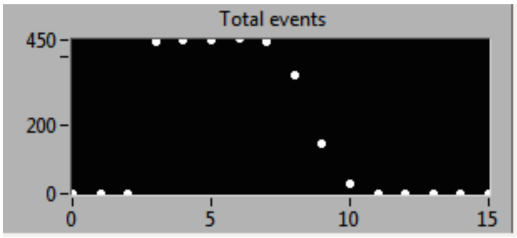


Figure 5.18: Events registered from the chip as a function of several threshold levels.

Figure 5.18 shows an example of the result of this scan. 450 pulses are sent to the Front End and the "Total Event" graph shows how many of them cross the threshold for different values of it. Below 3, the lower threshold of the hysteresis comparator is below the base line, so the chip doesn't respond.
After some optimisations it is possible to measure the noise level from the data of this type of scan. The data have to be fitted with an S-curve, the derivative of this curve has a gaussian shape, Figure 5.19. Its mean value is 18.88 mV and its sigma equal to 1.80 mV is the noise peak to peak. The resulting RMS noise is 0.30 mV.

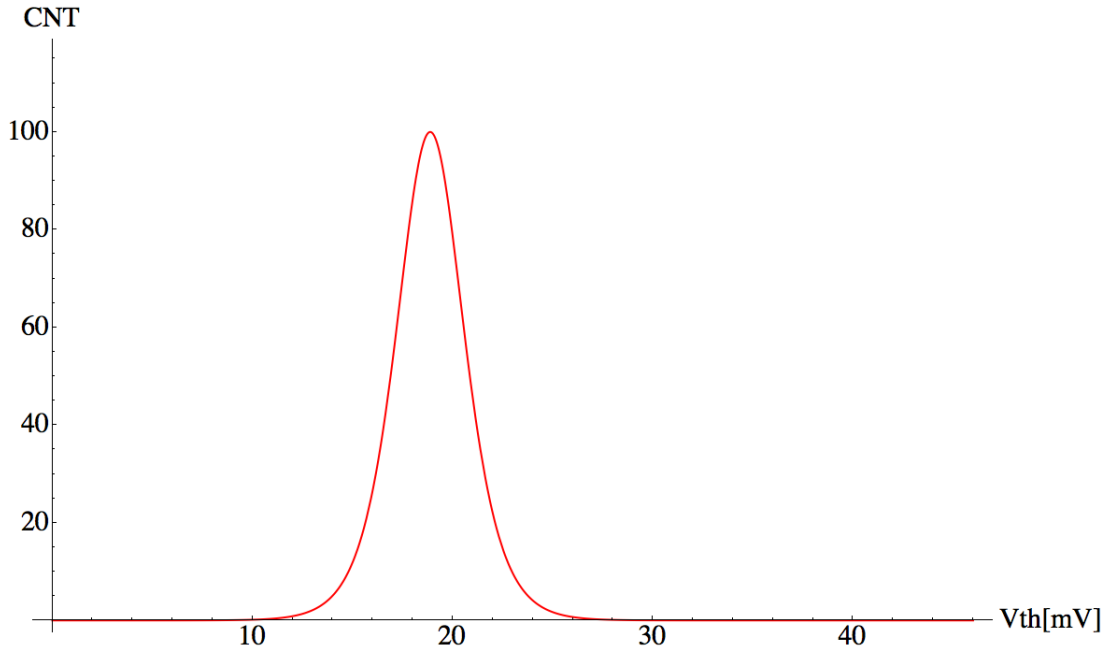


Figure 5.19: Derivative function of the threshold scan with an optimised Front-End: μ=18.88 mV, σ=1.80 mV.

The input signals used for the measurements is generated on chip by the global calibration circuit. It is designed to generate input signals with an amplitude and a shape similar to the ones coming from the silicon strips. For this analysis, as already mentioned, the smallest signal is used. By design it represents an input voltage generated by a charge of 1fC into the sensor. Of course it is not possible to assert that the signal thus generated corresponds to 1fC without a proper calibration. However, it is possible give a first estimation of the ENC under the assumption that the input signal used is equal to the one generated by 1fC. The resulting ENC is 387 e^-, without any sensor capacitance connected. This value is bigger respect the one estimated with the simulations. The simulations have been done for the schematic of the circuit without parasitic capacitors that are generated by the layout. Moreover, in the simulations the input signal is ideal without noise while in the tests, the tests pulses generated on chip are affected by jitter.

To measure the linearity of the Front End chain, a amplitude scan is performed to obtain the coarse ToT information as a function of the amplitude of the test pulse signal feeding the CSA. For simplicity only the coarse ToT that is given by the difference between “E coarse time” and

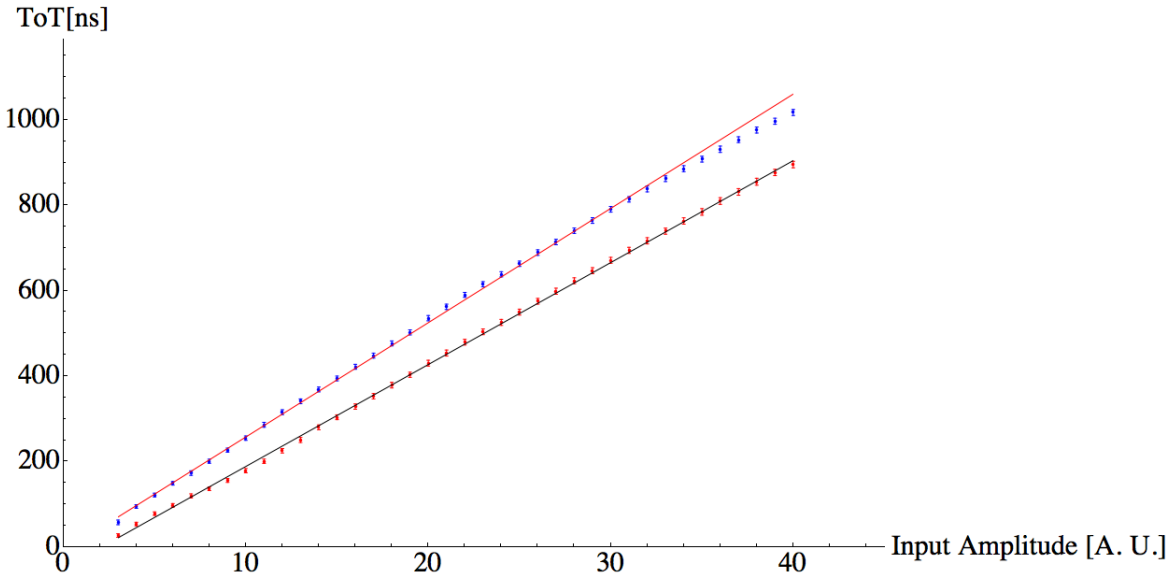


Figure 5.20: The blue (red) dots represent the ToT obtained as difference between "E coarse time" and "T coarse time", in the case of p-type (n-type) strips, as a function of several input amplitudes of the test pulse. The red (black) line is the best fit of the data. The last five points of p-type configuration are not taken into account for the linear fit because there is a compression of the points for high charges.

"T coarse time" is measured without the fine information given by the TDC circuits. The behaviour of the configuration for the p-type strips is shown in Figure 5.20. The blue points represent the coarse ToT while the red line is the best fit of the data, omitting the last five points since there is a compression for high charges as expected from simulations. With a χ^2 of this fit equal to 42.53 the behaviour for this configuration is linear.
In Figure 5.20 the linearity measurement is done for a n-type strip configuration. The red dots are the data of the Front End while the black line is the best fit. For this configuration, a lower ToT gain is expected. The linearity is kept also for high charges. The χ^2 is 41.00 meaning that also for this configuration the Front End chain has a linear behaviour.

6

CONCLUSIONS

The topic of this thesis was the development of a first prototype (full size) of a readout ASIC for the double-sided silicon micro-strips of the $\overline{P}ANDA$ Micro Vertex Detector (MVD) called PANDA STrip ASIC (PASTA) with a particular attention to the design of a Time to Digital Converter (TDC).

The main tasks of the MVD are: a primary vertex reconstruction, identification of secondary vertices of particles displaced a few hundreds of µm from the primary one, contribution to the particle momentum reconstruction and support to the particle identification.
Taking into account these tasks together with a continuous readout, since $\overline{P}ANDA$ is a trigger-less experiment with a system clock of 160 MHz, the PASTA requirements were defined. Therefore, it is important to have both a precise time stamp of the hit and an energy loss measurement. Time over Threshold (ToT) is the technique which allows to have both information with limited power consumption.
In the PASTA chip two thresholds are used to perform the ToT measurements: one is close to the base line in order to increase the precision of the time stamp while the second one is higher, reducing the energy measurement uncertainty due to noise fluctuations. The two thresholds are set separately in two different discriminators. The one featuring the lower threshold is called *Time Discriminator* while the other is called *Energy Discriminator.* The ToT is thus given by the time distance between the Discriminator Output Time branch (DOT) leading edge and the Discriminator Output Energy branch (DOE) trailing edge.
The clock pulse count achieves a resolution of one clock period, meaning 6.25 ns. Therefore, to increase the time resolution, an analog TDC circuit is implemented. The TDC is designed to measure the time distance between the leading (trailing) edge of DOT (Discriminator Output Energy branch (DOE)) and the next clock pulses leading edge. In this way, it is possible to achieve a time precision up to 48.8 ps.

The prototype includes: 64 channels (each channel features a Front End chain, two discriminators, two TDCs and a digital local controller that manages the TDC and pre-processes the data), a global controller (used to set all the configurations needed, to manage data from the 64 local controllers, and to pack the data before transmitting them), the biasing cells needed by the analog structures, a calibration circuit (used to test the Front End chain), and 10 LVDS drivers (6 inputs and 4 outputs).
The chip features are: power consumption $\leq 4mW/channel$, Front End noise $< 600e^-$ for an input capacitance of 25pF, maximum data rate capability 100 kHz/channel, time binning 50 ps to 400 ps, charge resolution 8bit (dynamic range), radiation tolerance up to 100 kGy, input clock frequency of 160 MHz, input capacitance 10 pF to 35 pF.
The chip was produced in 110 nm CMOS technology ad its final dimensions are $(3.4 \times 4.5)\ mm^2$ with input pitch 63 μm.
After the project submission a dedicated test board was designed: Digital Interface for Strip data Handling (DISH). Together with a Virtex ML605 evaluation board and two dedicated software packages it was possible to setup two data acquisition systems that have been used in test and characterisation measurements.

First of all the powering of the chip was tested, some minor issues were discovered and solved. The second step was the verification of the configurations sent to the chip. Then the characterisation phase of the analog architectures of a typical channel started. The TDC shows a good linearity that reflects the simulated behaviour. From the data, it was possible to calculate the binning time that results to $(48.01 \pm 1.78)\ ps$. This result leads to an estimation of $(124.19 \pm 4.63)\ ps$ as quantisation error. This value is not the real resolution of the TDC because it also includes the jitter of the injected test pulse.
As for the Front End chain, it was possible to perform several measurements with the internal test pulse, changing the input amplitude, in order to verify if the ToT has a linear trend. The measurements show a linear behaviour of the Front End chain for both input signals (the one that represents a signal coming from n-type strips and the one from p-type strips). The calibration of the input amplitude has to be done in the future, using radioactive sources and particle beam.
The estimation of the Front End noise is 0.3 mV RMS without any sensor input capacitance. Since the input test pulse is not yet calibrated, the noise in terms of electrons is just a rough estimation. It results to be $387\,e^-$. That it is a bit higher than the one expected from the simulations. One of the main reason for this disagreement is that the value of one of the currents into the preamplifier is only half with respect to the simulation due to a mistake during the DISH design.

However, a second version of the chip is needed for bug fixing of the issues of the first prototype described in this thesis and problems that could come out during the final characterisation. In addition, a study of radiation tolerance of this prototype has to be done with x-rays, to perform total ionising dose tests, and ions, to analyse single event effects.
A beam test of PASTA connected to a strip sensor is already planned for the first half of 2017, using protons of various energies, which allows an in-depth study of the performance of the ToT measurements and the chip rate capability.

A

PASTA USERS GUIDE

A.1 Description

The PASTA prototype version 1 is a $3.40 \times 4.50\, mm^2$ chip designed with the UMC 110nm CMOS technology. The prototype consists of 64 channels (analog front-end, analog TDC, digital channel controller), the digital global controller, 10 LVDS (6 inputs, 4 outputs), a calibration circuit, and all the necessary bias structures (except for the preamplifier and for the latched comparator). The pad ring is designed with two breaks, as is shown in Figure 1, in order to separate the analog and the digital power domains.

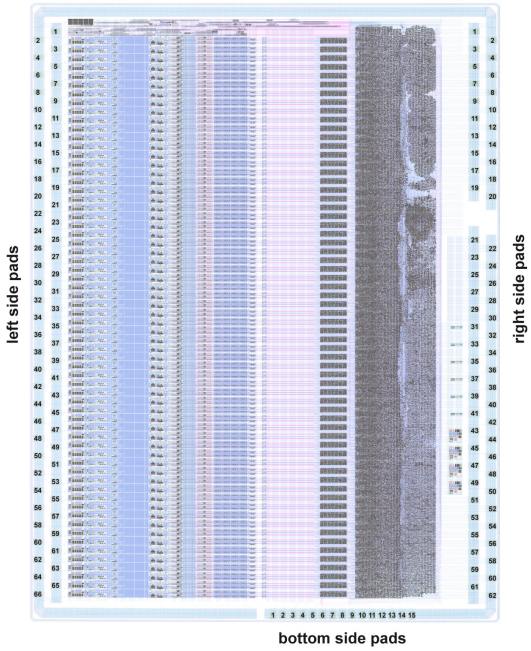


Figure A.1: PASTA Chip

A.2 PAD Layout

There are 143 pads in total:
- 66 pads on the **left side** starting form the top

Pad Number	Pad Name	Type	Description
1	PAD_TEST 0	Digital In	Pull-down to enable the [PAD_TEST 1]
2	PAD_TEST 1	Analog Out	ToT amplifier output for the Ch0
3-66	Ch[0:63]	Analog In	Channels input

Table A.1: Pads on the left side

- 15 pads on the **bottom side** starting from the left

Pad Number	Pad Name	Type	Description
1	DOT	Digital Out	Front-end comparator output (time branch)
2	DOE	Digital Out	Front-end comparator output (energy branch)
3	w_tcoarse	Digital Out	Flag for coarse time stamp (time branch)
4	w_ecoarse	Digital Out	Flag for coarse time stamp (energy branch)
5	r_soc	Digital Out	Flag for start of time to digital conversion
6	r_eoc_t	Digital Out	Flag for end of time to digital conversion (time branch)
7	r_eoc_e	Digital Out	Flag for end of time to digital conversion (energy branch)
8	ev_valid	Digital Out	Flag for a valid event
9-12	TAC_status[0:3]	Digital Out	If "0" TAC is free, if "1" TAC is busy
13	Comp_out_T	Digital Out	Latched comparator output (time branch)
14	Comp_out_E	Digital Out	Latched comparator output (energy branch)
15	playload_r	Digital Out	Last bit of the internal control link shift register*

Table A.2: Pads on the bottom side

*Enables to see if incoming data through the ASIC control link are recognized as such

- 62 pads on the **right side**

Pad Number	Pad Name	Type	Description
		Analog Section	
1	VBG	Vbias	External reference voltage for the bias cells (600mV)
2	CSA_IB2	Vbias	External reference current for the bias for the preamplifier (800μA)
3	Vref	Vbias	External reference voltage for the latched comparator threshold (850mV)
4-8	AVDD[0:4]	Power	Analog power supply (1.2V)
9-13	AGND[0:4]	Ground	Analog ground level (0V)
14-18	AVSS[0:4]	Substrate	Analog substrate voltage (0V)
19	AGNDIO	Substrate	Analog substrate voltage for the pad ring (0V)
20	AVDDIO	Power	Analog power supply for the pad ring(1.2V)
		Digital Section	
21-25	DVDDIO[0:4]	Power	Digital power supply for pad ring and LDVS 2.5V)
26-30	DGNDIO[0:4]	Ground	Digital substrate voltage for pad ring and ground level for LDVS (0V)
31	Test_Pulse -	LVDS In	Input for the external Test Pulse
32	Test_Pulse +	LVDS In	Input for the external Test Pulse
33	SYNC_RST -	LVDS In	Synchronous reset
34	SYNC_RST +	LVDS In	Synchronous reset
35	CLK_I -	LVDS In	Main clock (160MHz)
36	CLK_I +	LVDS In	Main clock (160MHz)
37	SDI -	LVDS In	Serial configuration data input
38	SDI +	LVDS In	Serial configuration data input
39	SCLK -	LVDS In	Serial clock (10MHz)
40	SCLK +	LVDS In	Serial clock (10MHz)
41	CS -	LVDS In	Chip select for configuration
42	CS +	LVDS In	Chip select for configuration
43	CLK_O -	LVDS Out	Main clock output to synchronize the serial data output
44	CLK_O +	LVDS Out	Main clock output to synchronize the serial data output
45	TX0 -	LVDS Out	Serial serial data output, first line
46	TX0 +	LVDS Out	Serial serial data output, first line
47	TX1 -	LVDS Out	Serial serial data output, second line
48	TX1 +	LVDS Out	Serial serial data output, second line
49	SDO -	LVDS Out	Serial configuration data output
50	SDO +	LVDS Out	Serial configuration data output
51-54	DVSS[0:3]	Substrate	Digital substrate voltage (0V)
55-58	DGND[0:3]	Ground	Digital ground level (0V)
59-62	DVDD[0:3]	Power	Digital power supply (1.2V)

Table A.3: Pads on the right side

A.3 Chip Configuration

The PASTA configuration is done via the ASIC Control Link (SCLK, CS, SDI, SDO). The SCLK is required to start at least one clock cycle before the CS goes high. The SDI pin can be shared with other ASICs while the SDO must be connected individually for each chip.
The data for the chip configuration follows the structure reported below:
- 4 bit (command)
- 7 bit (channel address, if necessary)
- N bit (data, if necessary)
- CRC-8 (8 bits)

Each part must be preceeded by the MSB, the default CRC-8 is "10001010" while the divider polynomial is $x^8 + x^2 + x + 1$ (100000111).
The available commands are summarized in Table A.4 (channel configuration) and in Table A.5 (global configuration), along with the length of the corresponding data.

Command	Address	Data Length		CRC-8	Description
		N_{wr}	N_{rd}		
0000	Required	42	42	Required	Write channel configuration
0001	Required	-	42	Required	Read channel configuration
0010	Required	1	1	Required	Write channel test configuration
0011	Required	-	1	Required	Read channel test configuration
0100	Required	-	10	Required	Read channel counter

Table A.4: Commands for the local configuration

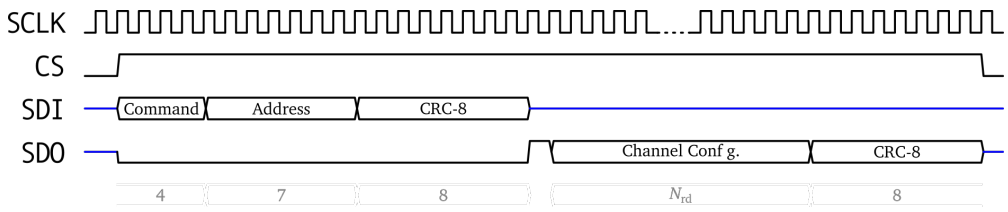


Figure A.2: Example of a reading command for the local configuration [78].

Command	Address	Data Length		CRC-8	Description
		N_{wr}	N_{rd}		
1000	-	172	1	Required	Write global configuration
1001	-	-	172	Required	Read global configuration
1010	-	26	26	Required	Configure internal test pulse
1011	-	-	10	Required	Read global counter
1100	-	14	1	Required	Write global test congfiguration
1101	-	-	1	Required	Read global test congfiguration

Table A.5: Commands for the global configuration

In the previous table there are two different values for the data length: N_{wr} and N_{rd}. N_{wr} is the number of bits to be written into a register for a successful transfer. However, for N_{rd} the meaning changes depending on whether a read or write command is issued. For a read command, this number represents the number of bits that are read, while for a write command it represents the number of clock cycles it is necessary to wait in order to have the command fully processed.
How the string of local configuration bits looks like is shown in Figure A.2, while in Figure A.3 the string for a global configuration is shown.

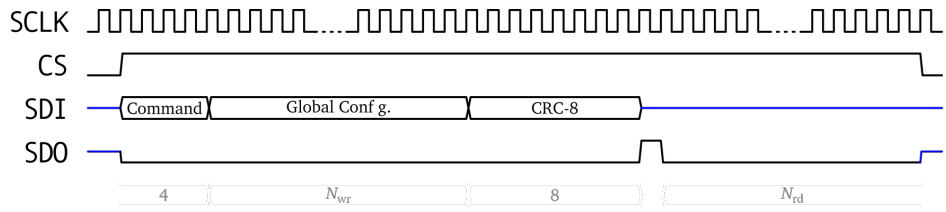


Figure A.3: Example of a write command for global configuration [78].

A.3.1 Local Configuration

The channel configuration includes a set of registers that can be programmed for each channel of the chip. This allows a fine tuning of the parameters. Every channel command is described with the default values, it is important to notice that the default values are not the values of the chip after a power-cycle. They have to be tuned for each chip during the test phase in order to obtain the simulated behavior.

- **Local configuration**

The parameters of each channel can be set. The definition of the 42 bits of this register is reported in Table A.6 with their default values.

- **Channel test configuration**

1 bit that controls the calibration of the channel. If it is set to "0" calibration is inhibited. If it is set to "1" the front-end amplifier is connected to the calibration circuit. The default value is "0".

- **Channel counter**

With this command it is possible to read the counter enabled in the channel configuration.There are severl counters that can keep track of : SEU, refresh signals, missed signals, discared events, dark events, and valid events. It is possible to count none (all deactivated), only one, or more than one simultaneously. In this case, the different individual trigger signals will be combined with a logic OR, thus increasing the counter for any of the activated triggers. However, the information of which trigger increased the counter is lost.

Position	Description	Default
	Analog Configuration	
41	finish configuration	0
40:37	"Iref_ratio_e" Fine tuning of the TDC's discharging current (energy branch)	1010
36:33	"Iref_ratio_t" Fine tuning of the TDC's discharging current (time branch)	1010
32:28	"HCLDAC_e" Front-end comparator threshold (energy branch)	00000
27:23	"HCLDAC_t" Front-end comparator threshold (time branch)	00000
22:18	"If" Fine tuning of the feedback current of the ToT amplifier	10000
	Digital Configuration	
17	Enable delay line (time branch)	1
16	Enable counting of SEUs	0
15	Enable counting of refresh signals	0
14	Enable counting of missed signals	0
13	Enable counting of discarded events	0
12	Enable counting of dark events	0
11	Enable counting of valid events	1
10:9	Delay for the "stop charging" signal expressed in clock cycles	00
8:7	Length of the synchronization chain	01
6	Enable parallel Fip-Flop	1
5	Use hit validation in energy branch in prediction mode	1
4	Enable prediction mode	1
3:2	Trigger mode	00
1	Enable test mode to use test pulse instead of discriminator outputs	0
0	Enable channel	1

Table A.6: Default values for the channel configuration

A.3.2 Global Configuration

- **Global configuration**

This command is used to set several parameters that influence the functionalities of the whole ASIC. Digital values are shown in Table A.7, while analog values are shown in Table A.8,

Position	Description	Default
31	Enable the [CLK_O]	1
30	Enable the test pattern mode for serial data output lines	0
29	If "1" a "high" CS acts as a veto and will disable all channels	0
28	Define the data transmission mode: if "1" full mode, if "0" compact event mode	1
27	Enable counting of SEUs in the global controller	0
26	Enable counting of truncated events due to a full frame buffer	0
25	Enable counting of missed events due to a full event buffer	0
24:21	Counting interval for the channel counter, range from 2^{10} ("0000") to 2^{25} ("1111") clock cycles	0000
20:13	Subtraction value t_offset for the fine counter in compact event mode	x"00"
12	Mode of the finetime counter : if "1" will saturate, if "0" will wrap around*	0
11	Enables clock gating for TDC read logic	1
10	Enables clock gating for TDC write logic	0
9:8	Clock divider	00
7:4	Sets TAC refresh period from 2^{12} ("0001") to 2^{26} ("1111") clock cycles. "0000" deactivates it	0011
3	Enable the "test_pulse" for all channels	1
2	If "0" [TX] is single data rate, if "1" it is double data rate	0
1:0	Set TX mode : If "00" only [TX0], if "01" also [TX1], if "11" sends a training pattern	00

Table A.7: Default values for the global configuration (digital settings)

*This bit is useful only if the Compact event mode is activated

Position	Description	Default
	Analog TDC Configuration	
171:167	"ILSB" Set the reference current for the fine tune of the "Iref_ratio_e\t"	01001
166:162	"Iref_cs" Set the refence current for the current generator of the analog TDC	01101
161:157	"Vcas_p" Cascode voltage for the pmos transistors in the TACs	10010
156:152	"Vcas_n" Cascode voltage for the nmos transistors in the TACs	10000
151:147	"Comp_Vcas" Cascode voltage for the latched comparator	11001
146:142	"Comp_Vb" Bias voltage for the latched comparator	01011
	Front-End Amplifier Configuration	
141:137	"BLR_Ib" Bias current for the baseline restorer	11110
136:132	"BLR_Vcas" Cascode voltage for the baseline restorer	10110
131:127	"CB_Ib1" Bias current for the input stage of the current buffer	01110
126:122	"CB_Ib2" Bias current for the output stage of the current buffer	10101
121:117	"CB_Vbias" Bias voltage for the input stage of the current buffer	01010
116:112	"CSA_Ib1" First bias current for the charge sensitive amplifier's input stage	01101
111:107	"CSA_IbSF" Bias current for the source follower of the charge sensitive amplifier's output stage	10111
106:103	"HCGDAC−" Reference voltage for the negative input of the hysteresis comparator	1001
102:99	"HCGDAC+" Reference voltage for the positive input of the hysteresis comparator	1111
98:94	"HC_Ib1" Bias current for the first stage of the hysteresis comparator	01000
93:89	"HC_Ib2" Bias current for the second stage of the hysteresis comparator	01110
88:84	"HC_Ib3" Bias current for the third stage of the hysteresis comparator	01000
83:79	"IfDAC_Ilsb" Current for the LSB of the channel ToT feedback current DAC	01101
78:74	"IfDAC_Imin" Reference current for the channel ToT feedback current DAC	10101
73:69	"PREAMP_Ifn" Input base current (n-type strip)	01110
68:64	"PREAMP_Ifp" Input base current (p-type strip)	01110
63:59	"PREAMP_Ishift" Shift of the preamplifier's output voltage (n-type strip configuration only)	10001
58:54	"PTA_Ibn" Bias current for peaking time adjuster stage (n-type strip)	01110
53:49	"PTA_Ibp" Bias current for peaking time adjuster stage (p-type strip)	01110
48:44	"PTA_Ibuf" Buffer current for peaking time adjuster stage (n-type strip configuration only)	10101
43:39	"ToT_Ib" Bias current for the ToT amplifier	01110
38:33	"Vbl" Baseline voltage	011111
32	"FSWITCH" Input signal polarity: "0" n-type strip configuration "1" p-type strip configuration	0

Table A.8: Default values for the global configuration (analog settings)

- **global test configuration**

This command is used to access the calibration circuit controlling the amplitude of the pulse and the channel to test (Table A.9).

Position	Description	Default
13:8	Channel address which is connected to the bottom pads	000000
7	Enable the probing of key signals going from selected channel to the output pads	0
6:1	DAC settings for the pulse amplitude	111111
0	Enable the calibration circuit	0

Table A.9: Default values for the Write global test configuration

- **configure internal test pulse**

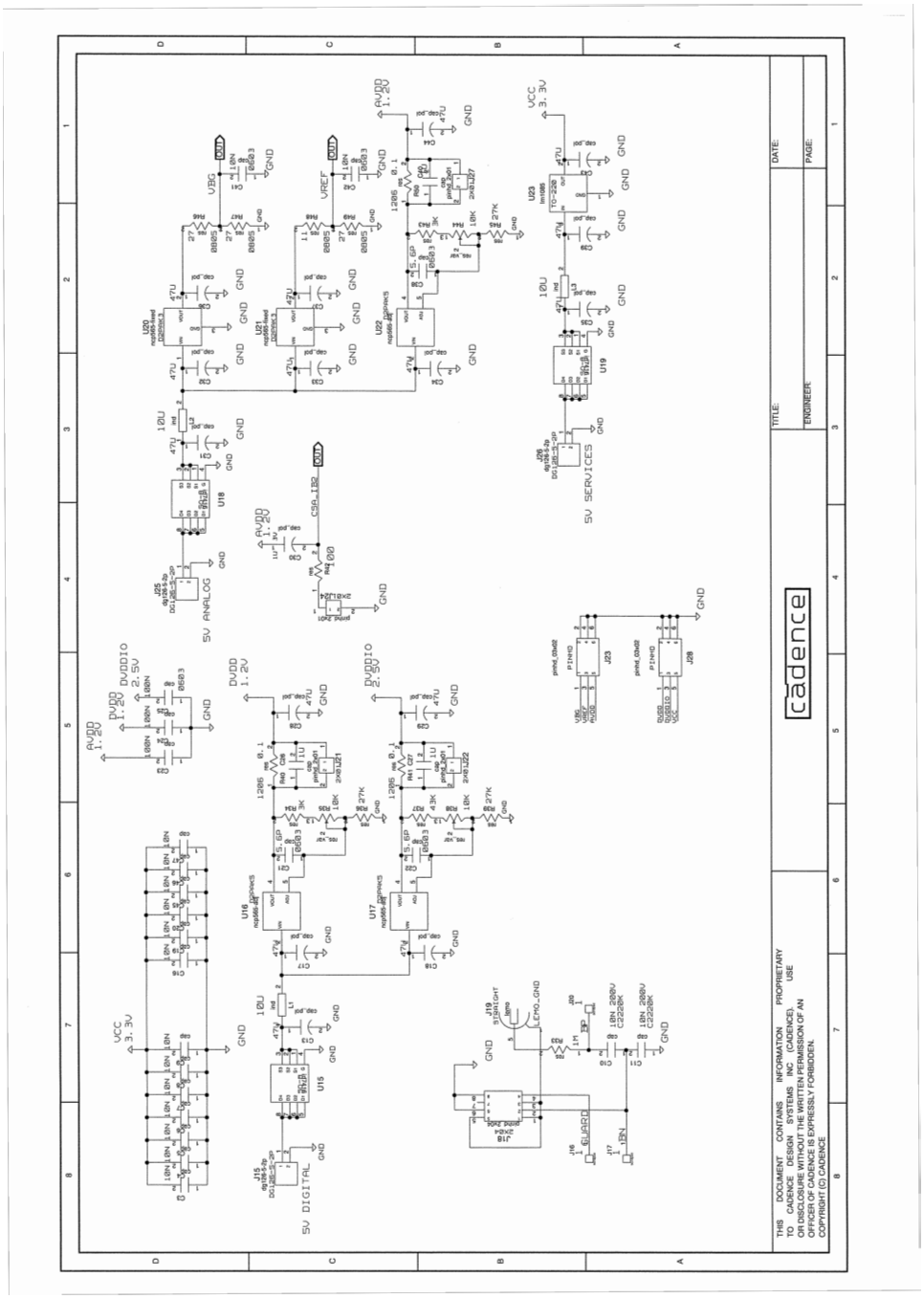
The test pulse can be injected in two different part of the chip: directly into the TDC circuit or at the input of the front end part. It is possible to choose between the two configurations by adjusting the bit in position 1 of the channel configuration register (see Table A.6).
This command is used to set some parameters of the test pulse. In particular the test pulse module will generate N+1 pulses, each one having a length of L+1 clock cycles and separated by $128 \times (S + 1)$ clock cycles. The way how to set these parameters is shown in Table A.10.

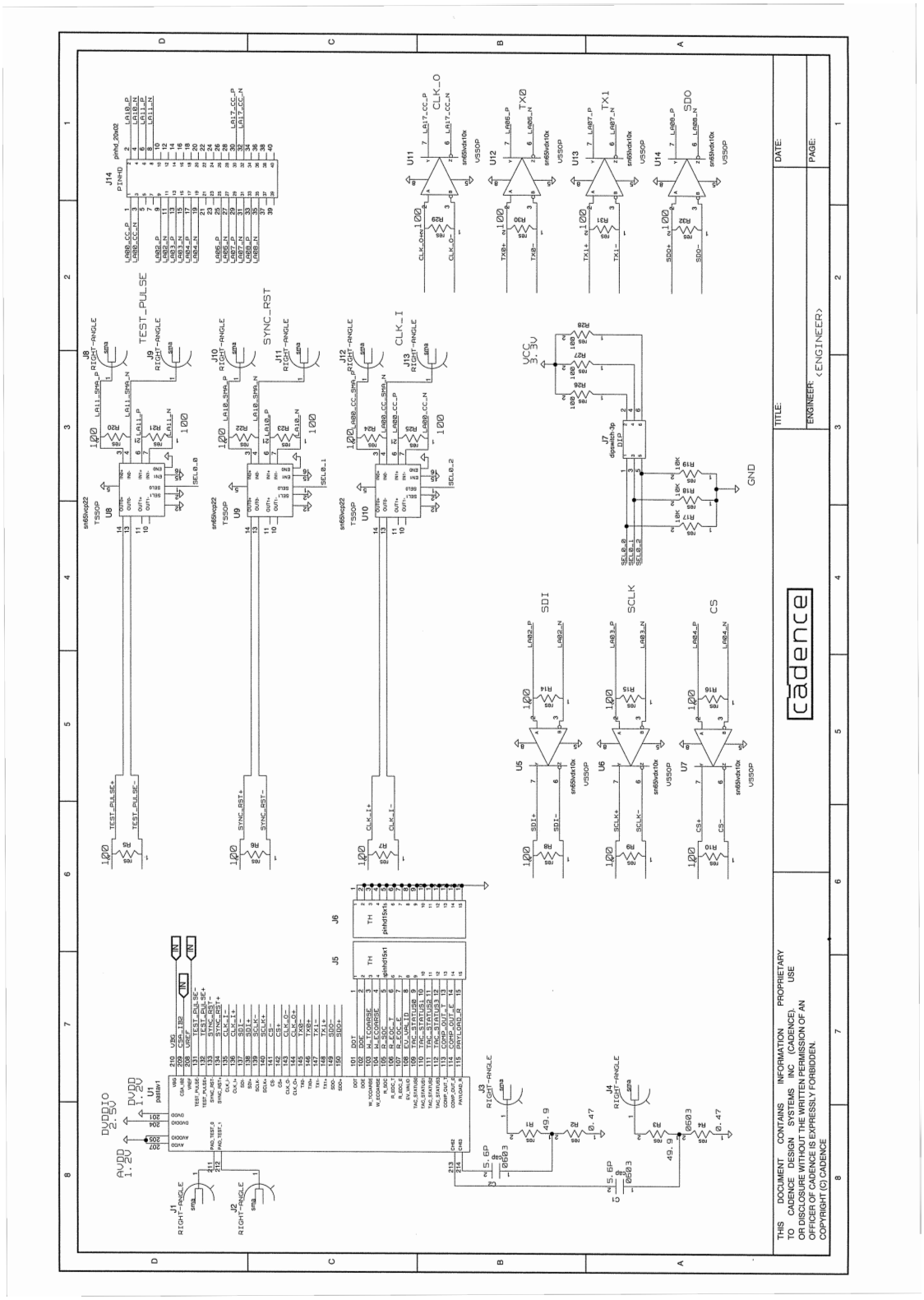
Position	Description
25:18	S, Pulse spacing
17:10	L, Pulse length
9:0	N, Number of pulses

Table A.10: Settings for the test pulse generator

B

DISH SCHEMATICS




TEST_PULSE
SYNC_RST
CLK_I
CLK_O
TX0
TX1
SDO
SDI
SCLK
CS
GND
VCC 3.3V
DVDD 2.5V
AVDD 1.2V
cadence
TITLE:
DATE:
ENGINEER: <ENGINEER>
PAGE:
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LIST OF ACRONYMS

ADC Analog to Digital Converter

APPA Atomic, Plasma Physics and Applications

ASIC Application-Specific Integrated Circuit

CBM Compressed Baryonic Matter

ChPT Chiral Perturbation Theory

CR Collector Ring

CRC Cyclic Redundancy Check

CS Chip Select

CSA Charge Sensitive Amplifier

DIRC Detection of Internally Reflected Cherenkov light

DISH Digital Interface for Strip data Handling

DNL Differential NonLinearity

DOE Discriminator Output Energy branch

DOT Discriminator Output Time branch

DRC Design Rules Check

DUT Device Under Test

EFT Effective Field Theories

EMC ElectroMagnetic Calorimeter

ENC Equivalent Noise Charge

EOC End Of Conversion

ESD ElectroStatic Discharge

FAIR Facility for Antiproton and Ion Research

FPGA Field Programmable Gate Array

FS Forward Spectrometer

GBTX Gigabit Transceiver ASIC

GDP Generalized Parton Distributions

GEM Gas Electron Multiplier

GSI GSI Helmholtzzentrum für Schwerionenforschung GmbH

HESR High-Energy Storage Ring

HV-MAPS High-Voltage Monolithic Active-Pixel Sensors

JDRS Jülich Digital Readout System

LHC Large Hadron Collider

LQCD Lattice Quantum ChromoDynamics

LSB Least Significant Bit

LVS Layout Vs Schematic

MCP-PMTs Micro-channel plate photomultiplier tubes

MDC Module Data Concentrator

MDT Mini Drift Tube

MMB MVD Multiplexer Board

MSB Most Significant Bit

MVD Micro Vertex Detector

NuSTAR Nuclear Structure, Astrophysics and Reactions

PASTA PANDA STrip ASIC

PANDA Antiproton ANnhilation at DArmstadt

PB Power Board

PEX Post-layout EXtraction

QCD Quantum ChromoDynamics

QGP Quark-Gluon Plasma

RICH Ring Imaging Cherenkov

RESR Recuperated Experimental Storage Ring

SCLK Serial CLocK

SciTil Scintillator Tile

SDI Serial Data Input

SDO Serial Data Output

SiPMs Silicon Photomultipliers

SOC Start Of Conversion

STT Straw Tube Tracker

TAC Time to Amplitude Converter

TDC Time to Digital Converter

ToPix Torino Pixel

ToF Time of Flight

TOFPET Time of Flight for Positron Electron Tomography

ToT Time over Threshold

TS Target Spectrometer

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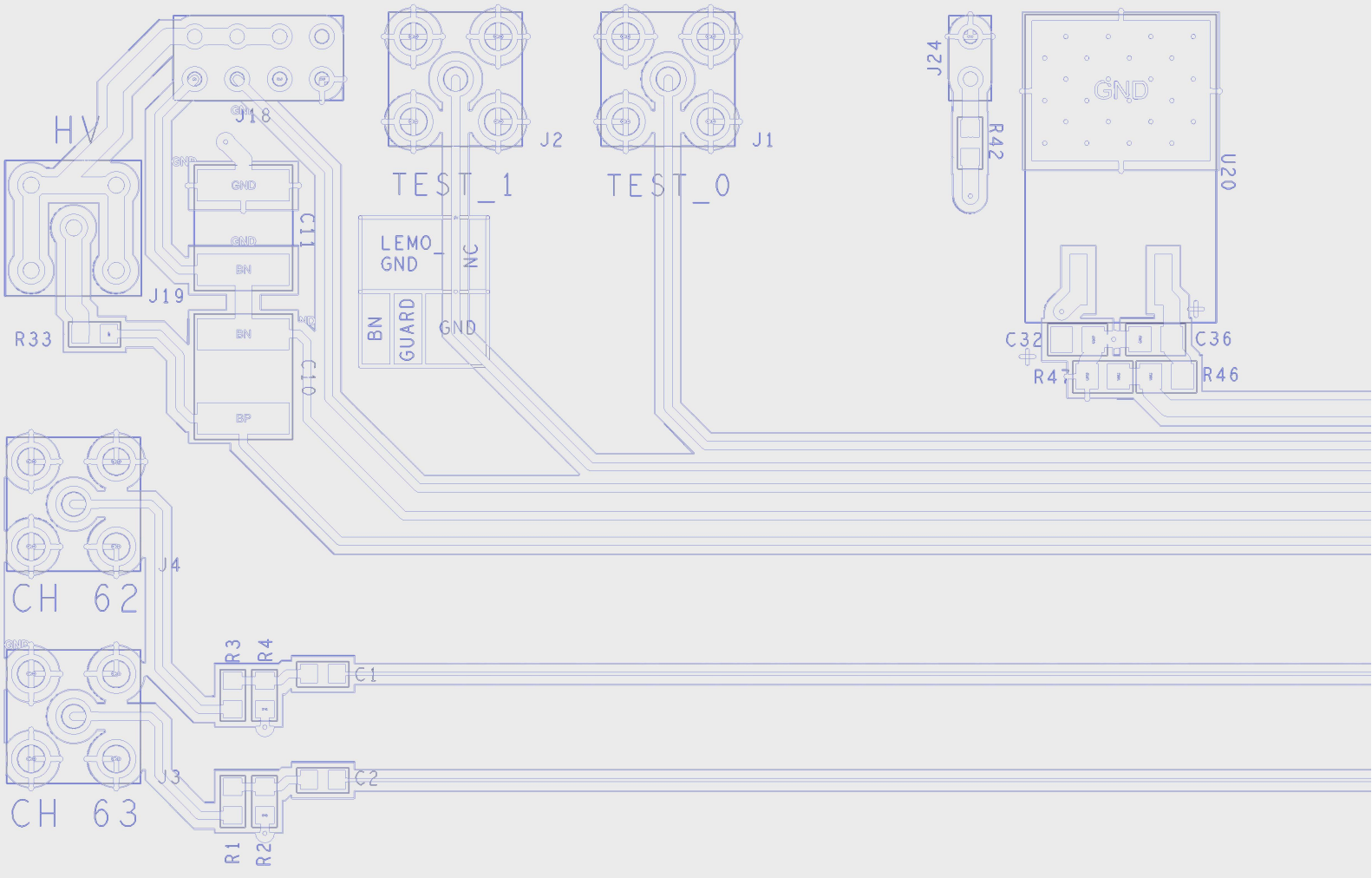
ERKLÄRUNG DER URHEBERSCHAFT

Ich erkläre: Ich habe die vorgelegte Dissertation selbständig und ohne unerlaubte fremde Hilfe und nur mit den Hilfen angefertigt, die ich in der Dissertation angegeben habe. Alle Textstellen, die wörtlich oder sinngemäß aus veröffentlichten Schriften entnommen sind, und alle Angaben, die auf mündlichen Auskünften beruhen, sind als solche kenntlich gemacht. Bei den von mir durchgeführten und in der Dissertation erwähnten Untersuchungen habe ich die Grundsätze guter wissenschaftlicher Praxis, wie sie in der "Satzung der Justus-Liebig-Universität Gießen zur Sicherung guter wissenschaftlicher Praxis" niedergelegt sind, eingehalten.

Gießen, Januar 2017

Alberto Riccardi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J2
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J1
TEST_0
J24
R42
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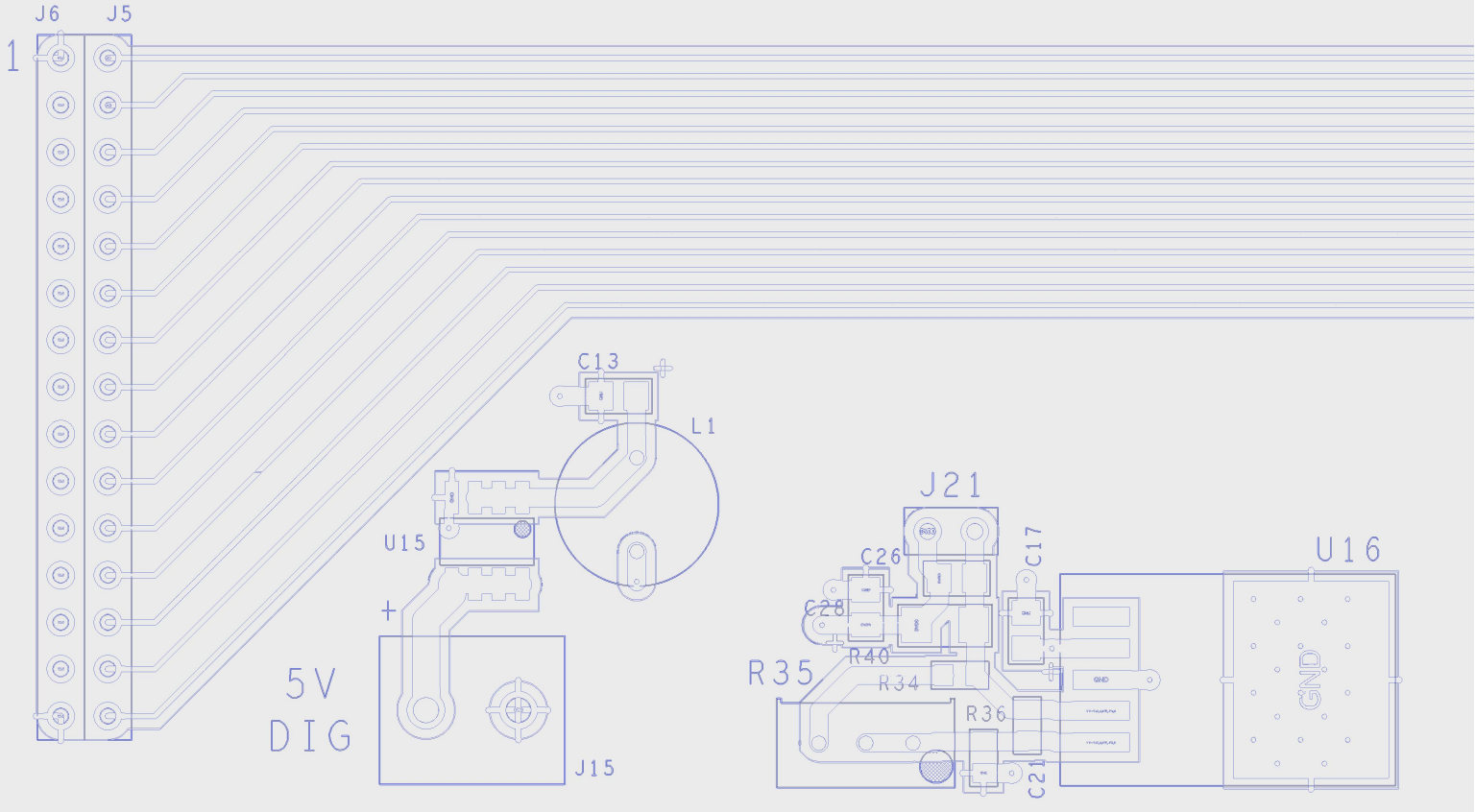
U20
GND
GND
BN
C11
J19
R33
BN
C10
BP
LEMO_
GND
NC
BN
GUARD
GND
C32
C36
R47
R46
J4
CH 62
GND
R3
R4
C1
J3
CH 63
C2
R1
R2


J6
J5
1
C13
L1
U15
+
5V
DIG
J15
J21
C26
C17
C28
R40
R35
R34
R36
C21
U16
GND