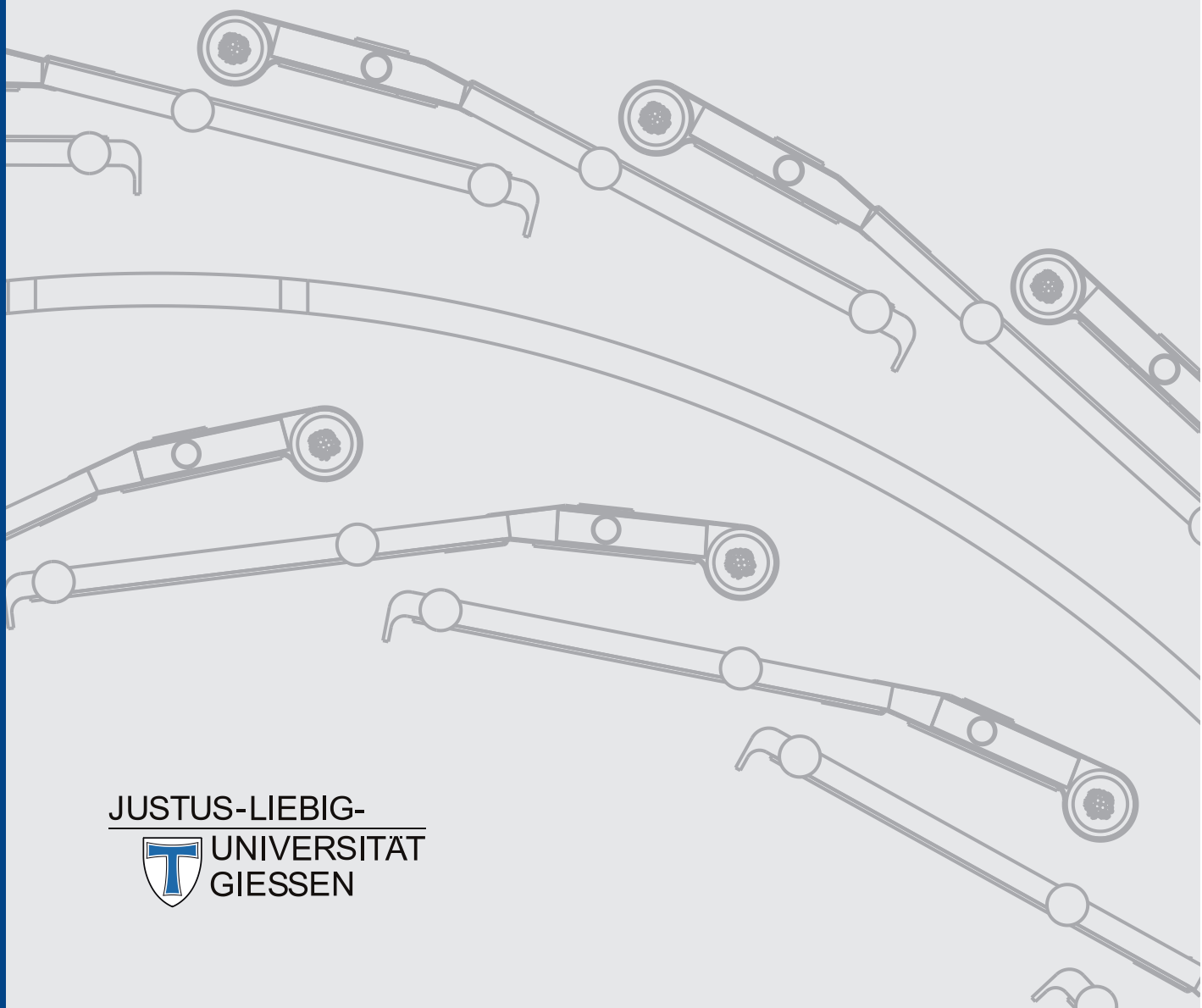
Tommaso Quagli

Hardware Developments for the Strip Detector of the $\overline{\text{P}}$ANDA MVD

Dissertation



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Hardware Developments for the Strip Detector of the $\overline{\text{P}}$ANDA MVD

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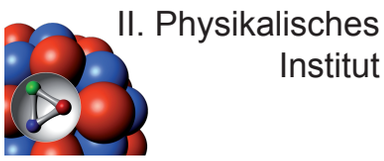

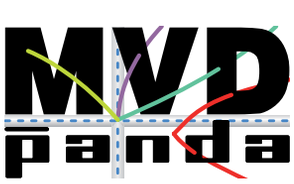

Tommaso Quagli, *Hardware Developments for the Strip Detector of the $\overline{P}$ANDA MVD*

Inaugural-Dissertation zur Erlangung des Doktorgrades (Dr. rer. nat.) im Fachbereich 07 (Mathematik und Informatik, Physik, Geographie) der Justus-Liebig-Universität Gießen.

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In loving memory of F. A.

ABSTRACT

$\overline{\text{P}}$ANDA is a key experiment of the future FAIR facility, under construction in Darmstadt, Germany. It will study the collisions between an antiproton beam with momenta between 1.5 GeV/*c* and 15 GeV/*c* and a fixed proton or nuclear target, allowing to study the QCD at intermediate energies.

The Micro Vertex Detector (MVD) is the innermost part of the tracking system of the experiment and its main task is the precise spatial identification of primary and secondary vertices. It will be composed of four concentric barrels and six forward disks, instrumented with silicon hybrid pixel and double-sided silicon microstrip detectors.

The work of this thesis is centered on the hardware development of the strip barrel staves. The general concept of the staves is briefly introduced, along with the description of the main sensitive elements and of the carbon fiber mechanical support. The tools and methods for the characterization of strip sensors, with a selection of results from three prototype runs, are presented. The setup designed to study the radiation hardness of the strip sensors has also been used to conduct systematic studies on epitaxial diodes for the pixel part of the MVD. Finally, the last chapter is devoted to the electro-mechanical integration of the barrel staves and describes the developments towards a supporting flexible printed circuit, the validation of the stave cooling system and an extensive evaluation of the powering and cabling scheme of the full MVD.

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1

THE $\overline{\text{P}}$ANDA EXPERIMENT

The $\overline{\text{P}}$ANDA experiment [1, 2] is one of the key projects at the future Facility for Antiproton and Ion Research (FAIR), currently under construction in Darmstadt, Germany, next to the site of the present GSI Helmholtzzentrum für Schwerionenforschung GmbH [3]. Once completed, the new facility will feature a complex system of accelerators which will deliver proton, antiproton and ion beams for a wide range of experiments for basic research and applied science.

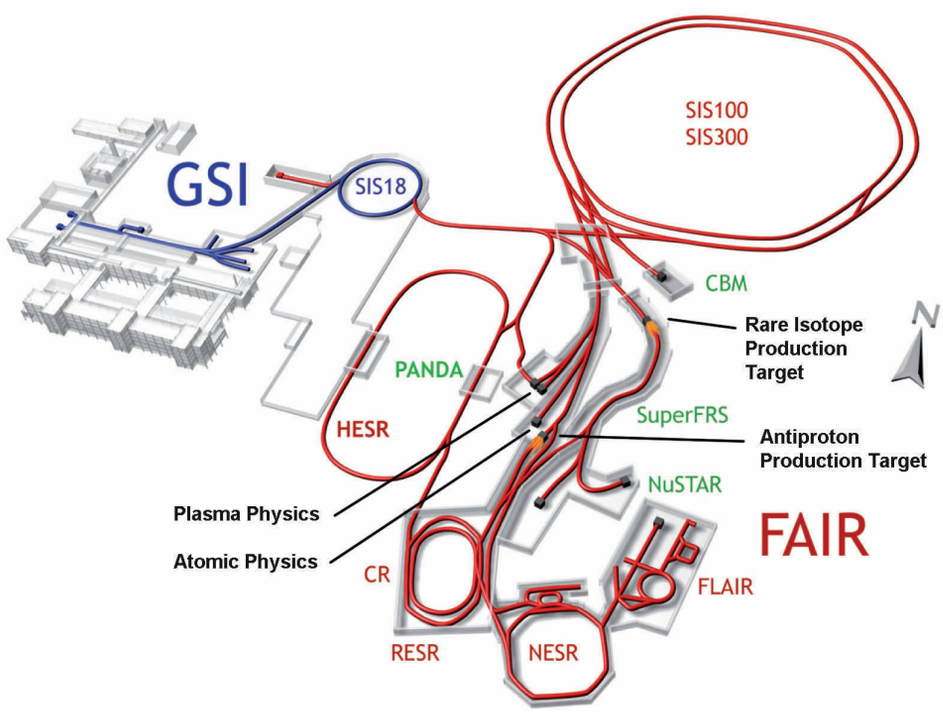


Figure 1.1: Layout of FAIR; in blue the existing facility and in red the new one. The sites of the main experiments are also shown.

The varied scientific program of FAIR consists of 14 different experiments, resting on four main pillars [4]:

- APPA: Atomic, Plasma Physics and Applications;
- CBM: Compressed Baryonic Matter;

- NuSTAR: Nuclear Structure, Astrophysics and Reactions;
- $\overline{\text{P}}$ANDA: antiProton ANnihilation at DArmstadt.

The FAIR facility will use part of the existing accelerators at GSI which will be upgraded and employed to inject the beams in the new structures (see figure 1.1). A new dedicated proton LINAC will accelerate the protons up to 70 MeV [5] and inject them in the upgraded SIS18. Here the protons will be accelerated up to an energy of 4 GeV, before being injected in the main element of the new accelerator system, SIS100. This is a superconducting synchrotron ring with a maximum magnetic rigidity of 100 Tm and a circumference of approximately 1100 m [6]. For the production of antiprotons, SIS100 will deliver a pulsed proton beam with bunches of about $2 \cdot 10^{13}$ protons at a maximum energy of 29 GeV.

The protons will impinge on the antiproton production target, which is a 11 cm long copper or nickel rod [7]; the antiprotons are cooled to a momentum of 3.82 GeV/c and injected in the Collector Ring (CR) and then in the High Energy Storage Ring (HESR). Further upgrades foresee an intermediate storage in the Recuperated Experimental Storage Ring (RESR) in order to increase the antiproton beam intensity [8]. The HESR, where the $\overline{\text{P}}$ANDA experiment will be located, will deliver the final antiproton beam to the experiment, with momenta between 1.5 GeV/c and 15 GeV/c and a peak luminosity in the order of $2 \cdot 10^{32}$ cm^{-2}s^{-1} (further details on the operation of the HESR are given in section 1.2.1).

The broad physics program of $\overline{\text{P}}$ANDA, which is presented in section 1.1, will be explored by means of studying annihilation reactions of antiprotons with protons and nuclei [9]. The $\overline{\text{P}}$ANDA detector, designed to achieve this goal, is presented in the second part of this chapter (section 1.2).

1.1 THE PHYSICS PROGRAM OF $\overline{\text{P}}$ANDA

The Quantum Chromodynamics (QCD), the quantum field theory of quarks and gluons, is the accepted theory of the strong interaction. At high energies, where the coupling constant α_S is small (e.g. $\alpha_S(M_Z) = 0.1185 \pm 0.0006$ [10]) and perturbation calculations can be applied, the theory is very well understood and has been extensively tested [11, 12, 13, 14]. However, in the low energy, non-perturbative region, the experimental knowledge is rather limited and there is not a common theoretical framework capable of making quantitative predictions. With the availability of high resolution antiproton beams and at the intermediate energies available ($\sqrt{s} = 2.25 - 5.47$ GeV), $\overline{\text{P}}$ANDA could be a key instrument to answer some of the open questions of non-perturbative QCD.

As demonstrated by the LEAR experiment at CERN [15, 16] and by the E760/E835 experiments at Fermilab [17, 18], antiproton experiments are a particularly suited instrument to study a wide range of QCD topics. Due to the additional degree of freedom given by the annihilation of the three valence quarks in the proton with the three antiquarks in the antiproton, many interesting states (e.g. quarkonia, flavorless mesons with a quark and its antiquark as constituents) can be formed directly in $\bar{\text{p}}$p annihilations. In contrast, e^+e^- annihilations, while providing a cleaner measurement environment, are limited to the formation of states with the virtual photon quantum numbers ($J^{PC} = 1^{--}$).

The direct formation of a resonance allows to study its properties by changing the energy available in the initial state. The parameters under study (for example the line shape of the resonance) can be

reconstructed as a function of the initial state energy by measuring a reaction rate while adjusting the beam momentum, scanning around the resonance peak. This scanning technique, used for the first time by the E835 experiment [19], allows to study resonances with greater precision than in traditional production experiments. The resolution on the reconstructed parameters depends mostly on the knowledge on the initial state energy, i.e., on the beam spread, and not on the resolution of the detector. In $\overline{\text{P}}$ANDA, the HESR will offer a high resolution operation mode which will allow to control the beam momentum with a precision of $\delta p / p = 10^{-5}$, which can provide a resolution in the order of 30 keV [20].

The $\overline{\text{P}}$ANDA physics program is articulated in several pillars: hadron spectroscopy, in-medium modifications of hadrons, study of the nucleon structure and hypernuclear physics. An overview of the particles which could be potentially produced at $\overline{\text{P}}$ANDA is shown in figure 1.2.

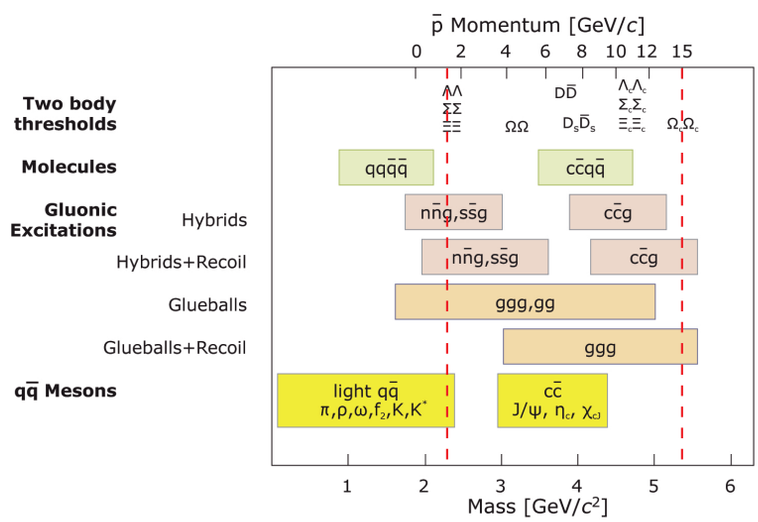


Figure 1.2: Overview of the accessible states in $\bar{\text{p}}$p annihilations as a function of the invariant mass and of the antiproton momentum. The range accessible to $\overline{\text{P}}$ANDA is indicated with red lines [21].

1.1.1 *Hadron spectroscopy*

1.1.1.1 *Charmonium spectroscopy*

Despite its first state being discovered more than 40 years ago in two indepentent experiments at BNL [22] and SLAC [23], the spectrum of the charmonium, i.e., a $c\bar{c}$ bound system, still holds several open questions.

The charmonium spectrum, apart from the scale, is much alike to the spectrum of the positronium (a bound state of an electron and a positron). This suggests that the description of the charmonium in the framework of the strong interaction could be similar to that of the positronium in the electroweak theory, implying the presence of a $1/r$ Coulomb-like potential in addition to a linearly rising confinement part.

However, the finer details of the spectrum cannot be explained in this first coarse approximation. Model calculations can be performed within different theoretical models, such as effective field theories and Lattice QCD (LQCD). In the last decades, the charmonium states have been mostly studied through e^+e^- and $\bar{p}p$ experiments. Many states which don't fit in any theoretical predictions have been observed, while many predicted states have not yet been found [24]. Thanks to its higher luminosity and momentum resolution and to a better detector, $\overline{\text{P}}$ANDA will represent a significant improvement compared to the Fermilab experiments E760 and E835 and will offer an opportunity to shed new light on the subject.

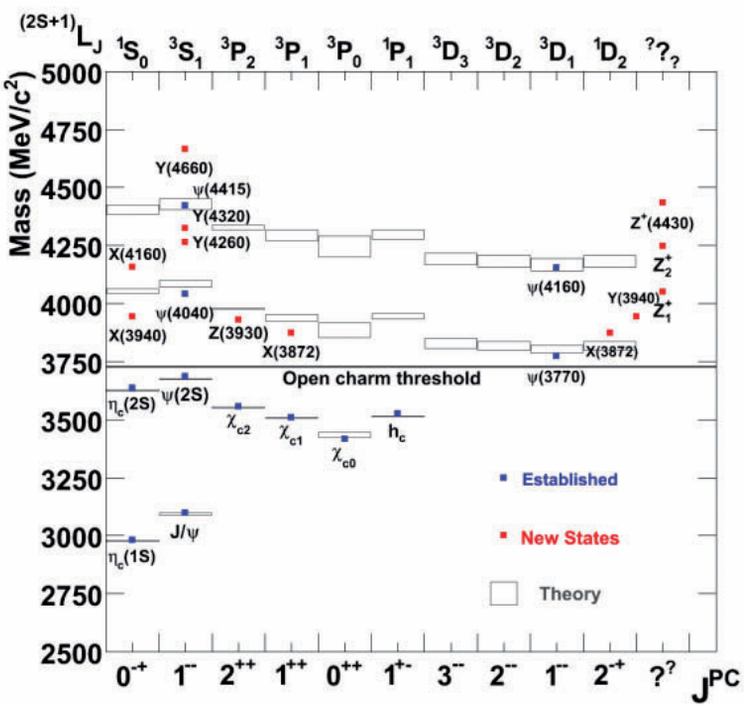


Figure 1.3: Charmonium spectrum with possible quantum numbers assignment in the mass range 1.5 – 5.0 GeV/c^2 [21].

The spectrum of the predicted and measured charmonium states is shown in figure 1.3. Eight states below the $D\overline{D}$ threshold (3.73 GeV) are experimentally established [10]; some of them (for example the J/ψ and the $\psi(2S)$) are measured with great accuracy, while others (especially the singlet states) still lack precise experimental data. The spectrum above the open charm threshold is much denser: besides a few established states observed by different experiments at electron-positron colliders, several new charmonium-like states, usually labelled X, Y and Z, were found recently at the B-factories [25]. Because of their quantum numbers assignment, charge or decay modes, the explanation of these states is not univocal. Several interpretation are considered, ranging from conventional $c\bar{c}$ states, to tetraquarks (multiquark state of four tightly bound quarks in a diquark-diantiquark structure), molecules (two charged mesons weakly bound by the exchange of a gluon or of a pion) and hybrids (states carrying gluonic degrees of freedom). For instance the X(3872), observed in various experiments with a mass very close to the DD^* threshold [26, 27, 28, 29], has been suggested to be a molecular or tetraquark

state; recent studies [30] have determined unambiguously its quantum numbers to be $J^{PC} = 1^{++}$. The Y(4260), observed by Babar [31] and later confirmed by CLEO [32] and Belle [33], is another example of an established status which lacks an univocal interpretation, while the $Z_c(3900)$, observed in 2013 by BESIII [34] and Belle [35], is a strong candidate for the tetraquark interpretation.

1.1.1.2 *Search for exotic states*

The existence of hadrons with gluonic degrees of freedom is a possibility foreseen in the QCD. Two categories of states can be distinguished: hybrid states, where in a $q\bar{q}$ bound state the gluons carry additional excitation degrees of freedom, and purely gluonic states, called glueballs. Any of these states, thanks to the additional degrees of freedom added by the gluons, could carry exotic quantum numbers which are forbidden for hadrons within the Standard Model.

In the simplest interpretation, hybrids consists of a $q\bar{q}$ pair to whom an intrinsic gluonic excitation is added. The most promising evidence of hybrids comes from antiproton-proton experiments such as those at the LEAR facility [36, 37]. Hybrids in the charm sector are expected to be in the mass region between 3 and 5 GeV/c^2, where they could be identified unambiguously. Since only non-exotic hybrids can be obtained through formation from antiproton-proton annihilation, the strategy envisaged to look for exotic hybrids is to use the highest available beam momentum and search for them in production processes [9].

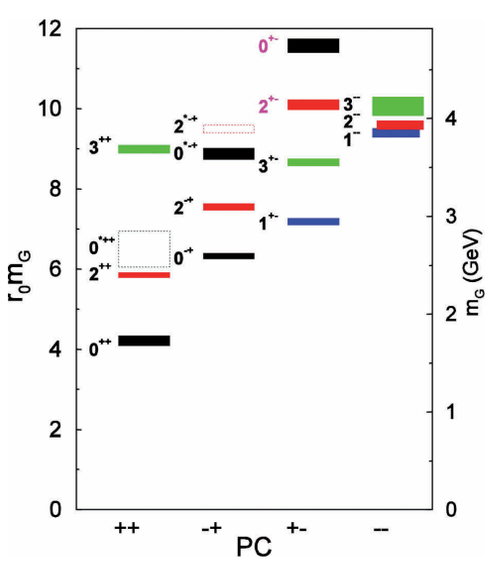


Figure 1.4: Spectrum of the glueballs predicted by LQCD calculations [38].

For what concerns glueballs, LQCD calculations predict about fifteen states, most of which with a mass in the region accessible at HESR [38]. The spectrum of glueballs predicted by LQCD is shown in figure 1.4. Glueballs with exotic quantum numbers, which are called oddballs, have a narrow width since they cannot mix with mesons and they should be easier to measure experimentally [39]. According to LQCD, the lightest oddball should have $J^{PC} = 2^{+-}$ and a mass of 4.3 GeV/c^2 [40], which is well within the range accessible to $\overline{\text{P}}$ANDA. Heavier oddballs, with a mass above the open charm

threshold, are expected to have a much larger width because of the many decay modes available and will therefore be much more difficult to identify.

1.1.1.3 *Charmed and strange baryons*

The understanding of the excited spectrum of baryons is an important goal of non-perturbative QCD. While a lot of experimental data about the nucleons is available, the agreement with the theoretical prediction from the quark models is poor [41]. However, for strange and charmed baryons the experimental data is sparse and the additional flavor content complicates the interpretation of the results.

Thanks to its 4π acceptance, particle identification and tracking detectors, $\overline{\text{P}}$ANDA can give a significant contribution to the spectroscopy of heavy baryons. The predicted cross section of several resonances, such as those of the Ξ, are large enough to make an experimental study feasible [42, 43]. Additionally, the decays of $\bar{\text{p}}\text{p}$ into $\Omega\overline{\Omega}$, $\Lambda_c\overline{\Lambda_c}$ or $\Sigma_c\overline{\Sigma_c}$ could be measured for the first time, allowing for the determination of their formation cross section [44].

Due to their short lifetimes, the detection of heavy baryons requires the reconstruction of their decay patterns. The presence of an advanced tracking system capable to detect displaced secondary vertices is therefore a crucial requirement for these studies.

1.1.2 *In-medium modification of charmed mesons*

The modification of the properties of the hadrons in the nuclear matter has been the subject of many studies. When produced in a medium, the mass of hadrons can be shifted as a result of a modification of the chiral symmetry breaking pattern of QCD due to the finite density [45]; the width is also expected to become larger, because some new decay channels, which are unavailable in vacuum, become open. In-medium effects are particularly significative for hadrons at rest or at low momenta.

Proton-nucleus, photon-nucleus, or nucleus-nucleus collisions have been used to study the mass shift of in-medium hadrons in the light quark sector. The antiproton-nucleus collisions available at $\overline{\text{P}}$ANDA can be used to study this topic also for charmed hadrons. For instance, an in-medium mass splitting between $\overline{\text{D}}$ and D mesons of about 100 MeV [46] and a downward shift of the $\text{D}\overline{\text{D}}$ average mass by about 50 MeV [47] were predicted.

Different experimental methods were proposed to study the D meson splitting, such as subthreshold production of D and $\overline{\text{D}}$ mesons in antiproton-nucleus collisions [46], or by using the DN and $\overline{\text{D}}$N interaction in $\bar{\text{p}}\text{d}$ collisions, with the spectator nucleon in the deuteron as secondary target [48].

Because of the high mass of the charmed mesons, the experimental conditions necessary to study in-medium modifications are hard to achieve. Therefore, these measurements are in principle experimentally feasible at $\overline{\text{P}}$ANDA, but they will require further theoretical studies and a thorough understanding of the experimental capabilities of the detector [9].

Antiproton-nucleus collisions at $\overline{\text{P}}$ANDA can also provide information on other topics, such as the $\text{J}/\psi\text{N}$ dissociation cross section, which is still almost unknown. This is closely related to the study of quark-gluon plasma (QGP) in ultra-relativistic nucleus-nucleus collisions [49].

1.1.3 *Hadron structure - Electromagnetic processes*

$\overline{\text{P}}$ANDA will allow for several experiments to study the nucleon structure. While the electromagnetic form factor of the nucleon has been thoroughly explored for space-like momentum transfers, with antiproton-proton annihilations it is possible to measure also the form factor in the time-like region, i.e., with a momentum transfer $q^2 \geq 0$. The reconstruction of the $p\bar{p} \to e^+e^-$ and $p\bar{p} \to \mu^+\mu^-$ processes will allow to determine separately $|G_E|$ and $|G_M|$ in a wide time-like transferred q^2 momentum range [50, 51].

The Drell-Yan processes, where a $q\bar{q}$ pair annihilates to create a lepton pair, could be an excellent tool to study the transverse distribution of the partons within the nucleon [52].

Finally, the Generalised Parton Distributions (GPDs), which are used to treat hard exclusive lepton scattering, can be studied through the reactions $p\bar{p} \to \gamma\gamma$ and $p\bar{p} \to \pi^0\gamma$ [53, 54].

1.1.4 *Hypernuclear physics*

Hypernuclei are nuclei where a nucleon is replaced by a hyperon, i.e., a nucleon where at least one up or down quark is substituted by a strange quark. Hyperons bound in the nucleus (e.g. Λ baryons) are not bound by the Pauli exclusion principle and can therefore assume many nuclear states unavailable to protons and neutrons. For this reason, they can be a useful tool to probe the nuclear structure and its modifications due to the presence of the hyperon; on the other hand, the properties of the hyperons can be modified by the surrounding nuclear medium [55]. Hypernuclear physics represents therefore an interesting topic with important consequences in the fields of nuclear, particle, many-body and astrophysics [56, 57].

At $\overline{\text{P}}$ANDA, hypernuclei will be studied using the reactions $p + \bar{p} \to \Xi^-\bar{\Xi}^+$ and $\bar{p} + n \to \Xi^-\bar{\Xi}^0$ and a dedicated experimental setup [58, 59]. The Ξ^- will be rescattered in the primary target and stopped in a secondary target, where double-Λ hypernuclei will be produced and detected. The γ-rays from the de-excitation of the hypernuclei will be detected by an array of high purity germanium detectors. Further details on the dedicated experimental setup for hypernuclear physics will be given in the relevant section (1.2.3.6).

1.2 THE $\overline{\text{P}}$ANDA DETECTOR

To explore the broad physics program presented in the previous section, the $\overline{\text{P}}$ANDA experiment requires a multi-purpose detector able to detect through various subsystems a wide range of charged and neutral particles over the almost full solid angle. The system must feature an excellent vertex and momentum resolution and must be capable of handling the high particle rate arising from the expected $2 \cdot 10^7$ $\bar{\text{p}}$p annihilations per second. Finally, it should be possible to modify the detector setup in order to perform some of the studies in the varied physics program (e.g. hypernuclear physics).

To satisfy these requirements, $\overline{\text{P}}$ANDA detector consists of two parts:

- the target spectrometer, based on a solenoidal magnet surrounding the interaction region and able to detect particles at large polar angles;
- the forward spectrometer, based on a dipole magnet and designed to detect particles at small polar angles in the forward direction.

1.2.1 *The antiproton beam*

The antiproton beam for the $\overline{\text{P}}$ANDA experiment is prepared and stored in the HESR [60]. This is a racetrack shaped ring composed of two straight sections 155 m long and two 180° arcs, for a total circumference of 575 m (see figure 1.5).

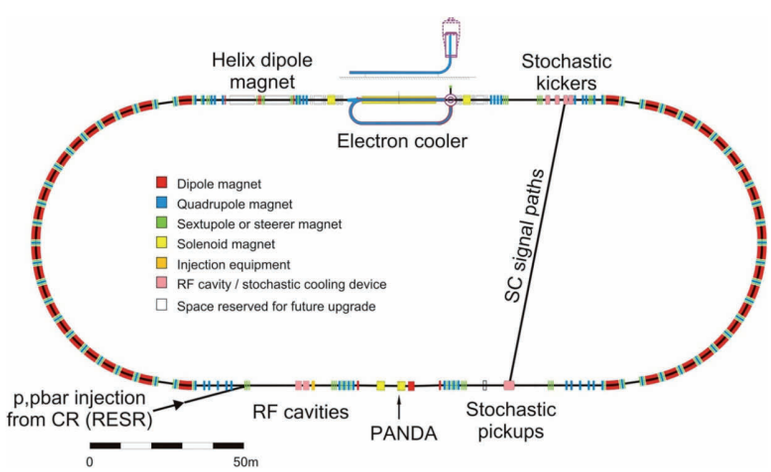


Figure 1.5: Layout of the HESR, used to store and deliver the antiproton beam used in $\overline{\text{P}}$ANDA [61]. The antiprotons are injected from the left in the lower straight section, where $\overline{\text{P}}$ANDA is located. The cooling systems and the HESR magnets are also indicated.

$\overline{\text{P}}$ANDA is located on one of the two straight sections. In order to compensate for the beam deviations induced by the $\overline{\text{P}}$ANDA magnets, two dipoles are placed before and after the experiment.

The accelerator foresees two different modes of operation [62]:

- High luminosity mode (HL), where the maximum luminosity of $2 \cdot 10^{32}$ cm^{-2}s^{-1} with 15 GeV/c antiprotons can be achieved; in this setup, the momentum spread is limited to $\delta p/p = 10^{-4}$.
- High resolution mode (HR), designed to reach a superior momentum resolution of $\delta p/p = 10^{-5}$; in this case, a maximum luminosity of $2 \cdot 10^{31}$ cm^{-2}s^{-1} can be achieved with 8.9 GeV/c antiprotons.

Two different cooling systems are available at HESR: an electron cooler, placed in the straight section opposite to $\overline{\text{P}}$ANDA [63], and a stochastic cooler with four kickers and the corresponding pick-ups on the opposite sides of the two straight sections [64].

1.2.1.1 *Luminosity considerations*

The interaction rate R, which determines the achievable number of particles in any physically interesting channel, is given by the product of the luminosity L with the total hadronic cross section σ_H. In order to evaluate the average luminosity with respect to the target value ($2 \cdot 10^{32}$ cm^{-2}s^{-1} in the HL operation mode), the beam intensity as well as the target density must be taken into account.

The antiprotons are injected in HESR at discrete time intervals. An injection cycle t_{cycle} can be therefore divided in the data taking time t_{exp} and the preparation time t_{prep}, when the target is off [62]. A sketch of the luminosity profile within an injection cycle is shown in figure 1.6.

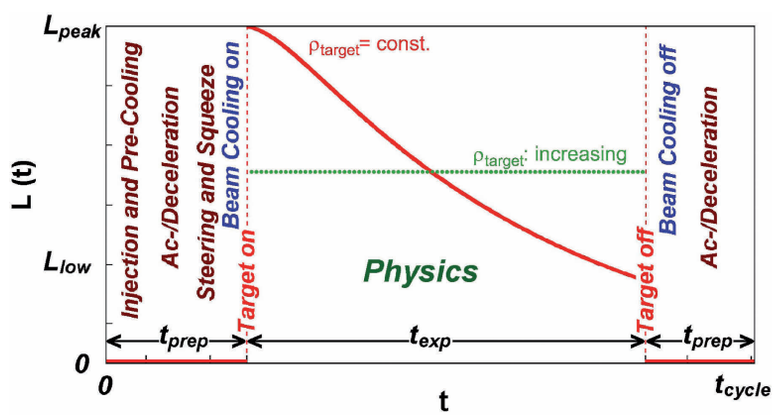


Figure 1.6: Schematic view of the luminosity profile $L(t)$ in one operation cycle for constant (solid red) and increasing (green dotted) target density ρ_{target}.

The beam intensity is not constant within an injection cycle, but decreases exponentially because of hadronic interactions, single Coulomb scattering and energy straggling of the beam circulating in HESR. If the target density is constant, then the luminosity decreases with the same exponential trend. On the other hand, a target with an adjustable density (as it is the case for the cluster jet system of $\overline{\text{P}}$ANDA described in section 1.2.2) can be used to compensate the beam intensity loss and to keep the luminosity as constant as possible.

To increase the luminosity, the residual antiprotons after each cycle are kept in the storage ring and mixed with the newly injected particles. To achieve this, a bucket-barrier system is used: the beam structure leaves an empty bucket of 10% of the orbit length for the injection of the new particles.

The average luminosity is therefore only 90% of the instantaneous one. Furthermore, the presence of a discrete time structure in the target, such as in the pellet target of $\overline{\text{P}}$ANDA, can introduce other fluctuations in the luminosity and increase significantly the peak values [65].

Taking into account these considerations and the machine parameters, a nominal interaction rate of $R_{\text{nom}} = 2 \cdot 10^7\, s^{-1}$ is defined as the event rate that every detector of the experiment must be able to handle [66].

1.2.2 *The target system*

Most of the $\overline{\text{P}}$ANDA physics program will study collisions of the antiproton beam with a proton target. Two solutions have been envisaged in order to provide this target: a cluster jet and a pellet system [67]. The physics program and the desired luminosity require a minimum effective target density of $4 \cdot 10^{15}$ hydrogen atoms per square centimeter; both technical options are being developed in order to meet this requirement.

The cluster jet target consists of a narrow supersonic jet of hydrogen clusters. A pressurized cooled gas is injected in vacuum through a nozzle; the gas condensates immediately forming a narrow jet of clusters, each with an average of $10^3 - 10^6$ hydrogen molecules. A good focussing of the antiproton beam can be used to define very precisely the interaction region in the directions perpendicular to the beam axis. On the contrary, in the antiproton beam direction the uncertainty on the definition of the interaction region is significantly higher (several millimeters) and arises from the lateral spread of the cluster jet. The main advantage of the cluster jet target is that it provides a very homogeneous and continuous target density. Additionally, the target density can be varied during operation, in order e.g. to compensate for the beam intensity losses during the HESR cycle. A prototype with the actual $\overline{\text{P}}$ANDA dimensions and geometry was built and reached an effective target density of $1.5 \cdot 10^{15}$ hydrogen atoms per square centimeter [68].

In the pellet target technique, a cryogenic liquid is injected through a thin nozzle into a gas of the same element close to its triple-point. A piezoelectric transducer applied on the nozzle breaks the jet into a series of droplets. The drops pass through a thin capillary into vacuum; during this phase their temperature decreases by a few degrees because of surface evaporation and the droplets become frozen pellets. The main advantages of this technique are the high effective target density that can be reached and a better determination of the interaction zone with respect to the cluster jet solution. The spatial resolution can be further improved by means of reconstructing the position of individual pellets with an optical pellet tracking system. The biggest disadvantage of the pellet target are the high fluctuations of the target density due to the stochastic time structure of the pellet distribution. The size of the pellets has also an impact on the ratio between the average and the peak luminosity: the latter must be kept below 10^{33} cm^{-2}s^{-1} in order to avoid pile-up in the detectors. The design of the pellet target is based on the one currently used at the WASA-at-COSY experiment [69]. The design goals include a pellet size between 25 μm and 40 μm, a lateral spread in the order of 1 mm and variations of the space between pellets between 0.5 mm and 5 mm.

1.2.3 *The Target Spectrometer*

The Target Spectrometer (TS) consists of several detectors placed around the interaction region in an onion-shell arrangement. It covers polar angles between 170° in the backward region and $5° - 10°$ (in the vertical and horizontal planes, respectively) in the forward direction. The layout of the target spectrometer is shown in figure 1.7.

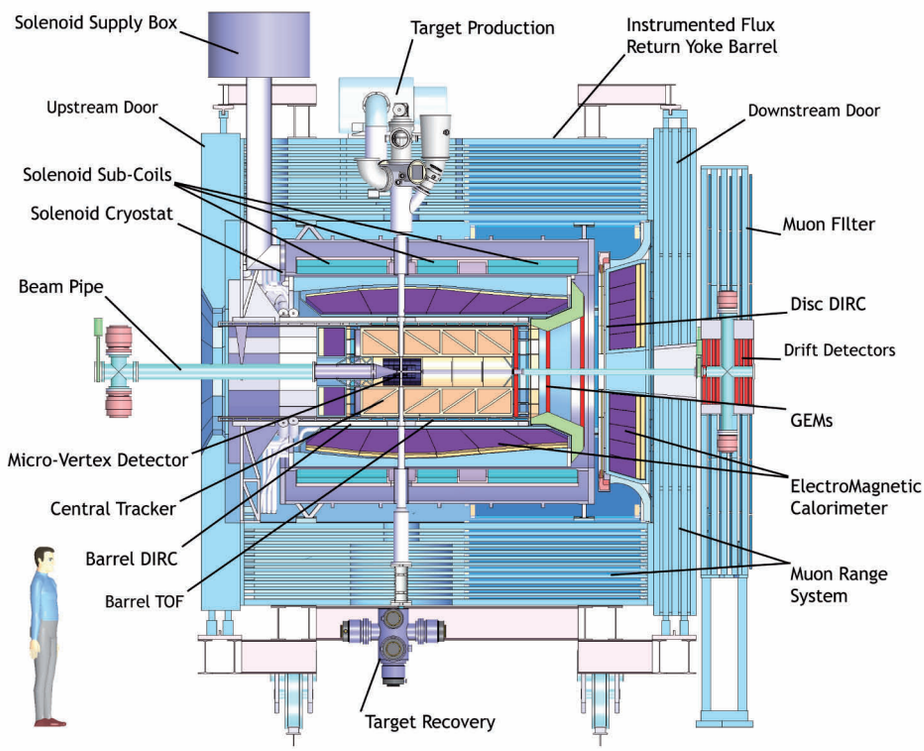


Figure 1.7: Side view of the Target Spectrometer.

The beam pipe crosses the target spectrometer horizontally; all the detectors are built with a cylindrical symmetry around it. A vertical cut out through the magnet and through all the detectors allows for the insertion of the target pipe, which intersects the beam pipe in the center of the spectrometer, defining the interaction region. At the center of the target spectrometer the beam and target pipes are made of beryllium and have a diameter of 20 mm and a wall thickness of 200 μm. A superconducting solenoid magnet permeates the whole target spectrometer with a 2 T field.

1.2.3.1 *Tracking*

The tracking system of the target spectrometer consists of three detectors: the Micro Vertex Detector (MVD), surrounding the interaction region, the Straw Tube Tracker (STT) immediately around it and three Gas Electron Multiplier (GEM) disks in the forward direction.

The Micro Vertex Detector

The Micro Vertex Detector is the innermost detector of $\overline{\text{P}}$ANDA and is designed to provide tracking information with hit points as close as possible to the interaction region [66]. The layout of the MVD, which is visible in figure 1.8, is composed of four concentric barrels and six disks in the forward direction, instrumented with double-sided silicon strip detectors and hybrid pixel detectors.

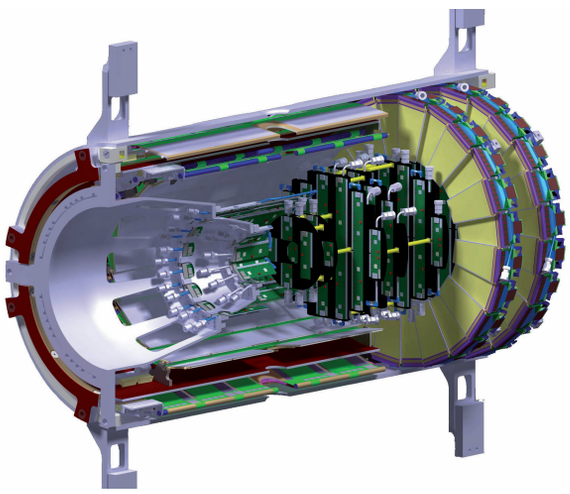


Figure 1.8: Layout of the Micro Vertex Detector, seen from upstream.

The main task of the MVD is the vertex reconstruction, with special focus on distinguishing between the secondary decay vertices and the primary interaction region, in order to reconstruct the decays of short-lived particles (e.g. of the D mesons). Due to the close proximity to the interaction point, a good radiation hardness and the ability to cope with high rates are of the utmost importance for the MVD. Furthermore, in order to limit the degradation of the performance of the subsequent detectors due to multiple scattering, the material budget of the MVD should not exceed 10% of one radiation length over all the detector acceptance.

Since the work of this thesis is centered on the development of the Micro Vertex Detector, this will be described in detail separately in chapter 2.

The Straw Tube Tracker

The Straw Tube Tracker is the central tracker of the experiment and consists of drift chambers in the shape of long narrow tubes, called straws [70]. Each straw has a diameter of 10 mm and a length of 150 cm; the wall of the straw is made of 27 μm thick aluminized Mylar and acts as the cathode. Along the axis of the straw, a single 20 μm thick gold plated tungsten wire represents the anode. The straws are filled with a gas mixture of Ar with CO_2 as a quencher; it is foreseen to fill the straws with an overpressure of 1 bar in order to stiffen and make them self supporting.

The layout of the STT is depicted in figure 1.9. The straws are arranged in 27 planar layers mounted in a hexagonal shape around the MVD; in total 4636 straws cover an area between 15 cm and 41.8 cm in the radial direction. The gas gain is not greater than 10^5 to ensure long term operation; under these conditions, the measurement of the drift time in the straws provides a resolution in the x and y planes

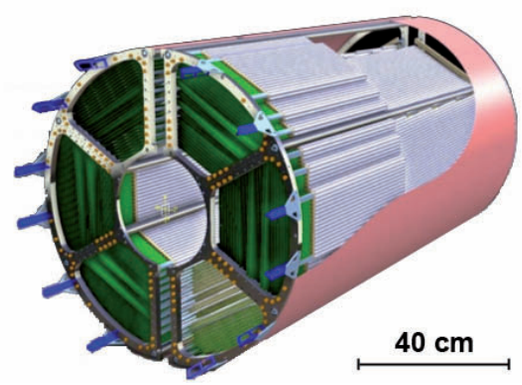


Figure 1.9: Layout of the Straw Tube Tracker, seen from upstream.

better than 150 μm. In order to provide a moderate resolution also in the direction of the beam, it is foreseen to place the central 8 layers of the detector with an angle of ±2.9° with respect to the outer layers; the matching of the hits between the straight and the skewed layers results in a z-resolution in the order of 3 mm.

The design of the detector is extremely light, since the overpressure of the straws supports most of the structure. This leads to a very low material budget, in the order of 1.2% of one radiation length.

The GEM stations

Three sets of GEM stations, placed 1.1, 1.4 and 1.9 m downstream from the interaction point, perform the tracking of particles emitted below 22° [71]. The layout of the GEM station is shown in figure 1.10.

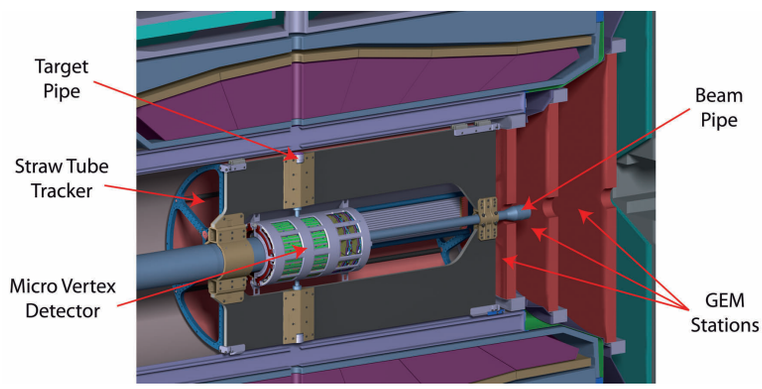


Figure 1.10: Layout of the GEM stations next to the other components of the PANDA tracking system.

Each section consists of a disk equipped with GEM foils as amplification stages; these are made of a thin, microperforated insulating foil, coated on both sides with a conducting layer. When a high voltage is applied at the two conducting layers a strong electric field is created inside the perforations and can lead to secondary ionisation and therefore multiplication of the initial charge. The advantages of this technique with respect to conventional Multi Wire Proportional Chambers (MWPC) or drift chambers include an easier manufacturing, a more flexible geometry and a much higher rate capability.

Each disk has a double plane of readout pads, featuring two projections per plane in order to reduce ambiguities in the high rate environment. The beam pipe in this area has a diameter of 5 cm, which defines the internal size of the disks and the lower limit of their angular acceptance. The outer radius of the disks increases with the distance from the interaction point: at present, a radius of 45, 56 and 74 cm is foreseen for the first, second and third disk, respectively.

1.2.3.2 *Particle identification*

The $\overline{\text{P}}$ANDA setup foresees several detectors to provide an efficient particle identification of a wide range of particles. A Cherenkov detector composed of a barrel part and a forward endcap part and a Time-of-Flight barrel cover most of the momentum spectrum. An overview of the particle identification detectors is shown in figure 1.11.

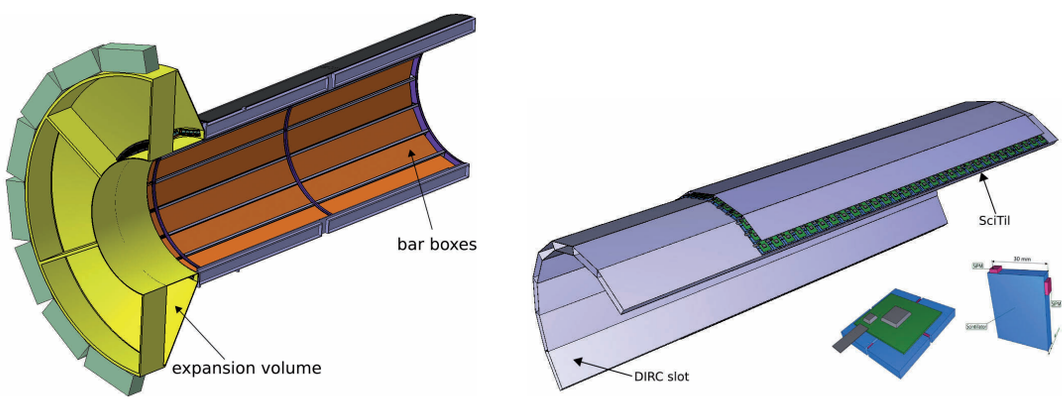


Figure 1.11: Layout of the detectors for particle identification. *Left:* layout of the barrel DIRC detector. *Right:* the Scintillating Tiles (SciTil) detector.

The Barrel DIRC

The barrel part of the Detection of Internally Reflected Cherenkov (DIRC) detector covers the polar angles between 22° and 140°[72]. Its concept is based on the BaBar DIRC [73] and consists of 80 fused silica (artificial quartz) slabs surrounding the beam line at a radius of 47.6 cm. Each slab is 2.5 m long and has a cross section of $1.7 \times 3.3\,\text{cm}^2$. Mirrors placed at the downstream edge reflect the light to the opposite edge, where the readout is performed. Here the slabs are coupled to an expansion volume filled with mineral oil; the light is then focussed onto micro-channel plate photomultipliers (MCP-PMTs) on the backside of the volume. The MCP-PMTs have a pixel size of 6.5 mm and were chosen because they can work efficiently in the 2 T field of the target spectrometer. The barrel DIRC is expected to provide pion - kaon separation for particle momenta up to 3.5 GeV/c.

The Disk DIRC

The forward endcap part of the DIRC has the shape of an octagonal disk and provides pion - kaon separation up to 4 GeV/c momenta in the polar angle below the acceptance of the barrel DIRC (22°) and above 5° and 10° in the vertical and horizontal planes, respectively. The disk DIRC is made of

the same fused silica employed in the barrel part; the disk has a thickness of 2 cm and a radius of 110 cm. It is placed directly upstream of the electromagnetic calorimeter forward endcap; the readout is performed at the outer radius of the disk, where either MCP-PMT or Silicon Photomultipliers (SiPMs) are placed.

The Scintillating Tiles (Time-of-Flight barrel)

The Scintillating Tiles (SciTil) detector, placed just outside the barrel DIRC, provides particle identification for slower particles. About 8000 square plastic scintillator tiles, with a side of 20 to 30 mm and a thickness of 5 mm, are used to form the barrel; each tile is read out with two SiPM, providing a fast signal with a time resolution in the order of 100 ps [74]. Besides for identifying particles below 1 GeV/*c*, the SciTil can be also used to provide track seeds for pattern recognition with the trackers.

1.2.3.3 *The Electromagnetic Calorimeter*

The Electromagnetic Calorimeter (EMC) of $\overline{\text{P}}$ANDA, shown in figure 1.12, detects neutral particles (such as π^0 and photons), leptons and hadrons [75, 76]. The high expected count rates and the compact layout pose strict requirements on the EMC, which must achieve an energy resolution in the order of 2% at 1 GeV and a time resolution better than 2 ns. With a short radiation length (8.8 mm) and Molière radius (2.19 cm), fast response and good radiation hardness, lead tungstate ($PbWO_4$) is the inorganic scintillator material chosen for this detector. Its potential has been exploited in high energy physics for the electromagnetic calorimeter of the CMS experiment at CERN [77]. The crystals in the $\overline{\text{P}}$ANDA EMC are 20 cm long, i.e., approximately 22 radiation lengths, and operate at −25°C in order to increase the light yield (an improvement of a factor 4 is expected with respect to room temperature).

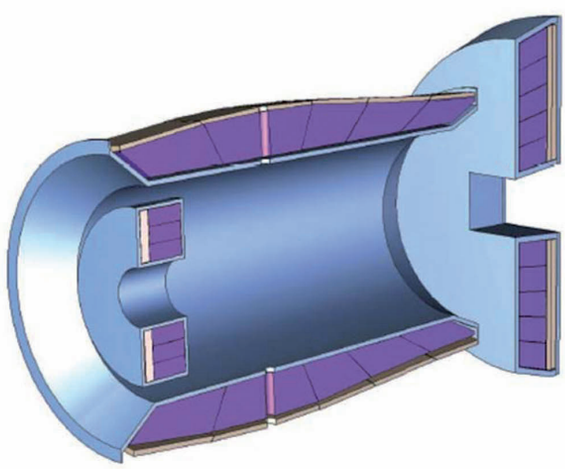


Figure 1.12: Layout of the Electromagnetic Calorimeter, seen from upstream. The barrel and the forward and backward end caps are visible.

The EMC is composed of three parts: a barrel, a forward and a backward end caps. The barrel has an inner radius of 57 cm and consists of 11360 tapered crystals placed directly around the Time-of-Flight detector. The crystals have a front size of $2.1 \times 2.1\,\text{cm}^2$ and are read out by means of large

area avalanche photodiodes (LAAPDs). In the forward endcap, 3600 tapered crystals in a planar arrangement are read out by vacuum photo-triodes [78]; finally, the backward endcap consists of 592 parallelepiped crystals read out by LAAPDs.

1.2.3.4 *The solenoid magnet*

The superconducting solenoid magnet of the target spectrometer is designed to provide a homogeneous 2 T field with fluctuations within ±2% [79]. The superconducting coil has a length of 2.8 m and an inner radius of 90 cm. Two warm bores with a 100 mm diameter on top and bottom provide the space for the target pipe. The solenoid is mounted inside a cryostat, which in turns serves as the supporting structure for the inner detectors. Supporting the cryostat, as well as other detectors, there is an octagonal barrel-shaped iron yoke. The yoke returns the magnetic field of the solenoid ensuring its uniformity and is used in conjunction with sensitive layers to detect muons, as described in section 1.2.3.5. It is also useful to shield the outside area from the solenoid magnetic field. Both ends of the yoke are designed as large sliding doors to provide access to the inner detectors. A cross section of the solenoid magnet is shown in figure 1.13.

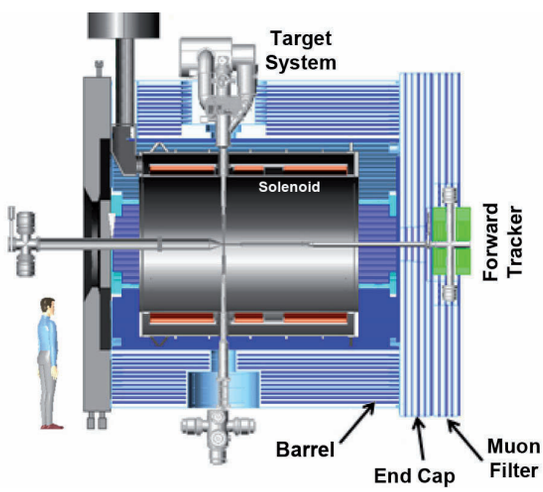


Figure 1.13: Layout of the solenoid magnet of $\overline{\text{P}}$ANDA integrated with the muon detector.

1.2.3.5 *The muon detector*

A series of aluminum rectangular Mini Drift Tubes (MDTs) interleaved in the iron layers of the magnet yoke is used as a range system to detect muons [80]. MDTs are drift chambers with additional capacitive coupled strips which are used to provide a longitudinal information. The muon detector is composed of two main parts: a barrel and a forward end cap. The barrel part consists of 13 MDT layers, each 3 cm thick, alternated with 3 cm thick iron layers; the first and the last iron layers are 6 cm thick. In the forward end cap, the design is optimized to take into account the higher expected particle momenta; the detector is therefore composed of six sensitive layers interleaved with five iron layers, each with a thickness of 6 cm. An additional muon filter with four iron layers and five MDT layers but

otherwise identical to the forward end cap is placed between the target and the forward spectrometer; it is used both to increase the muon detection cabability and to shield the forward spectrometer dipole from the solenoid. All together, the muon detector is instrumented with 2751 MDTs placed in the yoke and 424 MDTs in the additional muon filter.

1.2.3.6 *The detector for hypernuclear studies*

The studies of hypernuclei, described in section 1.1.4, require to exploit the modularity of the $\overline{\text{P}}$ANDA setup: the backward EMC and the MVD will be removed to insert a dedicated nuclear target setup and a detector for γ-spectroscopy [81]. The layout of detectors in the target spectrometer for the hypernuclear studies is shown in figure 1.14.

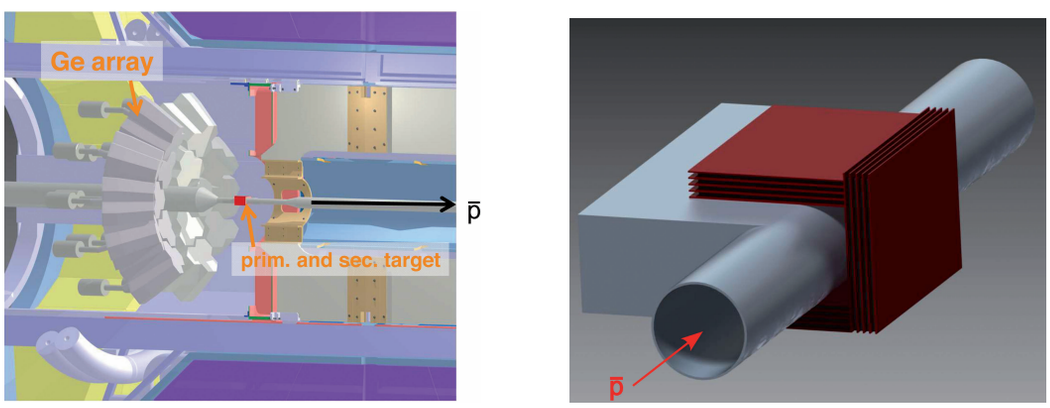


Figure 1.14: The detector for hypernuclear studies. *Left:* the HPGe array and the target system placed in the center of the target spectrometer of $\overline{\text{P}}$ANDA. *Right:* layout of the target system. The primary target and its mechanical support are contained in the rectangular enclosure to the left of the beam pipe. Three blocks of alternating silicon detectors (red) and absorbers (gray) are placed around it.

The hypernuclei production at $\overline{\text{P}}$ANDA follows a two-step process. Hyperons, especially $\Xi^-\overline{\Xi}^+$, are produced on a nuclear target. This consists of a ^{12}C micro-wire with a thickness of 3 μm and a width of 100 μm, suspended in the beam by a C-shaped silicon ring. A secondary target is needed for the formation of double-hypernuclei; its geometry must be very compact to comply with the short mean lifetime of 0.164 ns of the Ξ^-. Is is composed of alternating layers of silicon strip detectors and absorbers, arranged in three blocks around the enclosure of the primary target. Each block has five detector layers, each 300 μm thick, and four absorber layers 1 mm thick, made of ^{9}Be, ^{10,11}B or ^{12,13}C.

The γ-rays from the de-excitation of the hypernuclei are detected by an existing array of high purity germanium detectors, positioned in the backwards direction and equipped with a refurbished readout.

1.2.4 *The Forward Spectrometer*

Because of the fixed target layout of $\overline{\text{P}}$ANDA, an important part of the detector is the Forward Spectrometer (FS), which covers particles emitted with polar angles below ±5° and ±10° in the vertical and horizontal planes, respectively.

Based on a dipole magnet, it is instrumented with trackers, a calorimeter, detectors for particle identification and a muon detector. The layout of the forward spectrometer is shown in figure 1.15.

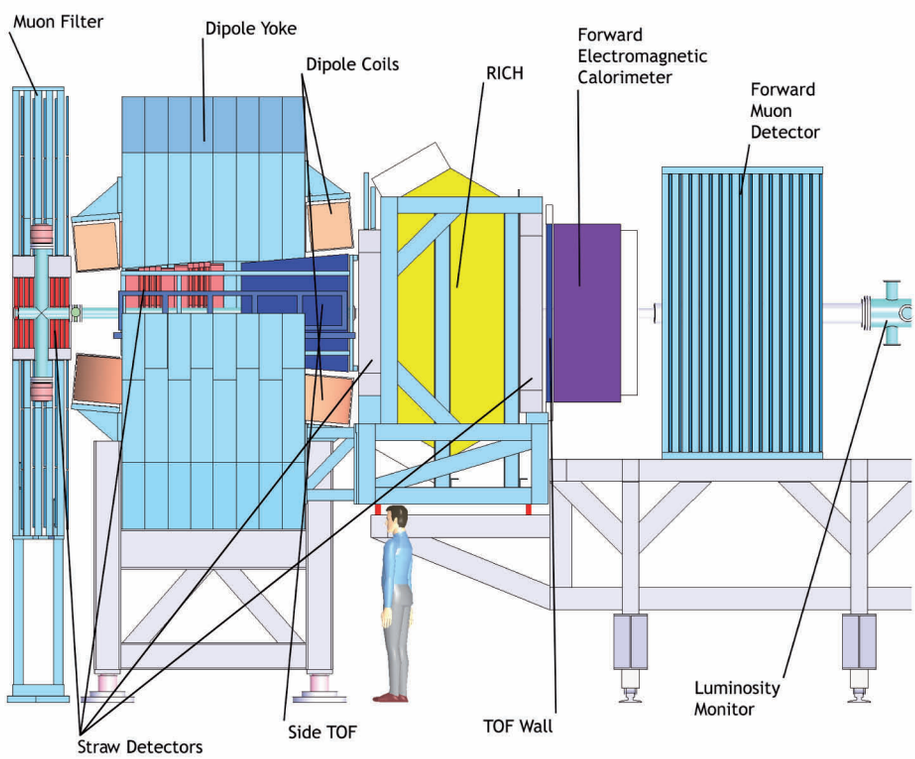


Figure 1.15: Side view of the Forward Spectrometer.

1.2.4.1 *The forward straw tube tracker*

The tracking in the forward region is performed by three stations equipped with straw tubes. Each station is composed of two independent detectors, each consisting of four double layers of straw tubes (two of which with vertical wires and the other two skewed, in order to reconstruct the vertical coordinate). The three stations are placed before, inside and after the dipole magnet. The layout of the forward tracking system is shown in figure 1.16. With the proposed layout it is possible to perform tracking also within each pair of detectors, allowing e.g. to track particles with low momenta that hit the magnet yoke.

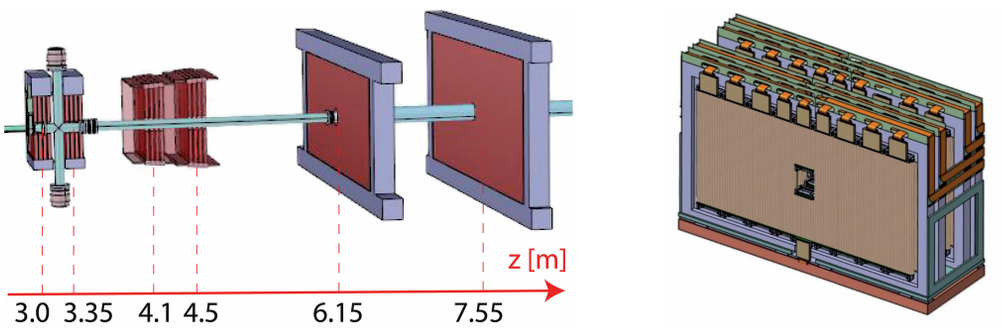


Figure 1.16: *Left:* Layout of the forward tracking system. The three pairs of straw tube detectors are visible; their distances from the interaction region are indicated. *Right:* a pair of tracking detectors.

1.2.4.2 *The forward particle identification detectors*

In the forward spectrometers the particle identification is performed by two detectors, shown in figure 1.17: a Time-of-Flight (ToF) wall and a Ring Imaging Cherenkov detector (RICH)

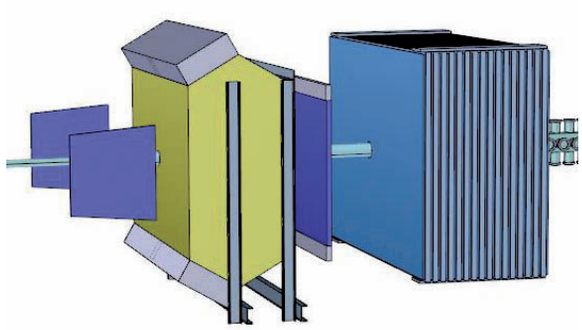


Figure 1.17: The detectors for the particle identification in the Forward Spectrometer: the Time-of-Flight walls, the RICH and the muon detector are visible.

Three ToF walls made of plastic scintillator slabs and read out from both sides with phototubes are used as time-of-flight stop counters. One wall is placed perpendicular to the beam at a distance of approximately 7 m from the interaction region; two smaller walls are placed inside the dipole opening and are used to measure soft particles that do not escape the dipole. The time resolution of the ToF walls is expected to be in the order of 50 ps and allows for a good π/K and K/p separation up to momenta of 2.8 GeV/c and 4.7 GeV/c, respectively.

The RICH detector is based on a dual radiator design similar to the one used at HERMES [82]. The use of silica aerogel ($n = 1.0304$) and C_4F_{10} ($n = 1.00137$) allows for a π/K and K/p separation in a wide momentum range from 2 to 15 GeV/c. A mirror is used to focus the Cherenkov light onto an array of phototubes placed outside the detector acceptance.

1.2.4.3 *The Shashlyk calorimeter*

The detection of photons and electrons in the forward spectrometer is performed by a Shashlyk-type calorimeter [83, 76], which is depicted in figure 1.18. This is realized with alternated plastic scintillator and lead absorber layers with a thickness of 0.275 mm and 1.5 mm, respectively. The readout is performed with Wavelength Shifting fibers (WLS) embedded in the sandwich block and coupled to photomultipliers at the end of the module. The size of one module is $110 \times 110\,\text{mm}^2$ and the length is 680 mm, corresponding to about 20 radiation lengths. To achieve a higher spatial resolution, each module is subdivided in four sub-modules, each with a front size of $55 \times 55\,\text{mm}^2$ and read out individually by one photomultiplier.

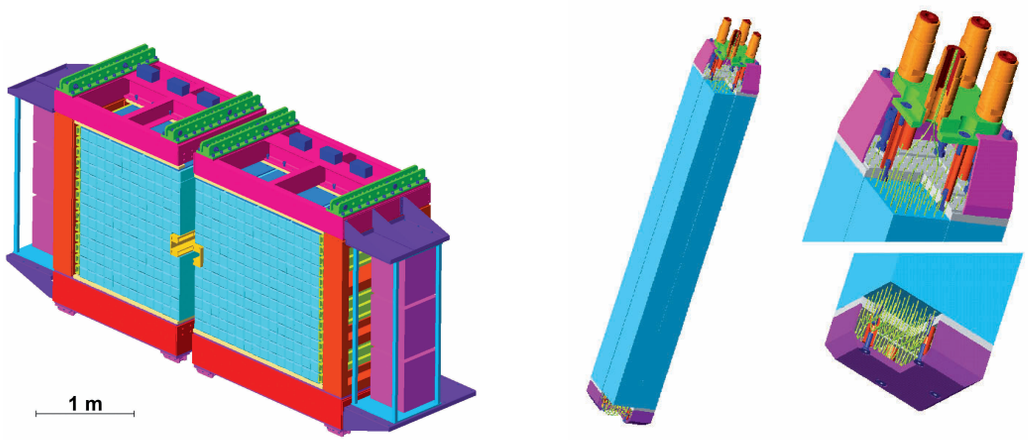


Figure 1.18: *Left:* layout of the Shashlyk calorimeter. *Right:* details of one module subdivided in four sub-modules, each coupled to one photomultiplier.

The calorimeter is composed of 351 modules in a planar arrangement of 13 rows and 27 columns, placed at a distance of 7.5 m downstream from the interaction region. With this layout, the expected energy resolution is in the order of $4\%/\sqrt{E}$.

1.2.4.4 *The forward muon detector*

The muon detector in the forward part is similar to the system used in the target spectrometer. Alternating layers of MDTs and absorbers, each 6 cm thick, enable the discrimination between pions and muons. Additionally, the system can measure with moderate resolution the energy of neutrons and anti-neutrons. The forward muon system is located about 9 m downstream from the interaction region.

1.2.4.5 *The dipole*

The forward spectrometer is based on a dipole magnet with a maximum rigidity of 2 Tm and an opening 3 m wide and about 1 m high [79]. The dipole extends for 2.5 m in the beam direction, with the entrance placed approximately 3.9 m downstream from the interaction region.

The bending power of the dipole causes a deflection of the antiproton beam of 2.2° at the maximum momentum of 15 GeV/*c*; this deviation is compensated by two correcting magnets placed before and after the $\overline{\text{P}}$ANDA experiment. Because of this, the dipole of the forward spectrometer is an integral part of HESR and cannot be removed from its in-beam position; additionally, the ramping of the dipole has to be synchronized with the HESR operation.

1.2.5 *The luminosity detector*

A precise measurement of the time integrated luminosity is essential to determine the cross section of physical processes. To achieve this it is possible to measure the count rates of a specific process with a well known cross section. At $\overline{\text{P}}$ANDA, the luminosity detector reconstructs the angle of elastically scattered antiprotons in the Coulomb-nuclear interference region, i.e., at very small polar angles (from 3 mrad to 25 mrad) with respect to the beam axis [84]. The detector is therefore placed in the most forward part of the experiment, at about 11 m from the interaction point. In order to minimize the scattering of the antiprotons, the detector is hosted in a large vacuum box traversed by the beam pipe.

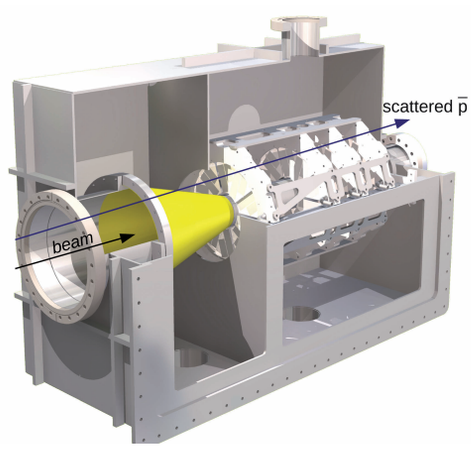


Figure 1.19: The layout of the luminosity detector [85]. On the right, the four rings of MAPS mounted on retractable aluminum frames. On the left, the transition membrane (depicted in yellow) connects the two sectors of the beam pipe and separates the HESR vacuum from the vacuum in the box of the luminosity detector.

The layout, shown in figure 1.19, foresees four tracking planes equipped with HV-MAPS [86]. On each plane, 10 HV-MAPS modules are glued on both sides of a CVD-diamond substrate. The substrate is used to support the detectors and to transfer the heat produced in the MAPS to an aluminum frame with an embedded cooling pipe, to which the diamond substrate is attached. To maximize the detector acceptance, the diameter of the beam pipe in the vacuum box is significantly smaller than outside; the two sections are connected by means of a thin conical 20 μm BoPET / 10 μm Al transition membrane, which must also separate the vacuum of the beam pipe from the one of the vacuum box.

2

THE MICRO VERTEX DETECTOR

The Micro Vertex Detector (MVD) is the innermost detector of $\overline{\text{P}}$ANDA and its main task is to reconstruct the vertex of particle decays and the momentum of charged particles, with hit points as close as possible to the interaction region [66]. The detector must be able to determine accurately the primary interaction region and to distinguish it from the secondary vertices from delayed decays of short-lived particles. The performance requirements and the position at the center of the experiment lead to a number of constraints which the detector has to satisfy.

- **Geometrical constraints:** the minimum distance from the beam axis for the innermost layer of the MVD is given by the beam pipe outer radius (1 cm), while the inner radius of the central tracker (15 cm) defines the limit of the outermost layer. Also, the cone shape of the beam pipe in the backward direction is necessary to achieve the required vacuum in the interaction region. Another geometrical constraint is the necessity to route all the services in the backward direction only; the implications of this requirement will be discussed in chapter 5.

- **High geometrical coverage:** the physics program requires the MVD to cover nearly the full solid angle. Examples of the expected momentum and polar angle particle distributions in $\overline{\text{p}}$p and $\overline{\text{p}}$N collisions, presented in figures 2.1 and 2.2, show that the performances of the detector in the forward region are especially critical. This is particularly true in $\overline{\text{p}}$p annihilations, where the Lorentz boost is reflected by a strong anisotropic emission, which increases with the antiproton momentum. In antiproton-nucleus collisions the anisotropy is less visible and disappears completely with high target atomic numbers.

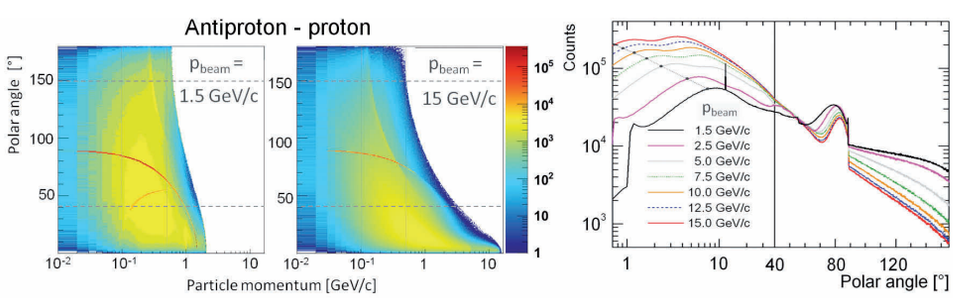


Figure 2.1: Expected particle distributions in $\overline{\text{p}}$p collisions, obtained with 10^7 Dual Parton Model (DPM) [87] events at two different p_{beam} beam momenta [66]. *Left:* particle distributions as a function of particle momentum and polar angle. *Right:* momentum - polar angle density plot.

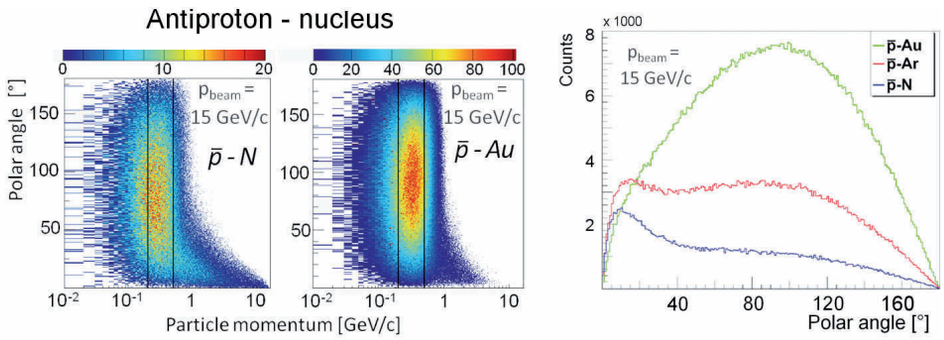


Figure 2.2: Expected particle distributions in $\bar{p}$N collisions, obtained with UrQMD [88] at the maximum beam momentum p_{beam} with different target elements [66]. *Left:* particle distributions as a function of particle momentum and polar angle. *Right:* momentum - polar angle density plot.

To achieve the required resolution in vertex and momentum reconstruction, it is mandatory to have a large number of hit points as close as possible to the interaction point. The design goal is to measure a minimum of 4 hit points per track in the whole acceptance of the detector.

- **High spatial resolution:** with the decay lengths of several open charm states in the order of a few hundred μm (e.g. 123 μm for the D^0 and 312 μm for the $D^{\pm}$), the spatial resolution must be of the same order of magnitude to be able to identify efficiently the displaced secondary vertices. A resolution of 100 μm in the z direction and of a few tens of μm in the xy plane is therefore envisaged.

- **High rates capability:** the high expected interaction rate of $2 \cdot 10^7$ $\bar{p}$p annihilations per second and the proximity of the first layers of the MVD to the interaction region mean that the detector will have to deal with high data rates. The choice of the technology for the various MVD layers, the granularity of the detector and the development of the sensors and of the readout electronics have been therefore strongly influenced by the necessity to cope with hit rates up to several kHz/channel.

- **High radiation hardness:** because of its position close to the primary interaction region, the MVD will be subject to a high radiation load. Considering 10 years of data taking at 50 % duty cycle, an estimated 10 Mrad of total ionizing dose and $10^{13} - 10^{14}$ $n_{1\text{MeV eq}}\,\text{cm}^{-2}$ of non-ionizing radiation have been defined as the levels that the detector components must be able to withstand.

- **Low material budget:** the degradation of the performance of the subsequent detectors due to the MVD must be small. The materials of the MVD, both active and passive, introduce multiple scattering and energy loss effects, which can lead to a biased track and momentum reconstruction in the outer detectors. The aim is to keep the material budget below 10% of one radiation length over all the detector acceptance.

2.1 LAYOUT OF THE MVD

To satisfy the requirements desribed above, the basic geometry of the MVD, which is visible in figure 2.3, consists of four concentric barrels and six disks in the forward direction.

In order to cope with the high expected particle rate, the inner layers of the MVD (i.e., the first two barrels and most of the forward disks) are instrumented with hybrid pixel detectors [89]. On the contrary, double-sided silicon strip detectors are used in the outer layers, i.e., in the last two barrels and in the outer part of the last two disks. Silicon microstrips are able to cope with the rates present in these regions and, with respect to the pixel detectors, can offer a lower material budget and a lower number of channels necessary to cover a given sensitive area [90].

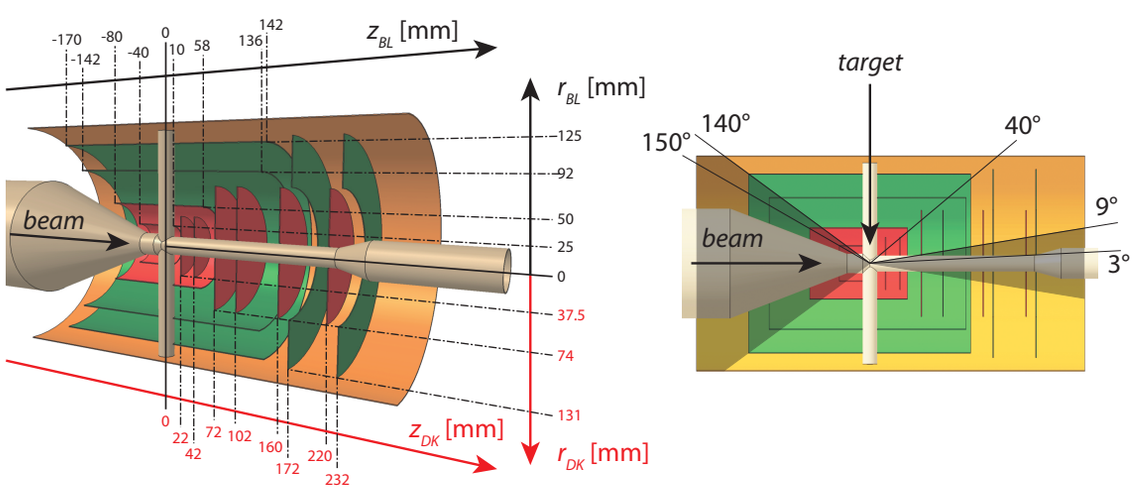


Figure 2.3: Basic geometrical layout of the MVD. *Left:* radial and longitudinal position of the disks (red scales) and of the barrels (black scales) with respect to the nominal interaction point. The red elements represent the pixel part of the detector, while the green elements represent the strip part. The numbers represent the average position between the various elements composing the detector layer and depend on how their position is defined: more details are given in tables 2.2 and 2.4, which describe the pixel and the strip parts, respectively.
Right: polar angle range covered by the various elements of the MVD. The lighter area represents the polar angle range between 9° and 140°, where for each track at least four hit points are detected. The transition between the disk and the barrel part is located at a polar angle of approximately 40°.

The detector is designed to provide some position information for tracks with a polar angle between 3° and 150°, and a minimum of four hit points for tracks between 9° and 140°. The four barrels are placed at a nominal radius of 25, 50, 92 and 125 mm around the beam axis and have a length of 50, 138, 278 and 312 mm, respectively. The pixel disks are of two different kinds: small (the first two, with an outer diameter of 75 mm) and large (the last four, with a diameter of 150 mm); the inner diameter is always 22 mm. They are distributed in the forward direction, with a z position between 22 and 220 mm downstream from the interaction point. Placed approximately around the last two pixel disks, two double-sided strip rings with an inner diameter of 148 mm and an outer diameter of 262 mm complete the detector setup.

2.1.1 *Detector simulations*

To study the performances of the proposed detector layout, an extensive set of MonteCarlo simulation within the PandaRoot framework [91] has been performed. The simulations make use of a detailed CAD model of the detector, which includes the sensors, the readout electronics and all the passive materials for the mechanical support, the cooling system and the cabling. A CAD converter allows to port the CAD model used for the mechanical design into PandaRoot [92]. A detailed review of all the detector simulations performed can be found in [93], [66] and [94].

2.1.1.1 *Detector coverage*

The detector coverage has been simulated with fixed momentum charged pions, generated at the nominal interaction point and emitted isotropically over the polar and azimuthal angles θ and ϕ. The results of the simulation, which takes into account also the solenoidal magnetic field, are shown in figure 2.4. The design goal of four hits per point track is achieved in a large part of the solid angle; lower values are however present in the transition area between the disk and the barrel part, for polar angles between 40° and 70°, and around $\phi = \pm 90°$, where the target pipe is located.

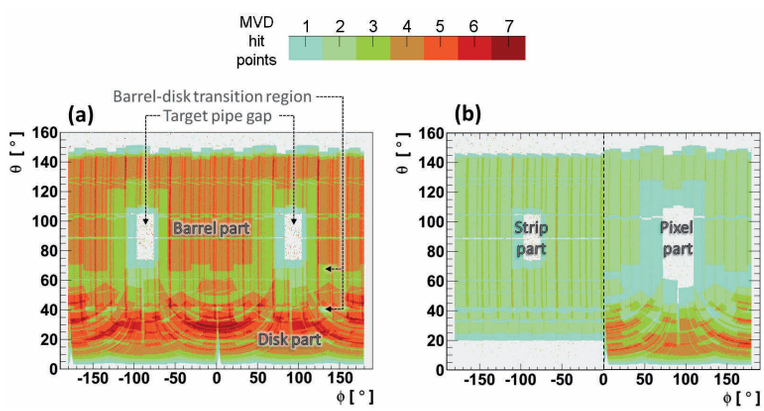


Figure 2.4: MVD detector coverage simulation [93]. *Left:* overall coverage for 1 GeV/*c* charged pions emitted from the nominal interaction point. *Right:* contribution of the MVD strip and pixel parts.

2.1.1.2 *Material budget*

The particles traversing the detector volume undergo multiple scattering and energy loss effects caused by the active and passive materials encountered. The negative impact of such materials can be quantified by their radiation length X_0, which is defined as a function of the charge and mass numbers (Z, A) of the element [10]. A commonly used empirical formula, which gives reliable results within 2.5% for elements heavier than helium, is given by [95]:

$$X_0 = \frac{716.4\ \mathrm{g \cdot cm^{-2}} \cdot A}{Z(Z+1)\ln\frac{287}{\sqrt{Z}}}. \tag{2.1}$$

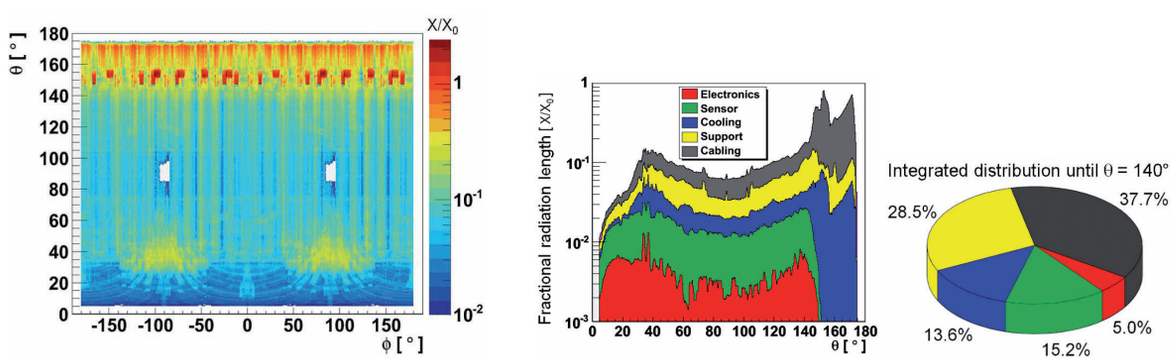
The material budget of the various components of the MVD can be quantified by the fractional radiation length X/X_0, which is summed over all the materials encountered by the particles along their tracks:

$$X/X_0 = \sum_j \frac{\rho_j \cdot L_j}{X_{0_j}}, \tag{2.2}$$

where X_{0_j} and ρ_j are the specific radiation length and density of the material j and L_j its traversed length. In the material budget simulation, two million virtual particles were generated in the nominal interaction point, emitted isotropically over the polar and azimuthal angles and propagated through the detector.

The result in figure 2.5a shows the fractional radiation length correlated with the initial θ and ϕ angles of the particle. The radiation length stays within the design limit of 10%X_0 in most of the solid angle with $\theta < 140°$. Higher values (up to 40%X_0) are present in a limited area around $\phi = \pm 90°$ and $\theta = 40°$, where the routing of the pixel disks is concentrated. Additionally, the radiation length for polar angles greater than 140° is significantly higher and reaches values of several radiation lengths, with large deviations along the azimuthal angle; this is due to the routing of all the detector services in the backward direction.

In figure 2.5b the contribution of the various detector components is shown. The material budget in every region of the MVD is strongly dominated by the passive materials, with the cabling amounting to about 38%, the support structures to 28.5% and the cooling system to about 14% of the total material budget integrated up to $\theta = 140°$.



(a) 2D material budget map of the MVD as a function of the polar and azimuthal angles.

(b) Contribution of the different components of the MVD to the overall material budget, as a function of the polar angle θ and averaged over the azimuthal angle.

Figure 2.5: MVD material budget simulation [93].

2.1.1.3 *Hit rates*

A careful evaluation of the expected particle rate on the various elements of the detector is important to define the specifications of the readout electronics, as well as to design proper data and power transmission lines. $\bar{p}p$ reactions were studied, both at minimum (1.5 GeV/c) and maximum (15 GeV/c)

beam momentum, using the DPM generator and considering the nominal interaction rate of $2 \cdot 10^7$ annihilations per second.

The results shown in figure 2.6 represent the hit rate distribution on the front-end chip level, both for the disk and for the barrel parts.

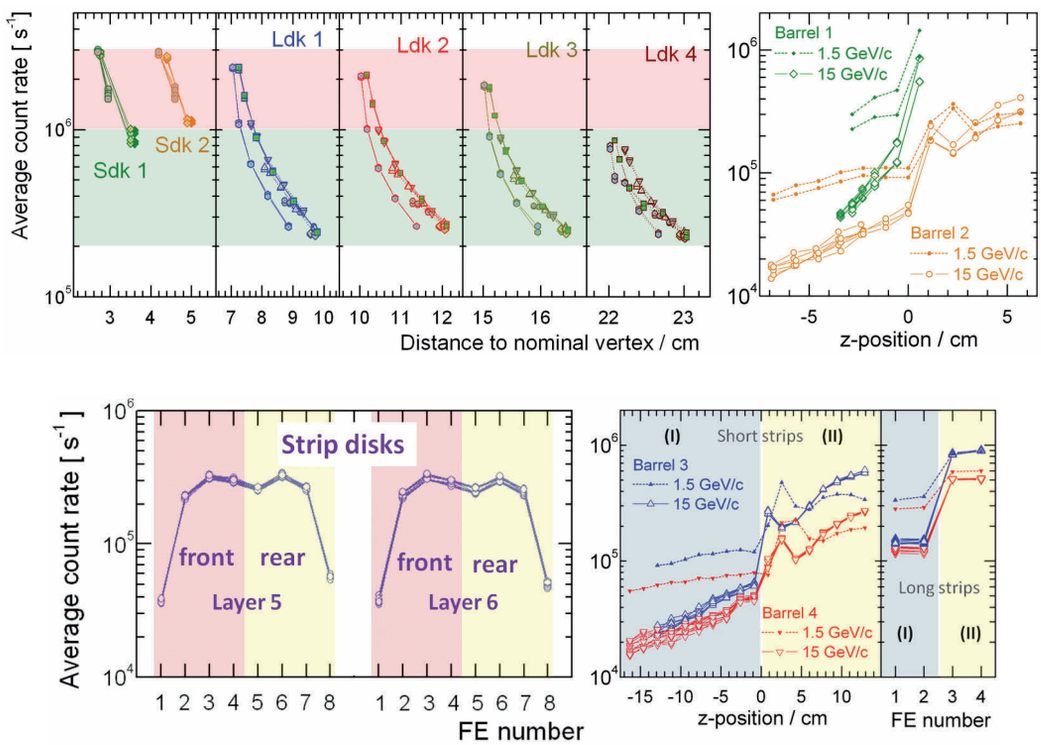


Figure 2.6: MVD hit rates simulation [93]. *Top:* pixel disk and barrel part. *Bottom:* strip disk and barrel part.

The highest rates occur at maximum beam momentum in the disk part at small polar angles. Many front-ends on five out of six pixel disks experience hit rates in excess of 10^6 counts per second, with peak values reaching up to $3 \cdot 10^6$ counts per second. Because of the greater distance from the interaction point and the consequent smaller covered solid angle, the count rates in the strip disks are significantly lower and reach a maximum of approximately $3 \cdot 10^5$ counts per second. However, the detector geometry implemented in the simulation for the strip disk part is considerably different from the one presently foreseen and the simulation should be taken with great care.

In the barrel part, the hit counts are affected by the larger number of particles emitted at large polar angles and at lower momenta. Higher count rates are therefore obtained at the minimum beam momentum, especially in the upstream region ($z < 0$). The highest values are found in the downstream part ($z > 0$), where the frontmost front-ends experience hit rates in the order of 10^6 counts per second both in the pixel and in the strip part. The values obtained for the long strips are consistently higher than those for the short strips; it must be however noted that the simulation considers a scenario where the long strips of two subsequent sensors are ganged together to reduce the number of readout channels. This option has been since then discarded and therefore the long strip values are slightly overestimated.

It must be also noted that, in the strip part, the simulations consider an earlier design with 128-channel front-end chips instead of the current 64-channel layout of the current strip readout chip. The values on the front-end level obtained in the simulation are therefore overestimated; however, the channel level values remain unchanged, since the new design is a mere redistribution of the same number of channels among a larger number of front-ends.

On a channel level, the peak values obtained in the simulations are found at the inner radius of the first pixel disk and in the frontmost short strips of the inner strip barrel; these values are in the order of 1200 and 4000 counts per second in the pixel and in the strip part, respectively.

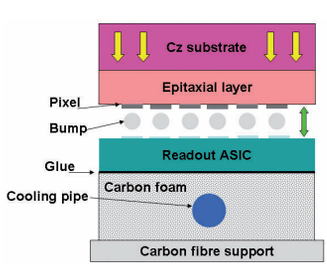
2.2 HYBRID PIXEL DETECTORS

2.2.1 *Detector components*

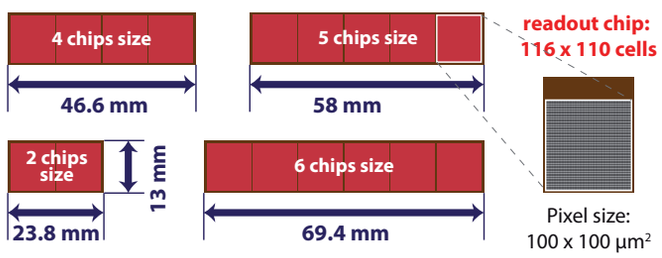
The technology of hybrid pixels has been extensively developed for high energy physics and in particular for the LHC experiments. The detector principle, shown in figure 2.7a, is based on a silicon sensor segmented in a matrix of diodes; each pixel is connected individually to the corresponding cell on a readout chip through a In or Sn-Pb bump. A charged particle traversing the sensor creates electron-hole pairs through ionizations; the charge is separated by means of applying a reverse bias to the junction and later collected and amplified by the readout electronics.

In the $\overline{\text{P}}$ANDA MVD, the design of the pixel detector features 100 μm $\times$ 100 μm pixels, implemented as p^+-type implants on a high resistivity (2 – 4 k$\Omega \cdot$cm) n-type epitaxial layer [96]. The epitaxial layer is 100 μm thick and is grown on a low resistivity (0.01 $\Omega \cdot$cm) n^+-type Czochralski substrate, which has an original thickness of several hundreds of μm, but is later thinned down to about 20 μm to reduce the material budget. The overall thickness of the sensor is therefore in the order of 120 μm.

A readout ASIC named ToPix has been developed in a commercial 130 nm CMOS technology [97]. It is a radiation tolerant, triggerless chip providing fast readout with a system clock of 155.52 MHz. The charge information with 12 bit resolution is obtained through the Time-over-Threshold (ToT) technique. The chip has a cell size of 100 μm $\times$ 100 μm, designed to match the pixels on the sensors,



(a) Concept of the hybrid pixel detector.



(b) Basic sensor geometry in the MVD pixel part: rectangular sensors of four different sizes are used. The elementary unit is the matrix of 116 $\times$ 110 cells in the readout chip, visible on the right.

Figure 2.7: Detector concept for the MVD pixel part.

and features a matrix of 110 columns and 116 rows. The active area is therefore 11.0×11.6 mm^2 and the overall size of the chip, including the peripheral logic, is 11.4×14.8 mm^2.

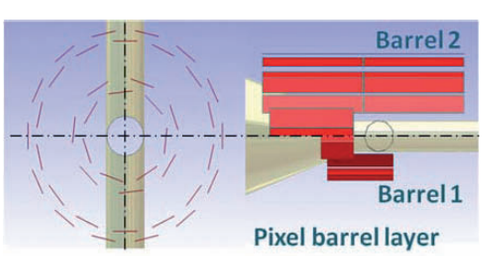
Rectangular pixel sensors of four different sizes will be used in both the barrels and the disks. The elementary unit is the matrix of 110×116 cells on the readout chip; sensors with a two-, four-, five- and six-chips size are foreseen, as shown in figure 2.7b. In order not to leave any gap in the sensitive area, the pixels in the first and last columns of each elementary unit will be wider (300 μm instead of 100 μm) to compensate for the small passive rim on the chip.

2.2.2 *Detector geometry*

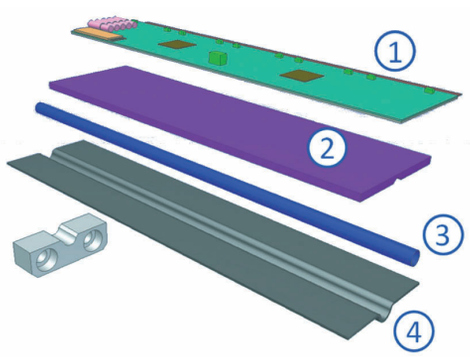
The detector is composed of modules, each consisting of one sensor, the readout chips bump-bonded to it and a multilayer bus. The bus is needed to configure the readout chips, transmit the data outside the MVD and provide the power supply to both the chips and the sensor. The chips will be connected to the bus by means of wire bonding. Depending on the size of the sensor, four different types of modules are foreseen (named in the following S2, S4, S5 and S6 for the two-, four-, five- and six-chips size sensors). The chip side of the module is glued on the mechanical support, which embeds an active cooling system to remove the excess heat produced by the chips, as visible in figure 2.7a. The type of support and its geometry differs between the barrels and the disks.

2.2.2.1 *Pixel barrels*

The barrels are composed of longitudinal staves of different length. Each barrel is made of two rings of different diameter to guarantee the absence of gaps over the azimuthal angle. The staves at the top and at the bottom of the barrels are shorter to accommodate the presence of the target pipe. The first barrel contains 14 staves, 6 of which composed of one S2 module and 8 composed of one S4 module. The second barrel contains 28 staves; 6 staves around the target pipe have a length of five chips, while each of the other 22 staves is made of two consecutive S6 modules, as visible in figure 2.8a.



(a) Transverse ($x-y$) and longitudinal views of the two pixel barrel layers, showing the arrangement of staves around the beam pipe.



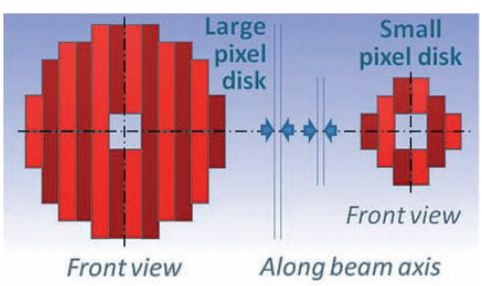
(b) Mechanical support of the pixel barrel staves. (1) detector module; (2) carbon foam; (3) cooling pipe; (4) carbon fiber Ω-support.

Figure 2.8: Geometry of the MVD pixel barrel part and structure of the modules.

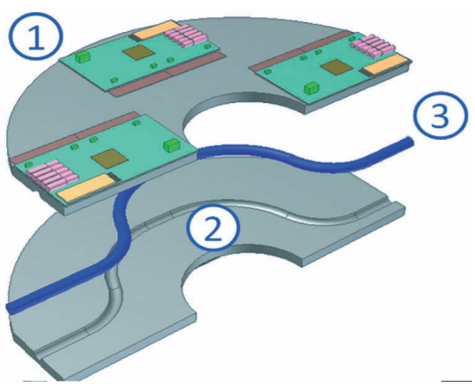
The structure of one stave is shown in figure 2.8b. The module is glued on a layer of carbon foam, a highly thermally conductive material used as a heat sink [98]. A Ω-shaped carbon fiber support is placed underneath and embeds a cooling pipe with an external diameter of 2 mm. On one edge of the stave a plastic reference block is used to connect the stave to the support cone which holds all the staves of both pixel barrels.

2.2.2.2 *Pixel disks*

In the pixel disks, the four differently sized assemblies are used to obtain an optimal coverage. Detector modules are placed on both sides of the disk to ensure a small overlap between adjacent modules and avoid holes in the sensitive area. The planned arrangement of sensors on the disks is visible in figure 2.9a. Each of the two small disks is covered with six S2 modules and two S4 modules, while on each of the large disks there are four S2 modules, four S4 modules, twelve S5 modules and four S6 modules.



(a) Large and small pixel disks. The modules on the front and the back sides of the disks are shown in the drawing in different shades of red.



(b) Mechanical support of the pixel small disks. (1) detector module; (2) carbon foam; (3) cooling pipe.

Figure 2.9: Geometry of the MVD pixel disk part and structure of the modules.

Each small disk is made of a 4 mm thick carbon foam layer, divided in two half-disks to comply with the assembly sequence described in section 2.4. The carbon foam layer is cut transversally in two 2 mm layers and the cooling pipe is embedded between the two, as visible in figure 2.9b; one cooling pipe serves each half of the small disks. The large disks are made of a solid 5 mm thick carbon foam layer, with the cooling pipes inserted in a groove on the carbon foam surface. By using a single carbon foam layer, the use of large quantities of glue to keep the two separate layers together can be avoided. Three U-shaped pipes are used in each half of the large disks.

Including the two barrels and the six disks, the 176 sensors in pixel detector feature about ten million channels, read out by 810 chips, over a sensitive area of 0.107 m^2. A summary of the pixel detector parameters and of the radial and longitudinal position of each barrel and disk layer is presented in tables 2.1 and 2.2, respectively.

Basic parameter	Barrel 1	Barrel 2	Small disks 2x (1 – 2)	Large disks 4x (3 – 6)	Total
Number of supermodules	14 staves	28 staves	–	–	
Number of sensors†	6 2-chips-size	–	6 2-chips-size	4 2-chips-size	34 2-chips-size
	8 4-chips-size	–	2 4-chips-size	4 4-chips-size	28 4-chips-size
	–	6 5-chips-size	–	12 5-chips-size	54 5-chips-size
	–	44 6-chips-size	–	4 6-chips-size	60 6-chips-size
Total:	*14*	*50*	*8*	*24*	*176*
Number of FE chips	44	294	20	108	810
Active silicon area [cm^2]	58.2	388.8	26.4	142.8	1071
Number of readout channels	$\approx 5.6 \cdot 10^5$	$\approx 3.8 \cdot 10^6$	$\approx 2.6 \cdot 10^5$	$\approx 1.4 \cdot 10^6$	$\approx 1.03 \cdot 10^7$

Table 2.1: Summary of design parameters for the pixel part of the MVD.
†The different rows indicate sensors of different sizes.

Detector part		R_{min} [mm]	R_{max} [mm]	z_{min} [mm]	z_{max} [mm]
Barrel 1	Inner ring	21.8	22.8	-46 (-42.4†)	9.5 (8†)
	Outer ring	27.8	28.6		
Barrel 2	Inner ring	47.3	47.9	-91 (-84†)	57.5 (52.5†)
	Outer ring	52.3	52.8		
Disk 1		11.7	36.6	19.8	24.2
Disk 2		11.7	36.6	39.8	44.2
Disk 3		11.7	74	69.3	74.7
Disk 4		11.7	74	99.3	104.7
Disk 5		11.7	74	157.3	162.7
Disk 6		11.7	74	217.3	222.7

Table 2.2: Position of the detector elements in the pixel MVD. The figures indicated with † represent the limits in z of the silicon sensors; the figures without any superscript indicate the overall limits of the detector parts, including the mechanical support.

2.3 DOUBLE-SIDED SILICON STRIP DETECTORS

2.3.1 *Detector components*

Silicon microstrip detectors are widely used as tracking devices in particle physics experiments. The detector principle is based on a silicon sensor segmented in narrow strips; in this way a one-dimensional spatial information can be obtained with a relatively low number of readout channels. Similarly to the pixels, each strip is a reverse-biased junction and the hole-electron pairs produced in the sensor are collected and amplified by the readout electronics, which is typically placed next to the sensor, outside its sensitive area. The spatial resolution depends mostly on the strip pitch p. Assuming that the particle hitting the sensor produces a signal on only one strip, and assuming a uniform distribution of particles over the width of the strip, the resolution is given by $\sigma = p/\sqrt{12}$. However, this can be improved significantly if the charge is shared among neighboring strips [89, 99].

To get a two-dimensional spatial information, two sensors with the strips oriented in different directions are used in conjunction. In a double-sided strip detector the two sets of strips are implemented on the same sensor; in this way, a 2D information can be obtained with a single silicon layer, therefore reducing the material budget.

The main limitation of the strip detectors with respect to the pixels is the lower particle rate that they can sustain, mostly due to the ghost hit effect. When two different particles hit the sensor at the same time, two couples of x and y coordinates are registered, leading to the reconstruction of four hits (the two real hits and two ghosts); the discrimination between real and ghost hits requires further assumptions such as on the charge deposition and becomes more difficult as the rates grow higher. Additionally, the larger area of the individual channels could introduce pile-up effects when several particles hit the same strip in a short time interval.

In the $\overline{\text{P}}$ANDA MVD, the design of the strip detector requires three types of sensors: rectangular and square for the barrel part and trapezoidal for the disk part; the layout of the three types of sensors is visible in figure 2.10.

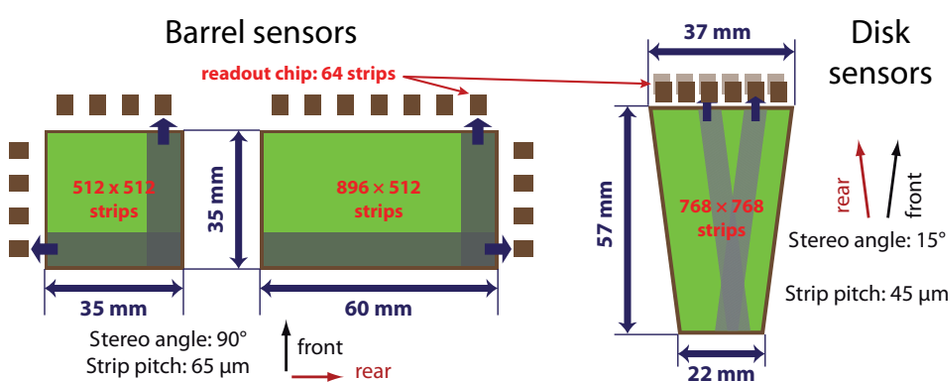


Figure 2.10: Basic sensor geometry in the MVD strip part. *Left:* squared and rectangular sensors used for the barrel part. *Right:* trapezoidal sensors employed in the disk part. In both cases, every second strip of the sensors is read out.

All sensors are 285 μm thick. In the barrel, the sensors feature a strip pitch of 65 μm and a stereo angle of 90°, while in the barrel a strip pitch of 45 μm and a stereo angle of 15° are used. It is foreseen to put one passive intermediate floating strip between the strips connected to the readout electronics, which influences the charge sharing and improves the spatial resolution [100]. The readout pitch will therefore be 130 μm in the barrels and 90 μm in the disks.

A detailed description of the sensors and the results of the characterization of the prototypes can be found in chapters 3 and 4. A readout ASIC named PASTA and a Module Data Concentrator (MDC) chip are currently under development in a commercial 110 nm CMOS technology; these are described in chapter 3.

2.3.2 *Detector geometry*

The structure of the strip detector differs significantly between the barrels and the disks, although the basic philosophy is the same. One sensor is readout by several PASTA chips (from a minimum of 8 chips for each barrel square sensor, to a maximum of 12 chips for each trapezoidal disk sensor), distributed between the p- and the n-side. One MDC collects the signals from all the chips connected to one sensor and serves as interface to the outside. The active components are supported by a carbon fiber structure with an embedded active cooling system.

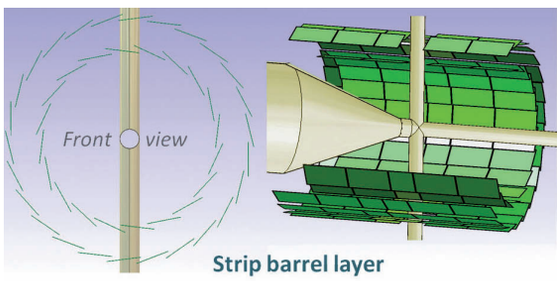
2.3.2.1 *Strip barrels*

The two strip barrels are the largest part of the MVD in terms of covered area, amounting to more than 70% of the full MVD and to approximately 85% of the whole strip detector. In terms of readout channels, however, the strip barrels contribute to only 1.5% of the total MVD channels, and the entire strip detector to less than 2%.

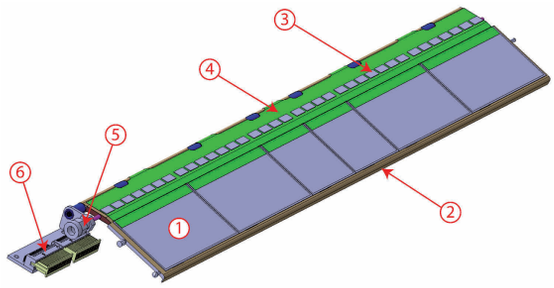
The basic element of the barrels is a stave, which contains between four and six sensors arranged in a straight line. The staves are arranged circularly around a common cylindrical support to form two barrels; a schematic layout is visible in figure 2.11a. A paddlewheel arrangement ensures a small overlap between adjacent sensors. The inner and outer barrel are equipped with 20 and 26 staves, respectively. Special staves are foreseen at the top and at the bottom of the detector to accommodate the target pipe.

The structure of one stave is shown in figure 2.11b. The sensors are glued on a carbon fiber support stave which embeds the cooling system; a flexible multilayer bus is also glued on the stave next to the sensors. The bus hosts the readout chips, the MDCs and all the necessary components such as the filtering capacitors. It is used to connect the sensors to the readout electronics and to provide interconnection between the various chips and to the outside world; the power supply to the chips and to the sensors is also provided through the bus.

A detailed description of the layout of the stave and of its integration into the two barrels can be found in chapters 3 and 5.



(a) Transverse ($x - y$) and longitudinal views of the two strip barrel layers, showing the arrangement of staves around the beam pipe.

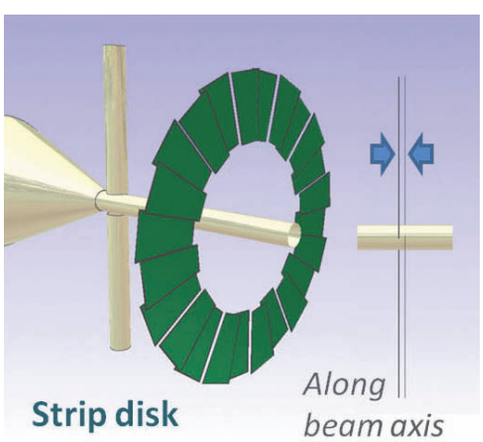


(b) A fully equipped barrel stave. (1) sensor; (2) carbon fiber stave; (3) readout chips; (4) flexible bus; (5) cooling pipe; (6) power connector.

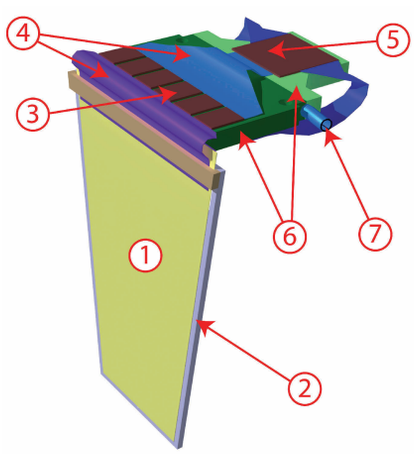
Figure 2.11: Geometry of the MVD strip barrel part and layout of a stave.

2.3.2.2 *Strip disks*

Two identical strip disks are placed 172 and 232 mm downstream from the interaction point, roughly around the last two pixel disks. Each strip disk is composed of 24 modules, each based on one trapezoidal sensor. The schematic arrangement of sensors in one disk is visible in figure 2.12a. Two adjacent modules are placed with an offset in the z axis of 5 mm, thus allowing a small overlap between the sensors.



(a) Arrangement of the trapezoidal sensors in one strip disk.



(b) Fully equipped module of a strip disk. (1) sensor; (2) carbon fiber frame; (3) PASTA chips; (4) flexible bus; (5) MDC chip; (6) carbon foam; (7) cooling pipe.

Figure 2.12: Geometry of the MVD strip disk part and structure of the modules.

Each disk module, visible in figure 2.12b, features one trapezoidal sensor read out by 12 PASTA chips (6 on each side). The chips are hosted on a carbon foam block connected to the cooling pipe; a second carbon foam block hosts the MDC and is also in contact with the pipe. Flexible multilayer

busses are used to connect the sensor and the chips. The sensor is supported by a light carbon fiber frame; the readout of both sides is performed at the sensor edge at the outer radius of the disk. The carbon foam block hosting the readout electronics is placed perpendicular to the sensor in downstream direction. Six modules share one cooling pipe and form a quarter disk; the four quarters composing a disk are assembled on a common support.

On the whole, the strip detector consists of 296 sensors covering an area of 0.5 m^2 with roughly $2 \cdot 10^5$ readout channels, requiring over 3000 readout chips. A summary of the strip detector parameters and of the radial and longitudinal position of each barrel and disk layer is presented in tables 2.3 and 2.4, respectively.

Basic parameter	**Barrel 3**	**Barrel 4**	**Disks 7 / 8**	**Total**
Number of supermodules	20 staves	26 staves	24 modules	
Number of sensors	80 rect.	104 rect.	–	184 rect.
	16 square	48 square	–	64 rect.
	–	–	24 trapez.	48 trapez.
Total:	*96*	*152*	*24*	*296*
Number of FE chips	1008	1528	288	3112
Number of MDC chips	96	152	24	296
Active silicon area [m^2]	0.17	0.25	0.036	0.5
Number of readout channels	$\approx 6.5 \cdot 10^4$	$\approx 9.8 \cdot 10^4$	$\approx 1.8 \cdot 10^4$	$\approx 2 \cdot 10^5$

Table 2.3: Summary of design parameters for the strip part of the MVD.

Detector part	$\mathbf{R_{min}}$ **[mm]**	$\mathbf{R_{max}}$ **[mm]**	$\mathbf{z_{min}}$ **[mm]**	$\mathbf{z_{max}}$ **[mm]**
Barrel 3	89.7	96.9	-142.3 (-140.7†)	135.8 (134.1†)
Barrel 4	123.2	129.2	-171.2 (-169.5†)	142.1 (140.4†)
Disk 7	74.3	131.2	172 (172†)	$\simeq$ 200 (177†)
Disk 8	74.3	131.2	232 (232†)	$\simeq$ 260 (237†)

Table 2.4: Position of the detector elements in the strip MVD. The figures indicated with † represent the limits in z of the sensors; the figures without any superscript indicate the overall limits of the detector parts, including mechanical support and cooling.

2.4 MECHANICAL INTEGRATION

A CAD representation of the layout of the MVD, showing the various sub-detectors and their mechanical integration, is presented in figure 2.13.

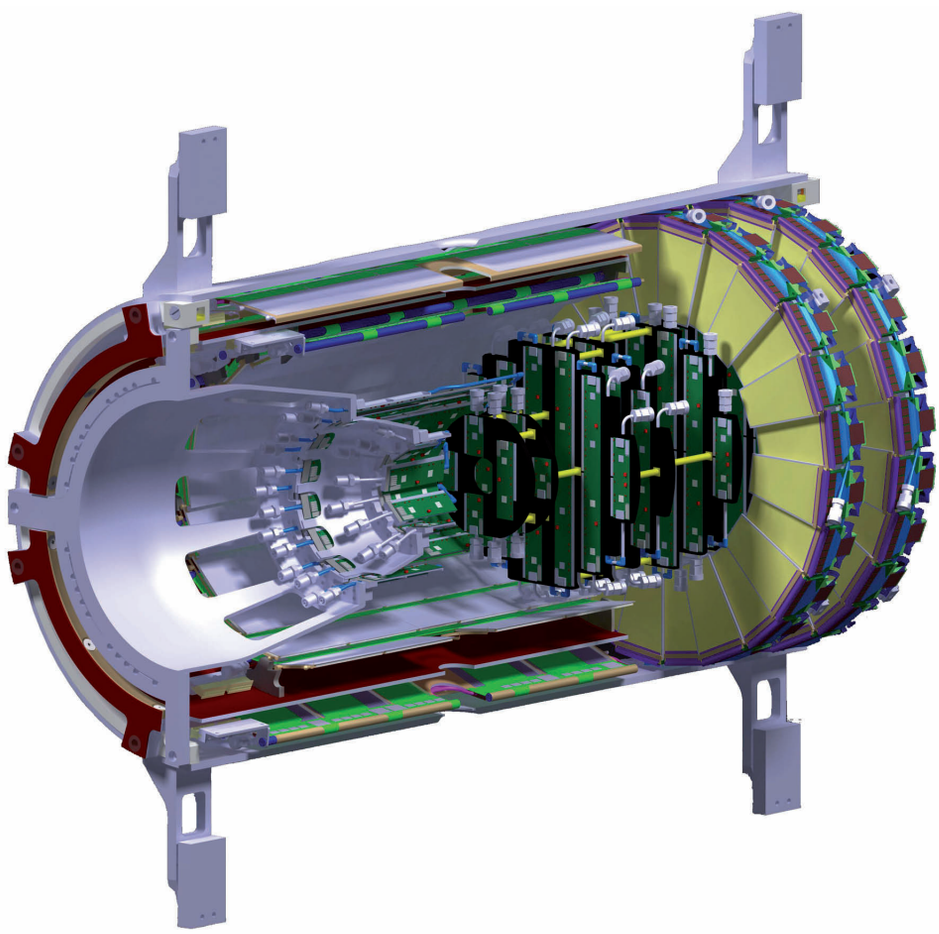


Figure 2.13: CAD drawing of the MVD, seen from upstream. All the subdetectors and the relative support structures are visible; some elements are hidden, thus allowing to see the inner components.

The main structural system of the MVD is the global frame, shown in figure 2.14. It is realized with two skins of M55J carbon fiber prepreg separated by a rigid foam filling and a series of reinforcement ribs; it serves both as a connection to the outside world, as well as a support for the sub-detectors. The global frame will be supported by the central tracker frame, which in turn is connected to rails on the outer detectors. During the assembly phase, the beam-target pipe assembly will be prepared separately and connected to the central tracker frame, to which the MVD was previously attached. This solution requires the MVD to be composed of two independent halves, separated in the $y - z$ plane, i.e., the one defined by the beam and target pipe axes; this division is maintained in each sub-detector.

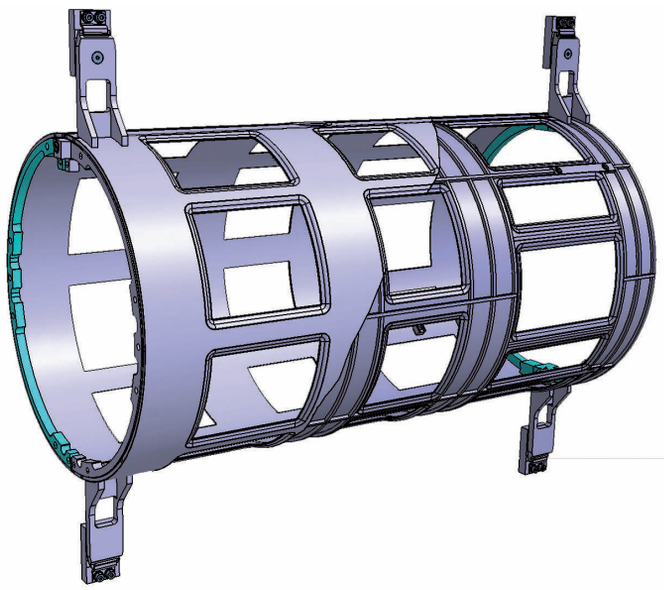
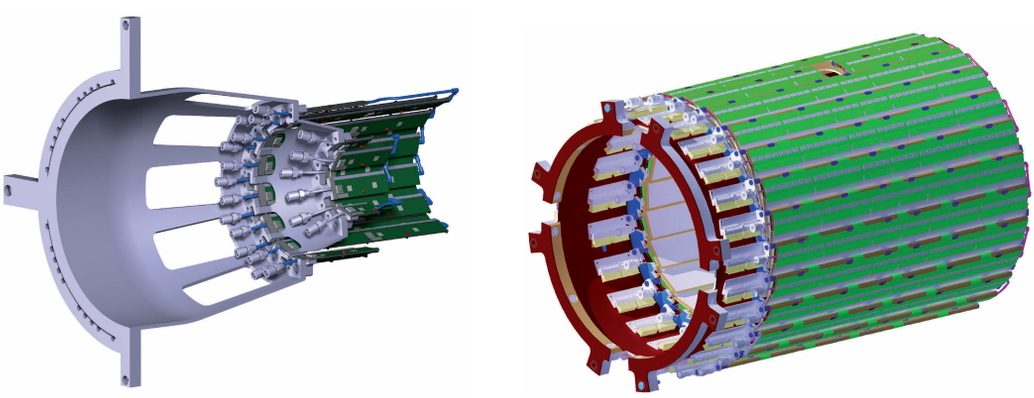


Figure 2.14: Mechanical integration of the MVD: the global frame, seen from upstream. In the right part of the picture the outer carbon fiber skin is hidden, showing the inner reinforcement ribs.

The pixel and strip barrels are attached in a cantilever mode to the backward flange of the global frame. In the pixel part, the staves of the inner and outer half-barrels are connected to a support cone, whose shape is mostly constrained by the presence of the beam pipe. Similarly to the global frame, the cone is realized with carbon fiber and rigid foam and it implements two fiber-reinforced plastic reference rings which are used for the precise positioning of the staves. The two half-barrels and the half-cone are visible in figure 2.15a. In the strip part the two barrels are arranged around a common carbon fiber/foam cylindrical support. The cylinder is 390 mm long and extends from the backward



(a) The two pixel barrels on the support cone, seen from upstream. Only the left half-detector is pictured.

(b) The two strip barrels on the support cylinder, seen from upstream.

Figure 2.15: Mechanical integration of the MVD: the barrel part.

flange of the global flange over the full length of the barrel staves, i.e., up to a z coordinate of +145 mm. Four sawtooth supports are placed on the cylinder, two on the inner side and two on the outer side; the staves of the third and fourth barrels are connected to the inner and outer sawtooth supports, respectively (further details can be found in chapter 3).

In the disk part, the connection to the global frame is achieved through the strip disks, which are suspended from the forward part of the frame; the pixel disks are in turn supported by the strip disks. The first five pixel disks are connected together by means of spacers attached on the carbon foam disk surface; the assembly is then suspended from the first strip disk, while the second strip disk supports only the last pixel disk. The entire MVD disk part is visible in figure 2.16.

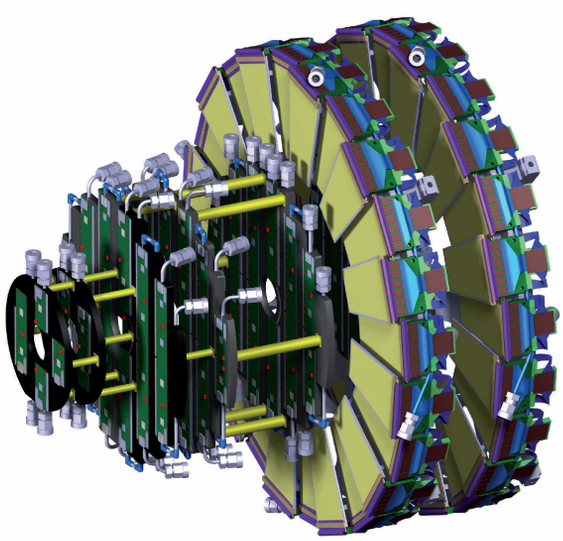


Figure 2.16: Mechanical integration of the MVD: the disk part.

2.5 OFF-DETECTOR COMPONENTS

The Micro Vertex Detector, described in the previous sections, is a compact system which contains most of the active elements required to perform its tasks. However, for its functioning it relies on the presence of a various range of ancillary systems for the power supply, the data transmission and processing and for the detector cooling. The development of these components takes into account the requirements for the detector performances, as well as the possible interferences with the rest of the $\overline{\text{P}}$ANDA setup.

A brief overview of the off-detector part of the MVD is presented in the following; the focus is on those components that have direct impact on the detector mechanical integration and on the cabling, i.e., the electro-optical transceivers, the power supplies and the MVD cooling system.

2.5.1 *GBT electro-optical transceivers*

The maximum expected data rate, derived from the hit rates simulations described in section 2.1.1, is estimated to be 450 Mbit/s/chip in some parts of the pixel MVD [66]. Because of the lack of a hardware trigger, no reduction of the amount of data is possible at the front-end level, thus requiring the implementation of fast transmission lines with a large bandwidth.

The data transmission on the ToPix chip in the pixel part, as well as on the MDC chip in the strip part, will be implemented with the e-link, a radiation hard, high speed serial link for chip-to-chip communication, developed by CERN for high energy physics applications [101]. An electro-optical converter will be used as close as possible to the detector, in order to increase the bandwidth of the lines and reduce the number of required cables. The conversion will be implemented with the GigaBit Transceiver (GBT) and the Versatile Link (VL), also developed at CERN, which will provide a comprehensive set of components for a radiation hard optical link [102, 103].

Detector part		Number of chips*	Number of GBT boards	
			minimal	extended
Strip part	Barrel 3	96	10	10
	Barrel 4	152	16	24
	Disks	48	6	8
Total strip:		*296*	*32*	*42*
Pixel part	Barrel 1	44	12	12
	Barrel 2	294	50	48
	Small disks	40	8	14
	Large disks	432	88	88
Total pixel:		*810*	*158*	*162*
Total MVD:		***1106***	***190***	***204***

Table 2.5: Required GBT boards for the strip and pixel parts of the MVD.
*MDC chip in the strip part and ToPix chip in the pixel part. Each MDC chip is connected through one e-link; each ToPix chip has one or two e-links, depending on the position in the detector.
The minimal number of GBT boards is derived from the number of required e-links, divided by ten (number of e-links on each GBT board) and rounded to the next higher even number to take into account the left-right detector symmetry.
The extended scenario, in an attempt to simplify the cabling, considers every GBT board connected to a maximum of two separate sensor module and each sensor module connected to exactly one GBT board. The left-right detector symmetry is preserved as well.

The GBT chipset employed for the MVD will be hosted on a small dedicated board, under development at INFN, containing one GBTX serializer-deserializer chip [104], the GBLD laser driver [105], the VTRx optical transceiver and all the additional components necessary for their operation. Each board will feature up to ten bi-directional e-link inputs with a data rate of 320 Mbit/s and one 4.8 Gbit/s optical link.

The number of GBT boards is derived, in a first approximation, from the number of e-links coming out of the MVD. In the strip part, the MDC chips collect the signals from all the chips on one sensor and are therefore the only interface to the outside; each MDC is equipped with one e-link. In the pixel part the situation is more complicated, since the expected data rates are higher than in the strip part. The e-link transceivers are implemented directly on the ToPix chips, withouht any further concentration stage. Each chip is equipped with two e-links: in the hottest areas of the detector, where the data rates are higher, both links need to be used, while elsewhere it is possible to leave one disconnected. In this scenario, a total of 190 GBT boards would be required for the entire MVD.

There are however other factors to be taken into account in order to dimension correctly the GBT section. The e-link multiplicity on stave- and disk-level for the strip part cannot be easily matched to the ten channels on each GBT board. An efficient utilization of all the boards would require putting together links from physically independent modules, sometimes placed far apart, leading to a complicated routing scheme and to extensive use of bespoke data cables. Similar issues are present in the pixel part as well.

A more conservative evaluation, considering each GBT board serving a maximum of two separate detector modules, each detector module connected to exactly one GBT board and a complete independence of the left and right detector halves, has been also considered. This leads to a total of 204 GBT boards, or 14 more than in the minimal solution. Both scenarios are presented in table 2.5.

In the current design, 192 boards boards are arranged on 12 aluminum bars, each hosting 16 boards. The bars are arranged on two cylindrical halves, clamped around the beam pipe directly upstream from the MVD; each bar embeds a cooling pipe to remove the excess heat from the GBT chips. The layout of one bar and of the entire GBT area are presented in figure 2.17. It must be noted that this layout is barely sufficient for the minimal number of GBT boards, and that the size of the board, at the time of writing, was not yet finalized. An eventual increase of the number of the boards or of their size will require extensive modifications to this part.

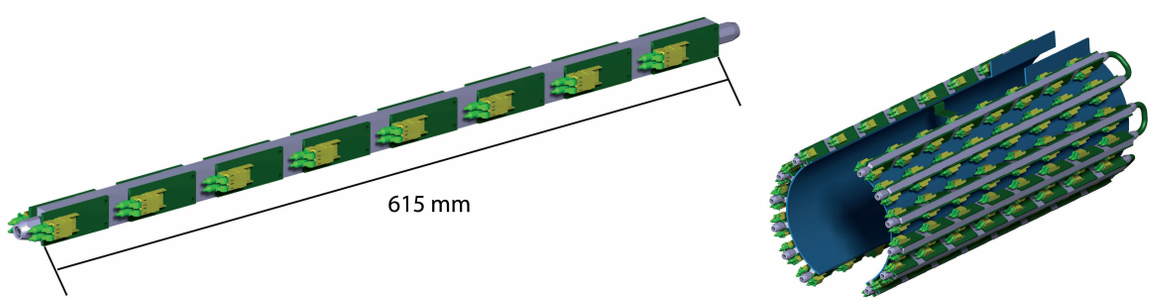


Figure 2.17: MVD off-detector components: the GBT electro-optical transceivers. *Left:* one of the bars, each hosting 16 GBT boards. *Right:* the twelve bars are arranged around the beam pipe, directly upstream from the MVD.

The inner diameter of the GBT sector, at 202 mm, is limited by the presence of a flange connecting two beam pipe sectors. The outer diameter is equal to 275 mm, leaving a 1.75 cm radial clearance until the maximum allowed outer diameter of the MVD services, equal to 310 mm. More details about this sector and about its cabling scheme can be found in section 5.3.

2.5.2 *Detector powering - DC-DC converters*

The use of DC-DC converters is foreseen for the power supply of the low voltage to all the front-end electronics in both the pixel and the strip part.

The FEASTMP converter, developed at CERN for the upgrade of the LHC experiments, will be used [106]. It features an input voltage from 5 to 12 V, an output voltage between 0.9 and 5 V selectable at the time of fabrication, a continuous load capability of 4 A and 10 W and a radiation tolerance well in excess of the $\overline{\text{P}}$ANDA specifications. It makes use of air core coils instead of ferrite ones, in order to be compatible with operation in a strong magnetic field. Including the electromagnetic shield and the connector, the module has an overall size of $17 \times 37.6 \times 14.4$ mm^3; a picture of a module is shown in figure 2.18.

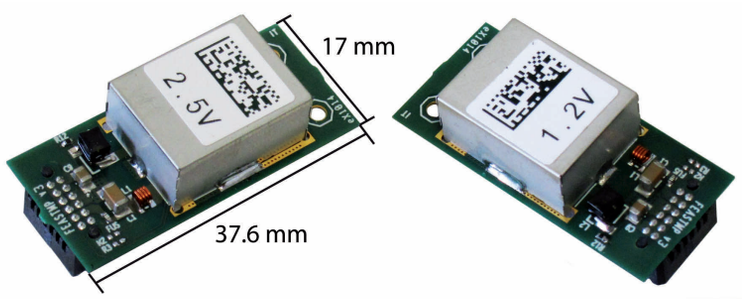


Figure 2.18: MVD off-detector components: two DC-DC converters.

The DC-DC converters will provide the power supply to a total of 810 ToPix chips in the pixel part, as well as to 3112 PASTA and 296 MDC chips in the strip part. In the current scenario, a minimum of 1792 DC-DC converters are required for the entire MVD. This number is derived from a detailed study of the strip and pixel powering scheme, presented in section 5.3, and takes into account the power and grounding requirements of the front-end chips, the properties of the chosen DC-DC converters and the issues related to the cabling.

The proposed layout, shown in figure 2.19, foresees three group of bars arranged cylindrically around the beam pipe, upstream from the GBT sector. Up to 24 bars with 88 converters each, for a total of 2112 converters, can be placed with such an arrangement. Each bar consists of two aluminum blocks, cast around a U-shaped steel pipe used for the cooling system. Four layers of converters can be placed on the outer faces of the two aluminum blocks.

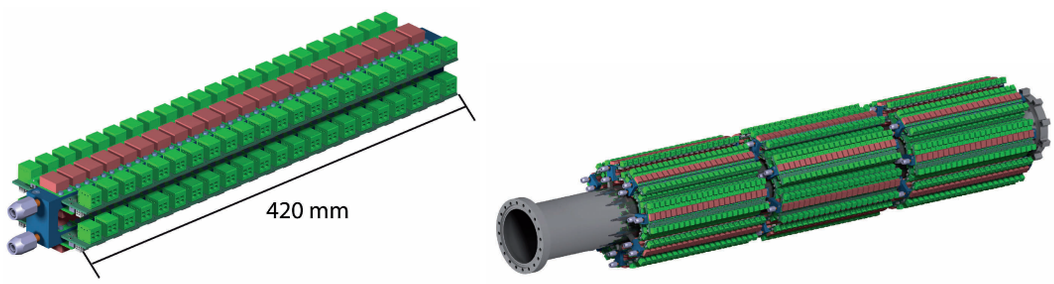


Figure 2.19: MVD off-detector components: the DC-DC converter boards. *Left:* one of the bars, hosting 88 DC-DC converters in four rows. *Right:* the DC-DC sector of the services around the beam pipe, directly upstream from the GBT boards. Up to 24 bars are accommodated in three groups, for a total of 2112 DC-DC devices.

2.5.3 *Cooling system*

The detector cooling system is designed to remove the excess heat from the front-end electronics and to keep the sensor temperature under control. Water at a temperature of 18°C will be used as coolant, with a depression system conceived to avoid any leak in the detector volume.

In all the detector modules, the cooling pipes will have an internal diameter of 1.84 mm and a wall thickness of 80 μm and will be realized in a Ni-Co alloy. U-shaped tubes, designed to use both the supply and the return line for cooling purposes, will be used wherever possible in the MVD. Each tube will therefore serve two adjacent staves in the barrel part (both for the pixels and for the strips). In the strip disks, one tube will be used to cool each disk quarter; in the pixel disks, each disk will use either two or six pipes for the small and large disks, respectively. A total of 32 metal tubes in the strip part and 49 tubes in the pixel part will therefore be present.

Immediately outside the MVD volume, flexible polyurethane tubes with a diameter of 6 mm will be used to route the cooling circuits until the manifolds, located around the beam pipe in the MVD service sector. Here groups of two-three metal tubes will be merged into a single circuit going to the outside; the pressure sensors will be also located here and will ensure the underpressure operation of the system. A total of 21 circuits from the pixel part and 22 circuits from the strip part, plus another 36 circuits for the cooling of the DC-DC and GBT boards, will be then routed for approximately 65 m until the cooling plant, located in a dedicated area in the $\overline{\text{P}}$ANDA hall.

3

DESIGN OF A STRIP MODULE

This chapter describes the design of a stave in the strip barrels of the MVD, whose basic concept has been briefly introduced in section 2.3.2.

In the first two sections, the active components of the strip detector, i.e., the silicon sensors and the two custom ASICs, will be presented. Particular emphasis will be given to the aspects related to the detector integration including, inter alia, geometrical layout, power supply and heat dissipation issues, connection requirements and pad position.

The last section is devoted to the mechanical support of the individual staves, with the embedded active cooling system, and to the support of the two barrels.

3.1 Double-sided Silicon Strip Sensors

As introduced in the previous chapter, square and rectangular double-sided silicon strip sensors are foreseen in the MVD strip barrels. The main dimensions of the sensors are shown in figure 3.1. These have been chosen in order to cope with the maximum expected particle rate per channel and to achieve a good coverage on the two barrels with a small number of different geometries. The limitations on the maximum size obtainable on 4" wafers, which are used by the sensor producer, have also been taken into account.

The rectangular sensors feature 896 short (33.299 mm) strips on the p-side and 512 long (58.247 mm) strips on the n-side. The square sensors feature 512 strips on each side. In both geometries, the strip on the two sides are orthogonal to each other. The strips have a pitch of 65 μm and a width of 30 μm and are implemented with p^+-in-n implants on the p-side and with n^+-in-n implants on the n-side.

The strips can be connected through AC- and DC-coupled bonding pads; to allow for some freedom in the module design, each strip features four AC pads and one DC pad. The DC pads are placed in two rows at the edge of the active area; the pads for the odd strips are placed at the bottom and those for the even strips at the top. Each pad has a passivation opening of 30×95 μm^2. The AC pads are distributed over four identical double-rows. Two double-rows are placed towards the top edge; the other two are placed symmetrically towards the bottom edge, as shown in figure 3.2. Within each pair of rows, the one closer the sensor edge contains the pads of the odd strips and the one towards the sensor center the pads of the even strips. The spacing between the two rows is 800 μm and the passivation opening of the pads has a size of 51×196 μm^2.

Any of the four AC-pads double rows can be used to connect all the strips on the sensor and the choice depends entirely on the module design requirements. Furthermore, since it is planned to use a

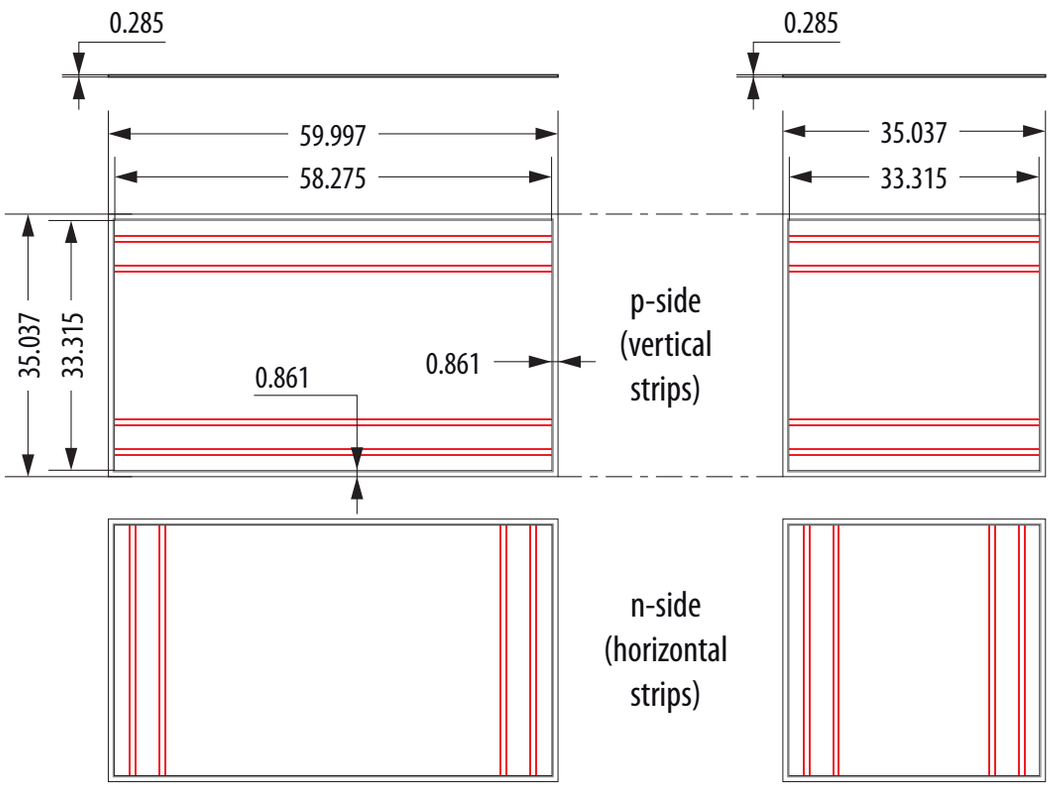


Figure 3.1: Dimensions of the sensor employed in the MVD strip barrel part (actual size; all figures are in mm). The outer dimensions, as well as the size of the active area, are indicated in the drawing. The double-rows of AC pads, pictured in red on both the p- and the n-sides of the sensors, are also drawn.

floating-strip technique, thus leaving every second strip disconnected, the use of one row within any of the four pairs is sufficient. In case one would like to connect the strips through the DC-coupled pads, both pad rows at the opposite sensor ends would have to be used; the floating strip technique simplifies the design, since only one row is then needed.

A bias ring, 110 μm wide, runs on both sides of the sensors immediately around the active area. In addition, around the bias ring on the p-side there are eight guard rings, for a total width of 200 μm. For the sensor operation and testing, the high voltage biasing must be provided through the bias rings on both sides of the sensor; the connection of the guard rings to the p-side high voltage would also be desirable.

All the sensors are (285 ± 10) μm thick. With this layout, each 4" wafer can accommodate one rectangular and one square sensor, plus several additional structures. In this way, a single set of masks is needed for the entire sensor mass production.

Two prototype runs and a first production batch were produced and a variety of tests were performed on them, including the measurement of the leakage current and of the full depletion voltage, the evaluation of the sensor capacitance and the studies of the radiation hardness. An overview of these measurements is presented in chapter 4.

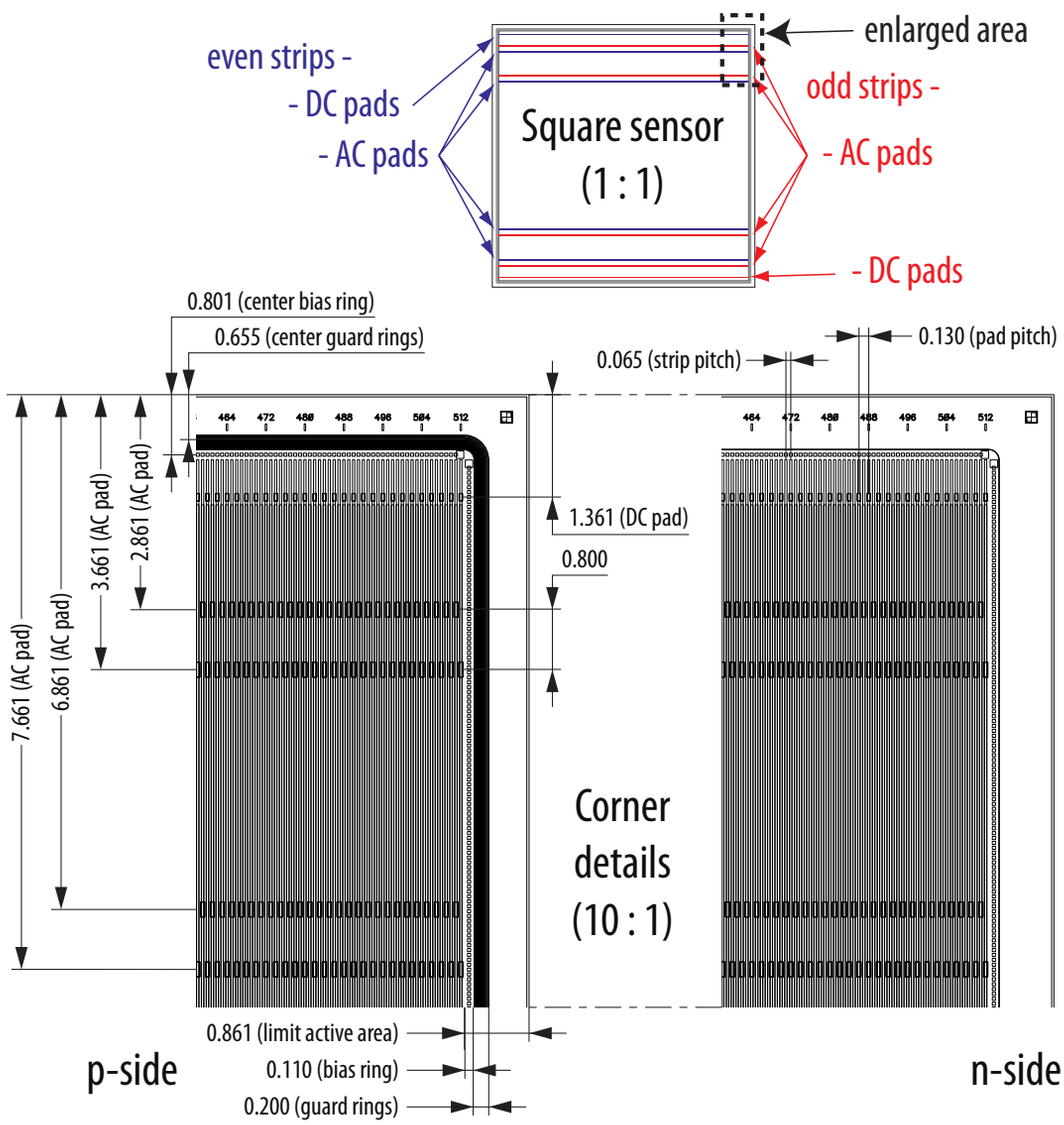


Figure 3.2: Features on the sensor corners; the individual strips with their AC and DC pads are visible, as well as the bias and guard rings. All figures are in mm.

3.2 READOUT ELECTRONICS

3.2.1 *PASTA: $\overline{P}$ANDA Strip ASIC*

The readout of the strip sensors in the $\overline{P}$ANDA MVD requires the use of a highly integrated front-end chip able to cope with the triggerless continuous data acquisition scheme of the experiment, as well as to withstand the expected radiation levels. Other critical requirements include a power consumption of less than 4 mW/ch, a dynamic input range between 10 and 35 pC, a charge measurement over this range with a resolution of at least 8 bit and a compact design.

Since no existing front-end chip fulfilling all these requirements could be found, the development of a custom solution, named PASTA ($\overline{P}$ANDA Strip ASIC), was chosen instead [107]. To simplify the development phase, the measurement concept and some parts of the ASIC design were adapted from the existing TOFPET chip, a self-triggering front-end developed for the EndoTOFPET-US project as a readout solution for scintillating crystals in a Time-of-Flight PET application [108, 109].

The main modifications from TOFPET to PASTA include a complete redesign of the analog front-end stage to cope with the different specifications of the sensors, the implementation of radiation hardness protection on both the analog and the digital part and the switch from a 130 nm to a 110 nm CMOS technology.

The measurement concept of the chip, based on the Time-over-Threshold (ToT) technique, is shown in figure 3.3. This method provides the information on the deposited charge by means of measuring the time when a signal stays above a certain threshold. In order to improve the time resolution, PASTA employs a dual threshold concept. A low threshold discriminator is used to measure precisely the beginning of the steep leading edge of a signal pulse. A second discriminator with a higher threshold measures the slower falling edge, thus providing the pulse length and the charge information [110].

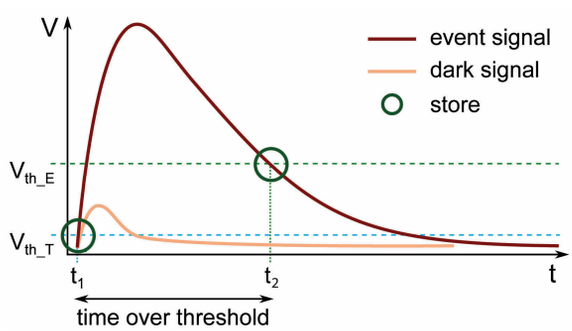


Figure 3.3: Measurement concept of PASTA.

The external clock of 160 MHz leads to an intrinsic time resolution of 6.25 ns; in PASTA, this is improved by using time-to-digital converters (TDC) with analog interpolators. A Time-to-Analog Converter (TAC) discharges a capacitor with a constant current between the threshold crossing and the transition of the clock; the charge is then transferred to a four times larger capacitor in the TDC stage, which is recharged with a current 32 times smaller. With these conversions an amplification ratio of

128 is reached, thus leading to a fine time resolution in the order of 50 ps. This process introduces a considerable dead time; in order to limit the pile-up effects, each discriminator is provided with four TAC stages which can buffer simultaneous events until they have been processed by the TDC.

A digital TDC controller is implemented in each channel and is used to select the TAC stage, to control the charge conversion and to transmit the timestamps to the global controller. This collects the signals from the 64 channels, distributes the configurations and transmits the data to the outside. The global architecture of PASTA is shown in figure 3.4.

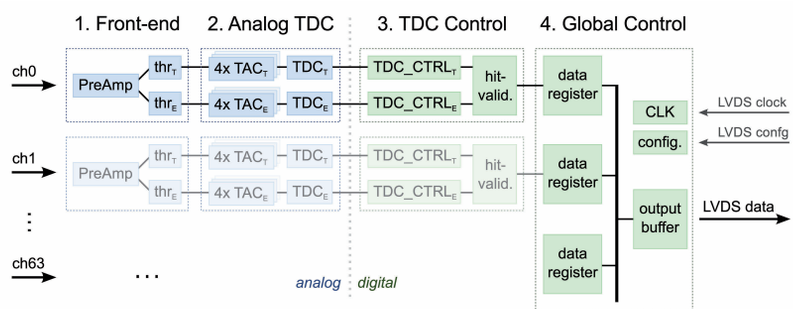


Figure 3.4: Block schematic of PASTA.

The final layout of the chip and the placement of the pads have been conceived taking into account both the requirements of the chip design and the constraints given by its application in the $\overline{\text{P}}$ANDA MVD.

The different sensors employed in the MVD have driven the decision towards the number of channels to be implemented in the chip. With the barrel sensors requiring 448 or 256 readout channels per side, and the trapezoidal sensors requiring 384 channels per side, a modularity of 64 channels per chip was chosen as the most convenient solution.

Given the dense arrangement of chips on both the disk and the barrel modules, a compact layout with a convenient form factor is mandatory for an efficient design of the detector modules. However, the requirements for the form factor in the barrel and in the disk part are somewhat different. In the barrels, the chips are arranged in a long row parallel to the long edge of the stave, as will be described extensively in the next section and in chapter 5. In this part it is mandatory to minimize the width of the chip (i.e., the extension in the direction perpendicular to the stave long edge) and to leave as much free space as possible behind the chip for routing purposes. In the disks, each of the modules hosts six chips per side and has a relatively small width of 33 mm, thus imposing a limit of approximately 5 mm on the chip length and favoring a more square design.

The final layout is a compromise between the different requirements and features a strip pitch of 63 μm, a length of 4.5 mm and a width of 3.4 mm, for a total area of 15.3 mm^2. A summary of the main properties of PASTA is presented in table 3.1.

Another important issue is the location of the chip's connection pins. The close placement of the chips next to each other in the disk modules exclude the possibility of having any type of pad on the two short sides of the chip; additionally, to simplify the layout of the FPC it is desirable to have all the I/O and power pads on the back-end side, leaving the front-end side dedicated exclusively to the analog inputs from the strip sensor.

The layout of the first PASTA prototype and its pad map, obtained taking into account these constraints, are shown in figure 3.5.

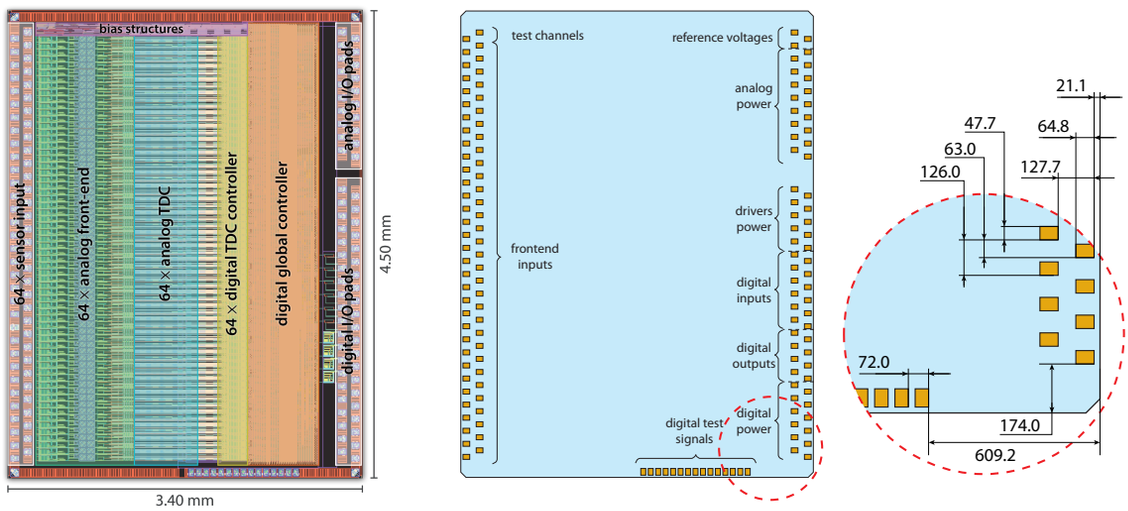


Figure 3.5: Layout of PASTA and map of its pads. Where not otherwise indicated, all figures are in μm.

On the front-end side there are the inputs of the 64 channels; additionally, two analog test pads are present. The back-end side hosts a total of 62 pads, divided in two categories: 10 differential pairs, 6 inputs and 4 outputs (20 pads in total), which provide the connection to the readout system, and the supply pads which provide the 1.2 V power supply to the analog and digital part, as well as the 2.5 V supply to the LVDS drivers. These have been implemented in the first prototype but will be replaced with SLVS drivers in the final version, thus removing the need for a separate supply. Additionally, three reference voltages are provided to the chip through dedicated pads. A third group of 15 pads, located on one of the lateral sides of the chips, allow to tap several digital signals inside the chip and are used for debugging. Since they will not be connected in the detector modules, their placement on the short side of the chip does not violate the design constraints.

On both ends of the chips, the pads are placed in two staggered rows, with a pitch of 63 μm between two consecutive pads (i.e., with a pitch of 126 μm between two nearby pads in the same row); each

Process technology	110 nm CMOS	Time binning	50 ps to 400 ps
Input clock frequency	160 MHz	Charge resolution	8 bit
Power consumption	256 mW	Number of channels	64
Input charge	10 pC to 35 pC	Die size	(3.4×4.5) mm^2
Input capacitance	< 38 fF	Radiation hardness	up to 100 kGy†
Max. input rate	≈ 100000 ev/s·ch		

Table 3.1: Review of the main design parameters of PASTA [110]. †Total Ionizing Dose.

pad has a size of $47.7 \times 64.8\ \mu m^2$. The probe pads are placed in a single row with a pitch of 72 μm. A detail of the chip corner, showing the position of the pads with respect to the chip edge, is shown in the bottom right corner of figure 3.5.

3.2.2 *MDC: Module Data Concentrator*

In the pixel detector, the ToPix readout chips are connected directly to the electro-optical transceivers in the service region. The adoption of a similar solution for the strip detector would be impractical, because it would require a very large number of data lines and transceivers; additionally, the low expected particle rate on the strip sensors means that the data lines would be used only up to a small fraction of the available bandwidth.

The adopted solution is to introduce an intermediate chip, the Module Data Concentrator (MDC), as close as possible to the PASTA front-ends. The MDC is connected to all the PASTA chips on one sensor and multiplexes the communication to them into a single data line. The chip is realized in the same 110 nm CMOS technology employed for PASTA [107].

In the disk part, the MDC has to collect the signals from six chips on each side, or 12 chips in total. The MDC was therefore conceived with 12 front-end inputs, since in the barrel part 11 and 8 inputs are sufficient for the rectangular and the square sensors, respectively.

Additionally, the MDC must be isolated from the high voltage present between the p- and the n-side of the sensor; to achieve this, an AC-coupling is foreseen on all the lines between the MDC and the PASTA front-end chips.

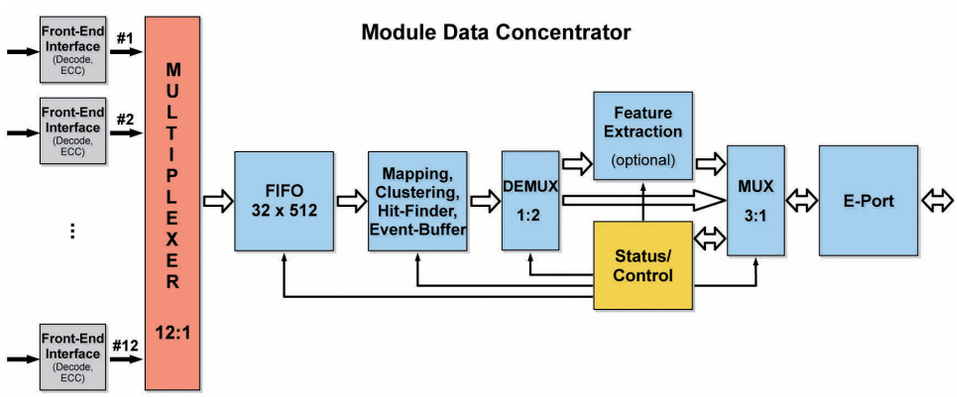


Figure 3.6: Block schematic of the MDC.

A block schematic of the MDC is shown in figure 3.6. The MDC must perform several tasks, starting from the time-ordering of the data coming from PASTA, to the multiplexing of signals from the different chips and to the 1D hit and cluster finding. In addition, the MDC can perform an optional 2D hit finding by measuring the charge correlation on the two sides, thus permitting a further reduction in the output data.

From the initial estimations, the expected power consumption of the MDC is in the order of 200 mW, with a chip size of $6 \times 6\ mm^2$ [111].

3.3 MECHANICAL STAVE SUPPORT

As briefly introduced in chapter 2, the sensors in the strip barrels are arranged in linear staves. In figure 3.7 a scheme of one complete stave is shown.

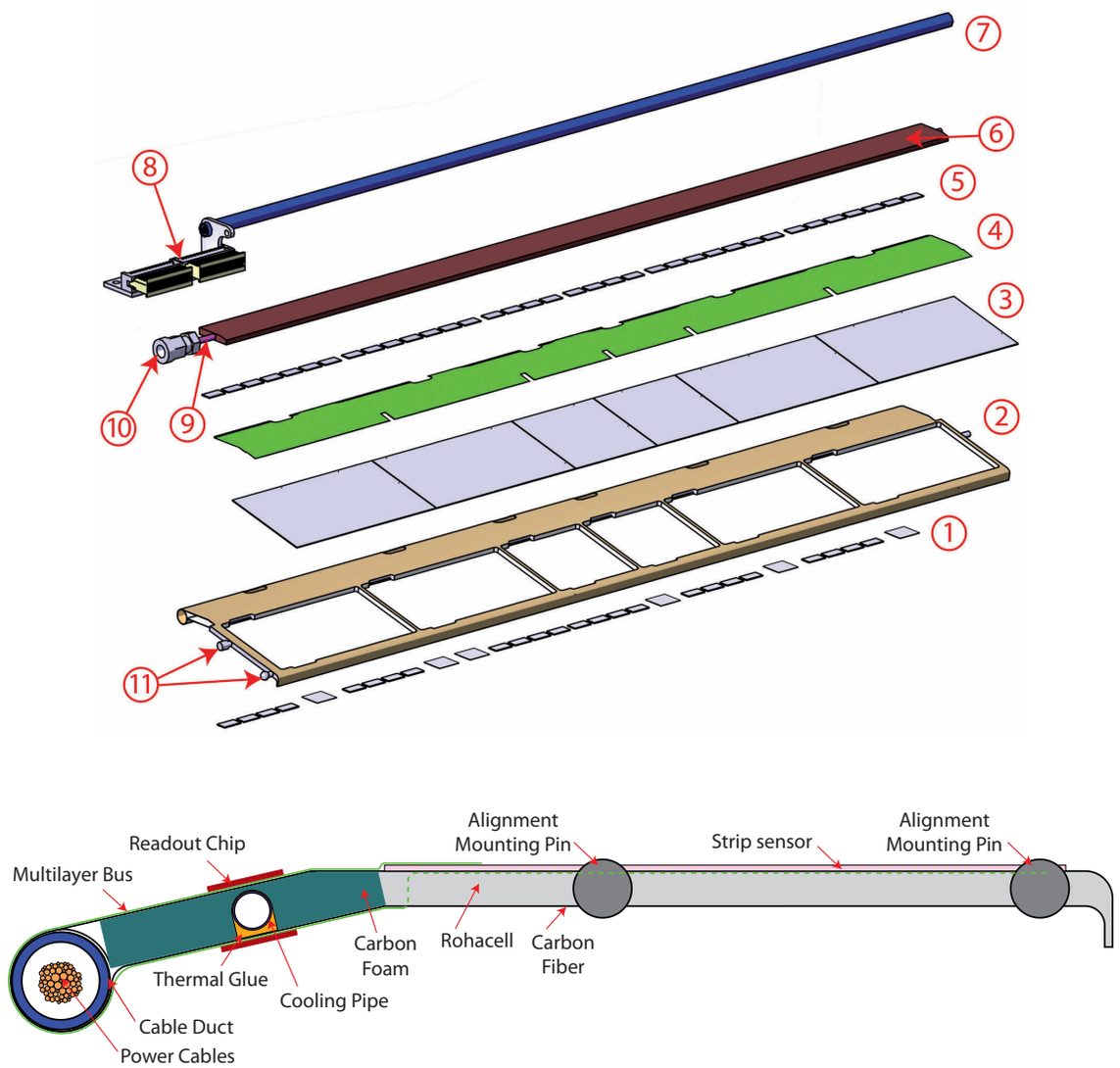


Figure 3.7: *Top:* exploded view of a fully equipped barrel stave, showing the relationship between the active elements and the mechanical support structures. (1) n-side PASTA and MDC chips; (2) carbon fiber stave; (3) sensors; (4) flexible printed circuit; (5) p-side PASTA chips; (6) carbom foam; (7) cable duct; (8) power connector; (9) cooling pipe; (10) plastic cooling connector; (11) alignment pins. *Bottom:* transverse view (see also figure 5.2).

Depending on the azimuthal position, each stave is equipped with a row of four to six strip sensors, both rectangular and square. All the relevant readout electronics is located on the stave next to the sensors, on a flexible printed circuit which is described extensively in section 5.1. The PASTA and the

MDC chips are arranged in a row parallel to the long edge of the stave. On the p-side, seven and four PASTA chips are placed next to each rectangular and square sensor, respectively. On the n-side, four PASTA and one MDC chips are placed next to each sensor, regardless of its size.

The core support component is a composite carbon fiber-based stave, which can be divided in two regions: the sensor part, mostly empty, which supports the strip sensors, and the electronics part, which implements the active cooling system and a duct for the power cables.

A schematic of one stave is presented in figure 3.8. The outer surface of the stave consists of a 200 μm layer of pre-preg 90°/0° Carbon Fiber Reinforced Plastic (CFRP). In the sensor region, the core is filled with a sheet of 2 mm Rohacell 51 foam, a proprietary polymethacrylimide closed-cell rigid foam with a density of 52 kg/m^3 [112].

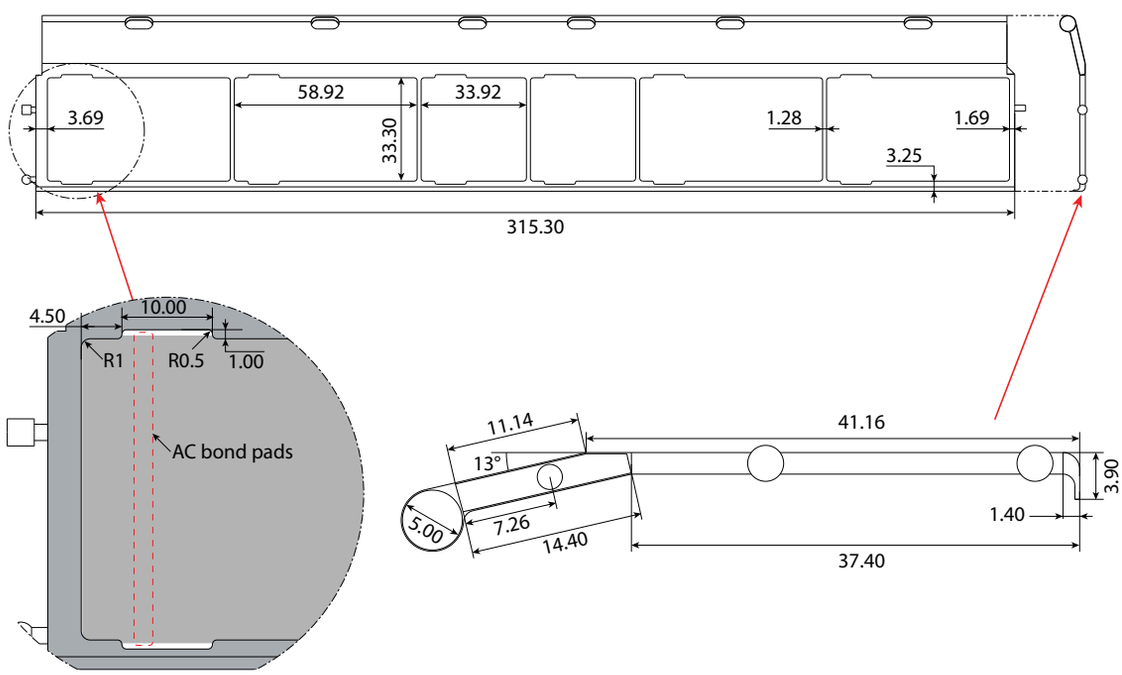


Figure 3.8: Schematic of a carbon fiber stave for the outer barrel; all figures are in mm. The staves in the inner barrel are shorter (280.10 mm), but share all the other specifications. The sensor cutouts implement two lateral recesses, required to access the bond pads of the strips at the edge of the sensor (the detail of one cutout, with the features of the strip sensor displayed for reference, is shown in the bottom left corner).

In the electronics region, the core of the stave must implement the active cooling system, designed to remove the excess heat from the readout electronics. The Rohacell foam is therefore replaced with carbon foam, a highly thermally conductive material. Two commercial foams, POCO HTC and POCO FOAM, have been considered for this application. The POCO HTC has a density of 0.9 g/cm^3 and an out of plane and in plane thermal conductivity of 245 and 70 W/m·K, respectively. The POCO FOAM has a density of 0.55 g/cm^3 and an out of plane and in plane thermal conductivity of 135 and 45 W/m·K, respectively [113]. The carbon foam is first cut in a block with a section of 15×4 mm^2 and a length equal to the length of the stave; the block is then machined to include the cooling pipe. This consists of a tube with a 2 mm external diameter and a wall thickness of 80 μm, fabricated in

MP35N, a nickel-cobalt-chromium-molybdenum alloy, by Minitubes [114]. A 2 mm hole is drilled in the foam through wire erosion; the tube is then inserted and fixed with thermally conductive glue. The cooling block is then pressed between the two layers of carbon fiber, together with the Rohacell core of the sensor part and with the cable duct, realized with a circular carbon fiber tube with an outer diameter of 5 mm. Additionally, two reinforcement plates fabricated in Polyether Ether Ketone (PEEK) or other similar plastic are inserted in the rims at the extremities of the stave and serve as mounting and alignment points.

The stave is then milled to realize the cutouts of the sensors and the accesses to the cable duct (two per sensor, one on each stave side). The cooling pipe is attached to a custom connector fabricated in Ryton R4 [66]; an electrical connector, featuring between 32 and 48 pins, is also attached to the stave edge and is used to connect the stave power cables. The study of the powering scheme of the staves and of the routing of the power cables will be presented in section 5.3; in particular, the listing of the cables that have to be routed through the stave cable duct is shown in table 5.10.

Several photographs of stave prototypes at various stages of construction are shown in figure 3.9.

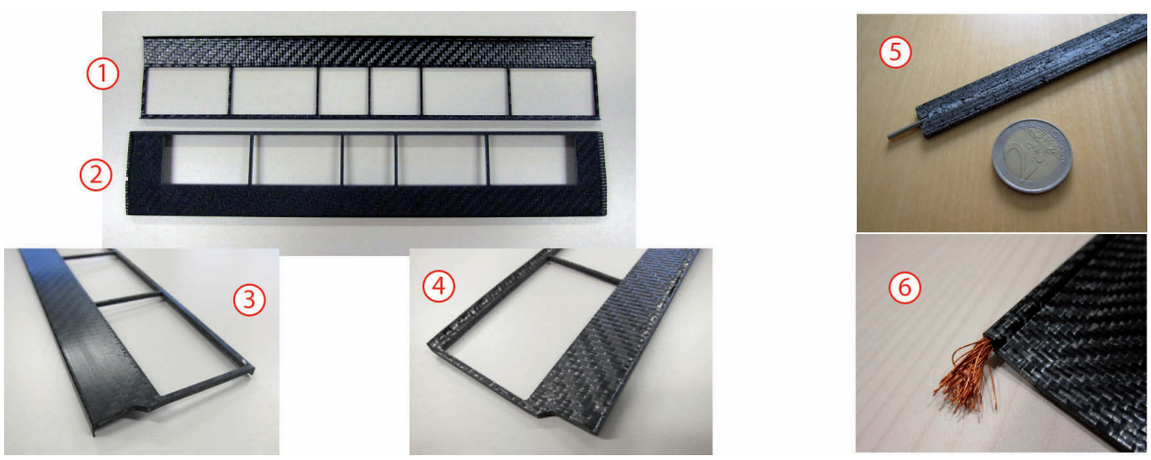


Figure 3.9: Construction prototypes of carbon fiber staves. (1) and (2) standard staves for the outer and the inner barrels, respectively (the latter has not yet been cut to its final length); (3) and (4) details of the sensor cutouts seen from the upper and the lower side of the stave; (5) detail of the cooling block, including the carbon foam and the cooling pipe; (6) detail of the cable duct with several enameled copper wires of different diameters.

Besides the standard staves, such as the one presented in figure 3.8, special ones are foreseen at the top and at the bottom of both barrels, to accommodate the vertical target pipe. These staves lack one square sensor at the center and may require a complicated arrangement of the cooling pipe and of the cabling. A total of six stave designs are therefore foreseen for the entire strip barrel part of the MVD, with the special staves of each barrel further differentiated in a left and a right version. A schematic comparison of the six designs is presented in figure 3.10 and in table 3.2 (the arrangement of the various stave types on the two barrels, described in the following, is visible in figure 3.11).

A total of 46 staves (20 in the inner barrel and 26 in the outer one) compose the entire strip barrel part of the MVD. A small overlap in the acceptance area of the sensors of two adjacent staves is achieved through a paddlewheel arrangement of the staves. As a consequence, the surface of the sensors is not normal to the barrel radius, but is tilted with an angle of 12° and 10° in the third and fourth

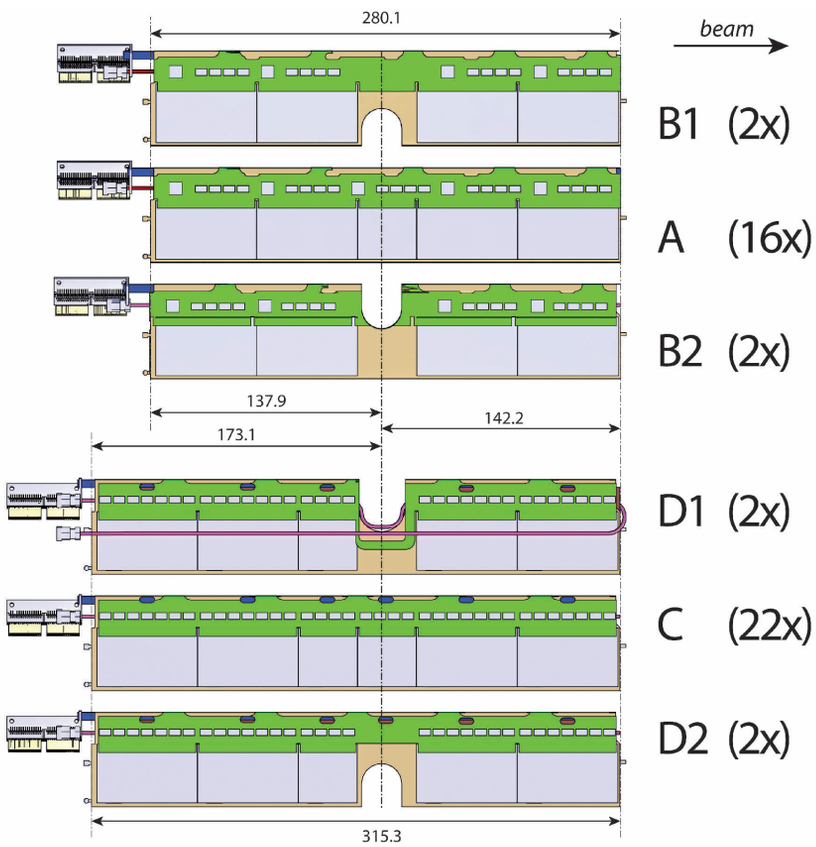


Figure 3.10: Comparison of the six different stave designs. The staves at the top and at the bottom feature a missing sensor and a U-shaped cutout with a radius of 12 mm in the carbon fiber stave, centered around the axis of the target pipe. All figures are in mm.

Stave type	Number of staves	Number of sensors rectangular	Number of sensors square	Number of chips PASTA	Number of chips MDC	Stave length [mm]
Barrel 3 standard (A)	16	4	1	52	5	280.1
Barrel 3 special (B1/B2)	4	4	0	44	4	280.1
Barrel 4 standard (C)	22	4	2	60	6	315.3
Barrel 4 special (D1/D2)	4	4	1	52	5	315.3

Table 3.2: Review of the six stave types in the two strip barrels. The special staves are foreseen at the top and the bottom of the two barrels, around the vertical target pipe.

barrels, respectively. A common cylindrical support, realized with two layers of CFRP filled with Rohacell, acts as the main holding structure for both barrels. Four sawtooth supports are placed on the cylinder, two on the inner side at $z = -141.4$ mm and $z = +143.75$ mm and two on the outer side at $z = -176.8$ mm and $z = +143.75$ mm. The staves of the third and fourth barrels are connected to

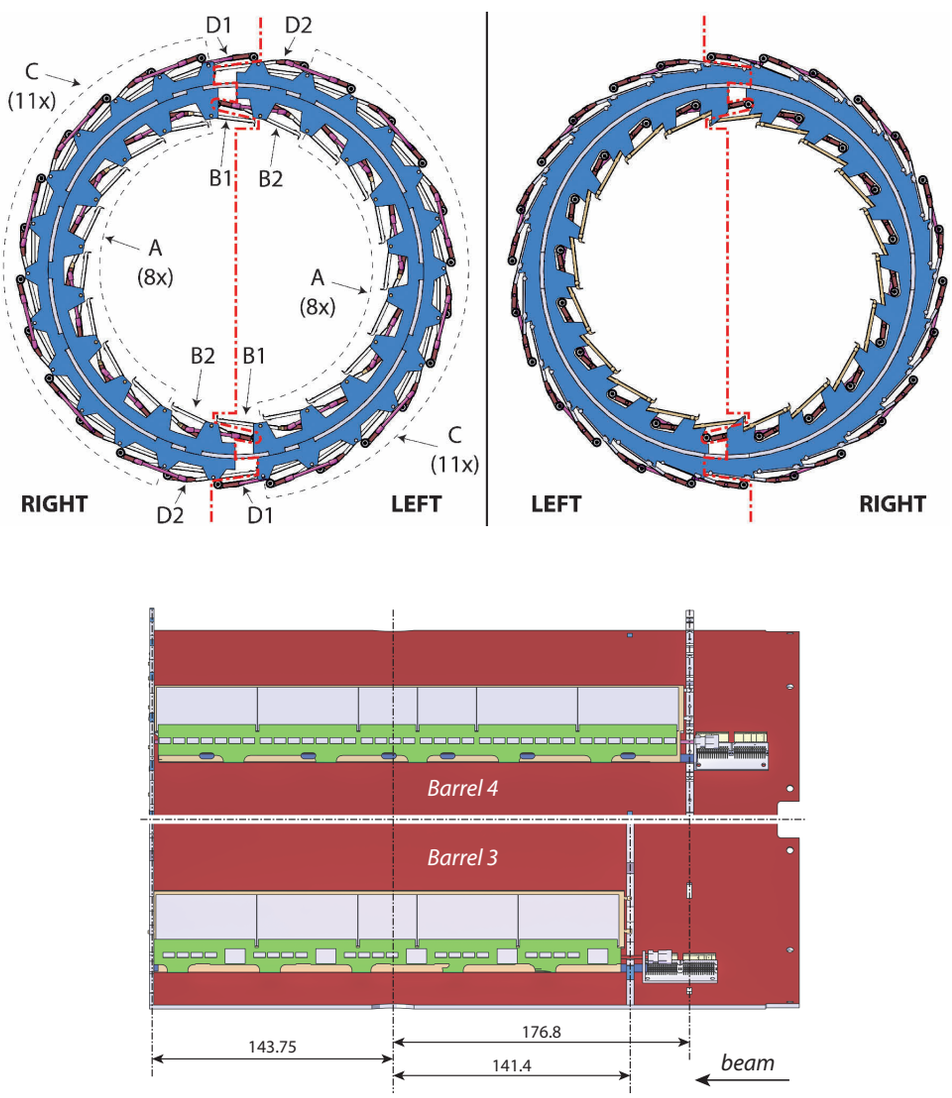


Figure 3.11: *Top:* cross section of the two strip barrels, highlighting the downstream (*left*) and upstream (*right*) sawtooth mounting structures. The position of the six stave types is also indicated. The two detector halves are identical: when one half barrel is rotated by 180° and mounted next to the other half, the B1 and D1 staves on one side are coupled to the B2 and D2 staves on the other. The boundary between the two halves is indicated with a red dotted line.
Bottom: longitudinal position of the sawtooth supports, with respect to the target pipe axis. All figures are in mm.

the inner and outer sawtooth supports, respectively; each sawtooth support is equipped with alignment pins matched to the ones implemented on the stave extremities.

The position of the sawtooth structures on the two barrels along the longitudinal axis is visible in figure 3.11. A cross section of the two strip barrels, showing the structure of the inner and outer sawtooth supports and the arrangement of the staves, is visible as well in figure 3.11.

Finally, the position of the staves in the two barrels with respect to the holding cylindrical support, as well as the clearances between adjacent staves, are shown in figure 3.12.

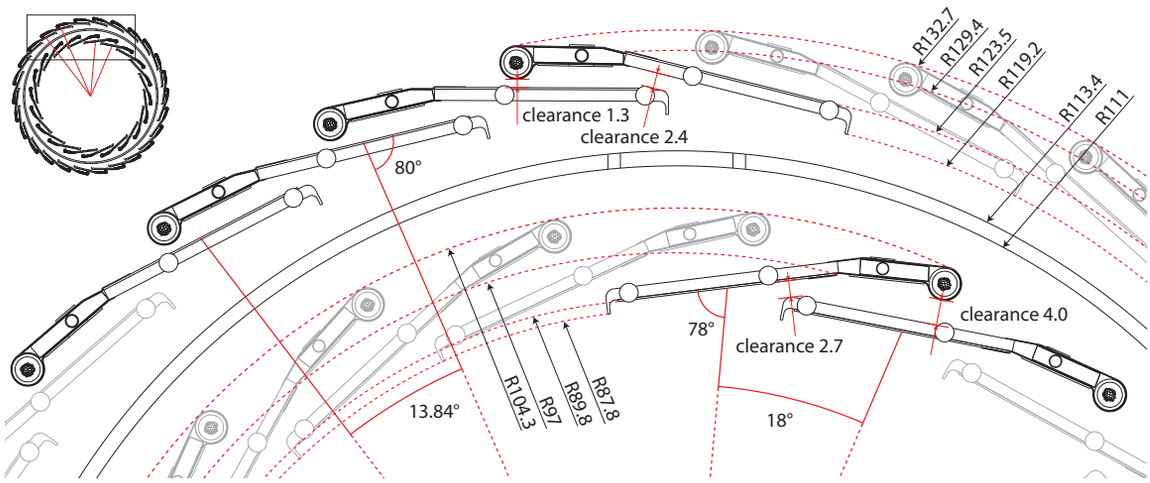


Figure 3.12: Relative position between adjacent staves in the strip barrels and between the staves and the cylindrical support. All figures are in mm.

4

DOUBLE-SIDED SILICON STRIP SENSORS

The double-sided silicon strip sensors used in the $\overline{\text{P}}$ANDA MVD have been briefly introduced in section 3.1.

Two sensors prototype runs were produced; in this chapter, an overview of some measurements performed on these prototypes is presented, along with a description of the experimental tools used and developed for the task.

4.1 Test Tools for Strip Sensors

For the sensor measurements presented in this chapter, several different tools are required. Those described in the following belong to two main categories: the setup for the characterization of the sensor properties via electrical measurements and the irradiation setup for the studies of the radiation hardness.

4.1.1 *Sensor characterization setup*

4.1.1.1 *Probe station and probe PCB*

The performance of systematic studies of the sensors requires the use of a dedicated setup for the electrical connection of the various structures on the sensor.

Depending on the quantities that have to be measured, the connection can be achieved in different ways. A first technique requires the use of a probe station as the one visible in figure 4.1. The sensor under test is placed on a motorized metal plate (chuck) and held by a vacuum system; on the top side, several removable needles are used to electrically connect the structures to be tested. The needles are controlled by means of manual micromanipulators, which allow for a precise placement on the desired pads.

The chuck of the probe station is electrically conductive and can be used to provide a contact to the back side of the device under test; this is particularly useful to provide the high voltage biasing to single-sided devices, such as the diodes studied in appendix A. In case of double-sided strip sensors, however, a large number of different pads are implemented on the back side, rendering the chuck

electrical connection unusable: in this case, an insulator layer must be placed between the sensor and the chuck.

An important limitation of the probe station setup is that, because of its layout, only the pads on one side can be connected at any given time, thus narrowing the range of available measurements. Additionally, the simultaneous connection of a large number of pads is awkward and is ultimately limited by the number of needles available (six on the device used for these studies).

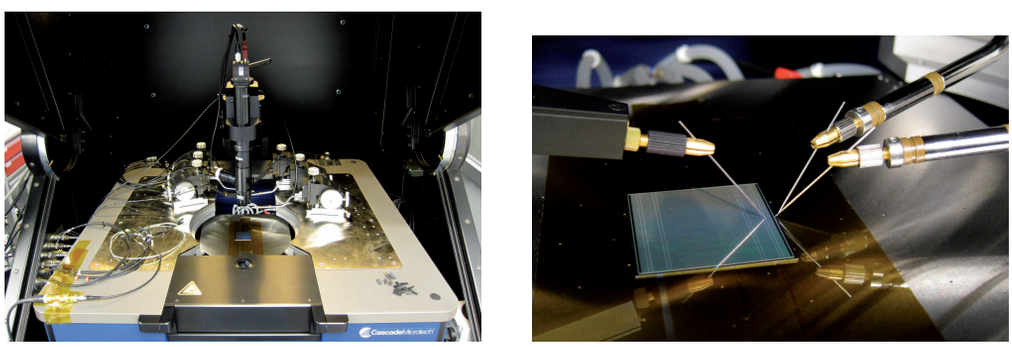


Figure 4.1: Probe station setup (*left*) and square strip sensor connected with 3 needles (*right*). A layer of kapton is used to insulate the sensor back side from the chuck; the kapton is perforated to maintain the vacuum holding system functional.

A second possible connection technique requires the use of a printed circuit board (PCB), onto which the sensor can be glued and connected by means of wire bonding. With respect to the probe station setup, the pads on the back side can be easily accessed as well; additionally, a much larger number of connections can be performed, e.g. to all the strips on one or both sides of the sensor. It can be therefore used to perform a wider set of measurements. An example of one such probe PCB, equipped with a $\overline{\text{P}}$ANDA prototype square sensor, is visible in figure 4.2.

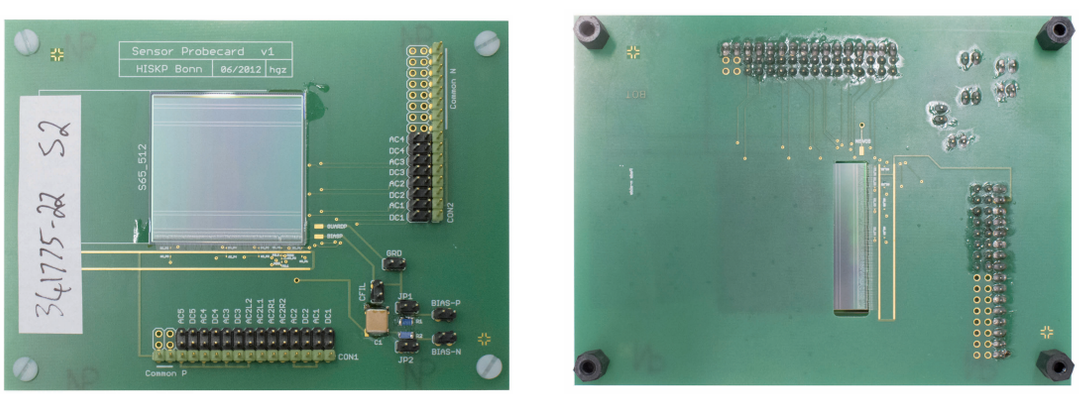


Figure 4.2: Probe PCB equipped with a square strip sensor. *Left:* top view (p-side); *right:* bottom view (n-side). The PCB provides on each side a common line to bond many strips in parallel; additionally, the AC and DC pads of five strips per side can be bonded separately to dedicated pads. The sensor biasing pads are implemented as well.

The extended measurement capabilities come at the expense of the need for a dedicated PCB, whose design must be tailored to the sensor under study. Moreover, once glued on the PCB the sensor must normally be discarded since its retrieval is in most cases impossible; this technique is therefore not appropriate for large scale, nondestructive testing.

4.1.1.2 *Electrical measurement setup*

Regardless of the technique used for connecting the sensors, the electrical measurements are performed with two separate devices. The first is a Sourcetronic ST2819 LCR-Meter, which is used to measure precisely the inductance, capacitance and resistance of the device under test. The second device is a high voltage Iseg SHQ 124 power supply, used to provide the sensor biasing.

The LCR-Meter features four ports, two of which providing an AC-stimulus to the device under test and the other two measuring the voltage at the device. A biasing box containing four carefully matched capacitors is used to protect the LCR-Meter inputs from the external high voltage. The biasing box contains also an R-L network that allows to connect the high voltage power supply to the same measuring needles, without influencing the device under test with the power supply impedance [100]. This connection scheme, shown in figure 4.3, is used for measurements of global sensor properties. Different measurements, such as single strip and coupling capacitances, require a different connection setup which is described in the relevant section.

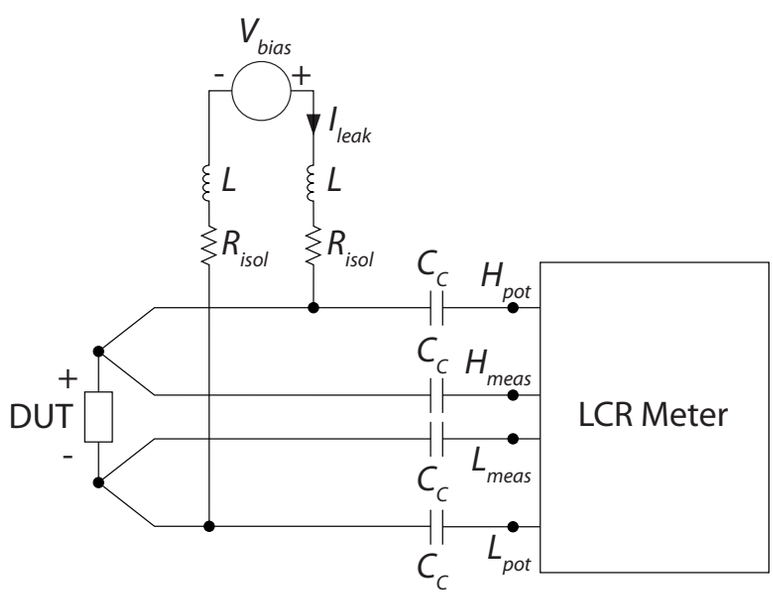


Figure 4.3: Biasing box for measurements of global sensor properties. The H_{pot} and L_{pot} terminals of the LCR-Meter provide an AC stimulus to the Device Under Test (DUT), while H_{meas} and L_{meas} measure the resulting voltage. The four C_C capacitors have a nominal value of 100 nF and are used to protect the LCR-Meter from the high voltage applied on the sensor. The leakage current I_{leak} is measured by the high voltage power supply, which is connected to the potential terminals through an R-L network.

4.1.2 *Irradiation setup at the Bonn cyclotron*

During the experiment operation, the strip sensors will be exposed to significant radiation levels, which can prove harmful to their performances. The expected radiation load in the various layers of the detectors has been evaluated [66]; according to the simulations, all the elements of the strip detector must be able to withstand a load of up to $3.5 \cdot 10^{13}$ $n_{1MeV\,eq}\,cm^{-2}$ of non-ionizing radiation over the entire $\overline{P}$ANDA lifetime. A good understanding of the sensor behavior after being exposed to radiation is therefore of the utmost importance.

The effect of the accumulated radiation has been studied by irradiating the sensors with 14 MeV protons at the Bonn Isochronous Cyclotron [115]. A dedicated experimental setup for the irradiations has been prepared inside the scattering chamber provided at the "high current area" at the cyclotron [116]. A schematic and a photograph of the experimental setup are visible in figure 4.4.

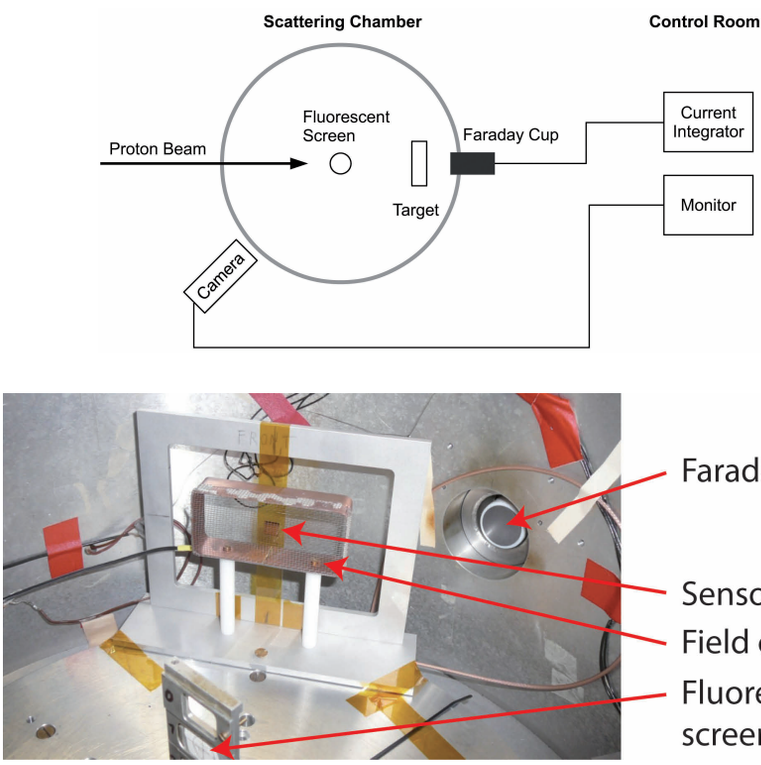


Figure 4.4: *Top:* Schematic of the irradiation setup. *Bottom:* Photograph of the irradiation setup inside the scattering chamber, showing the sample holder with a small strip sensor supported by the kapton tape, the field cage in front of it, the fluorescent screen and the Faraday cup.

The target is mounted on a rotatable platform inside the chamber, in front of the beam line opening from which the proton beam enters the chamber. The whole scattering chamber is kept in vacuum during the beam operation to minimize the proton scattering. A removable flourescent screen can be inserted without breaking the vacuum to monitor the position, shape and dimension of the beam spot; the interior of the chamber can be watched from the control room through a video camera.

The sample is suspended in the center of a metal frame through some kapton tape, thus minimizing the passive material exposed to radiation. The protons impacting the sensor can cause static discharge to the scattering chamber walls; to prevent this, a metal field cage is placed in front of the sample and is connected to a negative potential of 200 V.

A Faraday cup placed behind the sample and connected to a charge integrator is used to evaluate the applied proton fluence Φ_p, measured in cm^{-2}. This can be calculated through

$$\Phi_\mathrm{p} = \frac{C_\mathrm{cup}}{A \cdot e}, \tag{4.1}$$

where C_cup is the integrated charge collected by the Faraday cup, measured in Coulomb, A is the area of the cross section of the beam in cm^2 and e is the charge of the proton.

From this, the NIEL scaling hypothesis allows to calculate the neutron equivalent fluence Φ_n applied to the sensors, measured in $\mathrm{n}_{1\mathrm{MeV\,eq}}\,\mathrm{cm}^{-2}$ [117]. This is defined as

$$\Phi_\mathrm{n} = \Phi_\mathrm{p} \cdot K, \tag{4.2}$$

where Φ_p is the proton fluence in cm^{-2} and K is the hardness factor, obtained from scaling the values in figure 4.5. For 14 MeV protons, $K = D_{\mathrm{p\ 14\ MeV}} / D_{\mathrm{n\ 1\ MeV}} \approx 3$.

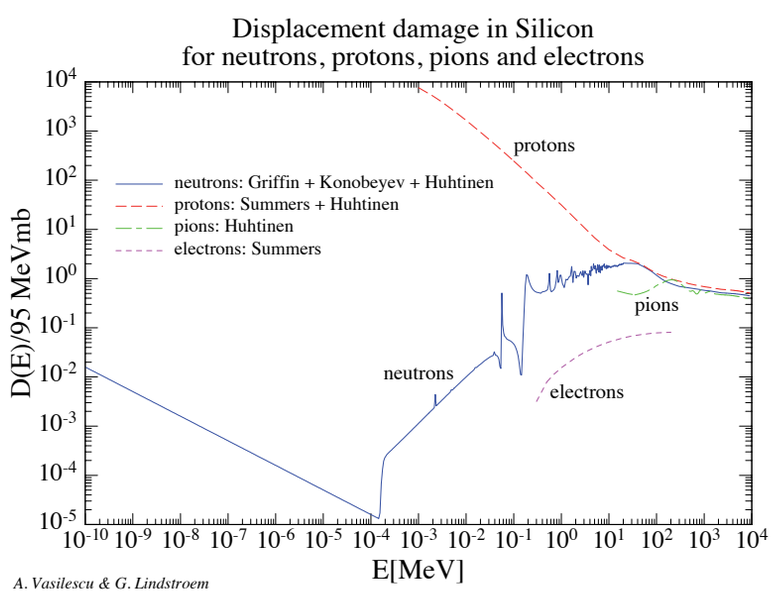


Figure 4.5: Hardness factor K of different particles, defined as the displacement damage cross section normalized to $\mathrm{D}_{\mathrm{n\ 1\ MeV}} = 95$ MeV mb, i.e., to the displacement damage cross section for 1 MeV neutrons [118].

The uncertainty σ_Φ on the equivalent fluence is derived through error propagation from the uncertainties on the integrated charge and on the beam spot area, with the latter playing the largest role. An additional uncertainty, which is however hard to estimate because of the lack of a beam monitoring device, comes from the uneven flux profile over the beam spot area.

4.2 CHARACTERIZATION OF THE SENSORS

4.2.1 *Sensor prototypes*

A first full-size prototype run was produced in 2011 by the company CiS in Erfurt, Germany [119]. The starting material is an n-doped silicon ingot, fabricated with the Floating Zone (FZ) technique, with a diameter of 4". The ingot is cut in wafers with a thickness of 285 μm, with a <111> orientation. The manufacturer uses a 10-layer process with single metal and passivation layers; the wafers are processed through several photolitographic and etching steps to implement the desired structures [100].

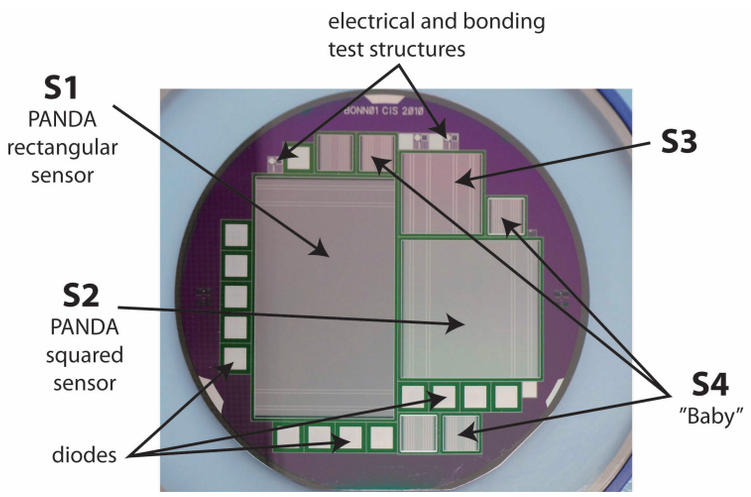


Figure 4.6: Wafer map, showing the different structures implemented on the 4" wafer.

A photograph of one wafer, showing the most important features implemented on it, is shown in figure 4.6. Each wafer contains a rectangular and a square $\overline{\text{P}}$ANDA full-size sensor, together with another square sensor with a strip pitch of 50 μm and an active area of 19×19 mm^2 compatible with the preexisting readout architecture [120] and five "Baby" sensors with an active area of 8×8 mm^2. Additionally, 14 diodes and several electrical and bonding test structures are implemented as well.

The front and back side strips are realized with p^+-in-n and n^+-in-n implants, respectively. The strips can be connected with DC and AC pads implemented on the sensors; the location and type of these pads has been described in section 3.1. The figures stated in figure 3.2 are valid for all sensors except the "Baby" type, on whom the AC pad rows are closer to the die edge. The charge separation on the n-side is realized by means of a p-spray isolation and the active area of the sensor is surrounded by eight concentric guard rings. The reverse biasing of the sensors is achieved by means of the punch-through scheme. In this technique, the p-strips are initially insulated from the guard ring; the application of a potential to the ring creates a depletion region that gradually expands until reaching the strip implants and covering the entire sensor.

A second prototype run was produced in 2013 to explore a different biasing technique. Here the biasing is achieved by means of high impedance polysilicon resistors between the bias ring and each

strip implant; the use of polysilicon requires however an additional process layer during the fabrication. Besides the biasing scheme, all the other design characteristics of the sensors remained unchanged between the two prototype runs. A photomicrograph of the p- and n-side corners of sensors from both prototype runs, highlighting the different biasing structure, is visible in figures 4.7 and 4.8.

A summary of the main properties of the prototype sensors is presented in table 4.1.

General properties			
Wafer material	FZ Si, n / P	n-side isolation	p-spray
Wafer diameter	4”	Guard rings	8
Thickness	(285 ± 10) µm	Stereo angle	90°
Resistivity	$2.3 - 5.0$ kΩ · cm	Passive rim	860 µm

Prototype sensors				
	Sensor S1 $\overline{\text{P}}$**ANDA rect.**	**Sensor S2** $\overline{\text{P}}$**ANDA square**	**Sensor S3**	**Sensor S4 “Baby”**
n-side / p-side strips	512 × 896	512 × 512	384 × 384	128 × 128
Pitch / width [µm]	65 / 30	65 / 30	50 / 20	65 / 30
Active area [mm^2]	58.275 × 33.315	33.315 × 33.315	19.230 × 19.230	8.355 × 8.355

Table 4.1: Properties of the prototype strip sensors.

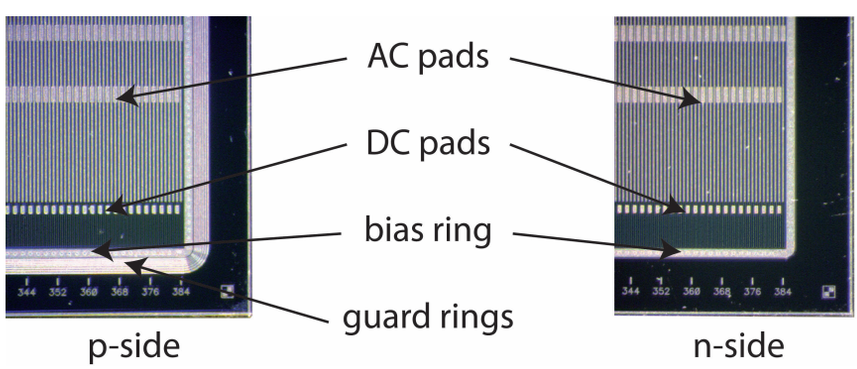


Figure 4.7: Photomicrographs of the corner of one sensor, showing the different structures implemented on the p- and on the n-side.

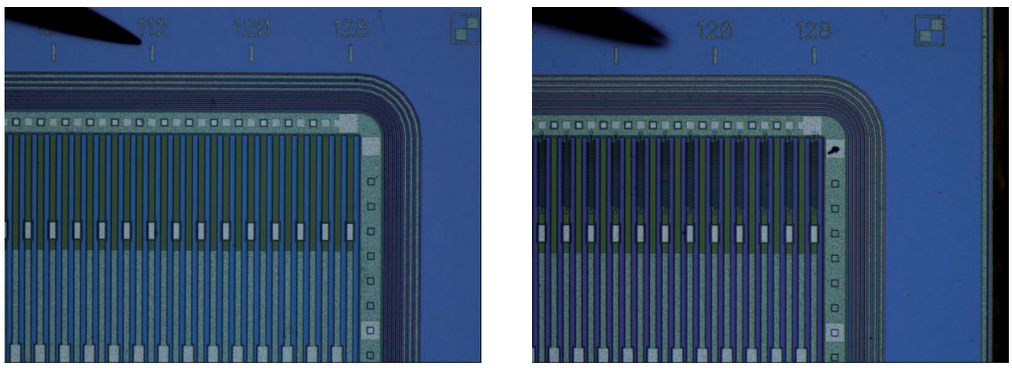


Figure 4.8: Photomicrograph of a sensor corner, showing the area on the p-side between the bias ring and the strip implants, for a sensor with punch-through (*left*) and one with polysilicon (*right*) biasing, with the polysilicon resistors clearly visible in the latter.

4.2.2 *Electrical characterization*

When using the LCR-Meter to measure a complex system such as a double-sided strip sensor, certain assumptions must be made in order to describe it with a simple model. Referring to the two-port model depicted in figure 4.9 on the left hand side, the small capacitance of the sensors implies that the effect of the series resistance R_s is negligible with respect to the effect of the parallel resistance R_p. The model can therefore be well approximated by a parallel $C_p - R_p$ model, as shown in figure 4.9 on the right hand side.

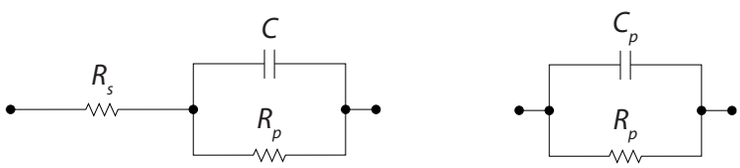


Figure 4.9: Generic two-port model used to describe a device with a complex impedance Z (*left*) and simplification in a parallel model under the assumption that the series resistance R_s is negligible (*right*).

In order to estimate the reliability of the measurement, it is useful to introduce the dissipation factor D, which is defined as

$$D = \tan\delta = \frac{\mathrm{Re}\,(Z)}{\mathrm{Im}\,(Z)} = \frac{1}{\omega C_p R_p}. \tag{4.3}$$

For the measured impedance Z to approximate correctly the true capacitance of the device, D should be small; when this is not the case and D approaches 1, the description of the device through the simple parallel model is less reliable and so are the capacitance measurements.

4.2.2.1 *First prototype run (punch-through biasing)*

The sensors from the first prototype run, produced in 2011, were thoroughly tested for a variety of properties. The full results of these characterizations are extensively presented in [100] and briefly summarized in the following.

The leakage current is the first important parameter to be studied; on the probe station, the sensor is connected following the scheme shown in figure 4.3 with one needle on the bias ring and the other needle on the bulk. In addition, the manufacturer provided a leakage current measurement on each of all delivered sensors; in figure 4.10 the leakage current behavior of the 25 rectangular sensors produced in the prototype run is shown. All sensors but two show a leakage current in the depletion region between 1 and 5 μA and a breakdown voltage of at least 200 V and often significantly higher [100, 121, 122].

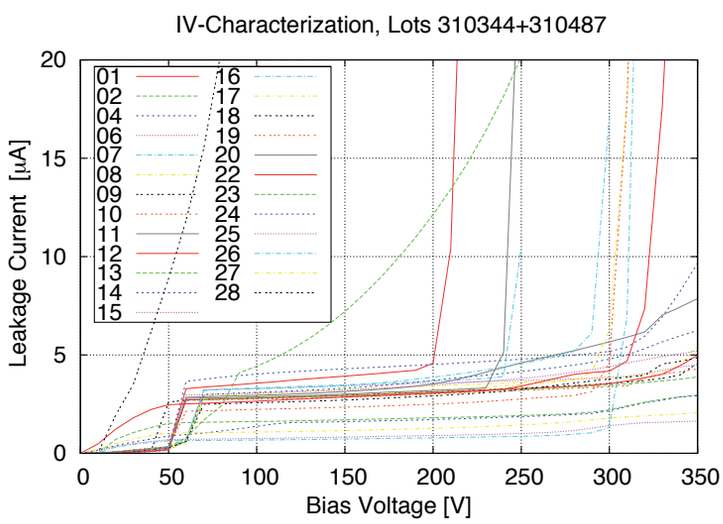


Figure 4.10: First prototype run - leakage current of 25 rectangular sensors as provided by the manufacturer [119].

A strip sensor is a complex system and a full characterization requires the measurement of several capacitance values; a comprehensive treatment of the quantities involved is available in [100].

The back side capacitance c_b is measured with all the p-side strips connected to one port of the LCR-Meter and all the n-side strips connected to the other port; this connection scheme is only feasible on the probe PCB. The C-V curve, shown in figure 4.11, yields a body capacitance of $c_{\text{body}} = (683.5 \pm 1.5)$ pF. This can be divided by the number of strips to obtain the back side capacitance of a single strip, whose values are $c_{b_{\text{p}}} = (0.7628 \pm 0.0017)$ pF and $c_{b_{\text{n}}} = (1.3350 \pm 0.0029)$ pF for the p- and n-side, respectively.

The measurement of the interstrip capacitance $c_{i,n}$, which represents the coupling of one strip to the first n neighboring strips on the same side, can be performed on the probe station setup, but only for a very small number of neighbors. Similarly, the coupling between two adjacent strips c_{is} can be also easily measured on the probe station. Complementarily, on the probe PCB it is possible to study the coupling of one strip to an arbitrary large number of neighbors, up to the limit case of $c_{is,\infty}$, where

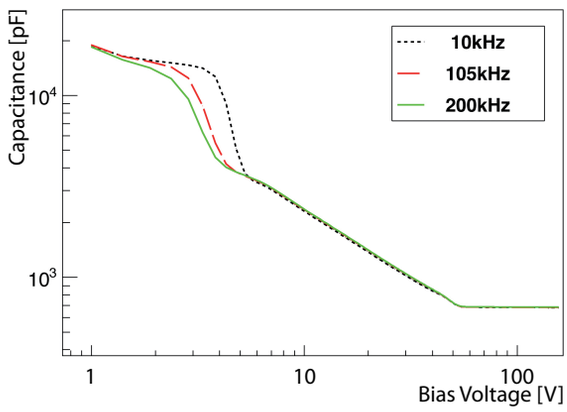


Figure 4.11: First prototype run - body capacitance.

one contact of the LCR-Meter is connected to the strip under test and the other to a common line onto which all the other strips on the sensor are connected. Values of $c_{is,\infty}$ in the order of 2.8 pF/cm were measured on the prototype sensors [100, 121, 122].

The use of AC coupled readout pads introduces a coupling capacitance, which depends on the strip geometry and on the thickness of the oxide layer separating the strip implant and the overlaying metal contact strip. It can be measured by connecting the contacts of the LCR-Meter to the AC and DC pads of the same strip. The coupling capacitance has a very strong dependence on the frequency of the AC stimulus provided by the LCR Meter; the low frequency limit is usually considered the best approximation of the true capacitance [100]. In order to avoid excessive drainage of the charge into neighboring strips, large values of the coupling capacitance are desired. The measurements of the sensors in the first prototype run yielded values of $c_{c_p} = (54.0 \pm 1.5)$ pF/cm and $c_{c_n} = (46.3 \pm 0.9)$ pF/cm for the p- and n-side, respectively.

Finally, connecting the LCR inputs to one AC pad and to the bias ring on the same side allows to measure the stray capacitance between the strip and the bias and guard rings. From this C-V characteristic it is possible to evaluate the depletion voltage. The capacitance drops steeply as the rising of the bias voltage leads to an enlargement of the depleted region. After the full depletion, the capacitance stays almost constant or decreases slightly; a double straight line fit can be performed before and after the kink occurring at the full depletion. The intersection of the two lines defines the full depletion voltage.

The knowledge of the body, interstrip and stray capacitance allows to calculate the capacitance seen by the front-end electronics [100]. On a rectangular sensor, this is in the order of 10 pF for the p-side and of 17 pF for the n-side [121].

4.2.2.2 *Second prototype run (polysilicon biasing)*

The second prototype run, featuring polysilicon resistors biasing, was fabricated in 2013. Two square sensors belonging to different lots from the run were characterized with the probe station setup. A variety of measurements were performed, with the goal of comparing the sensors produced with the two

biasing techniques, as well as evaluating the uniformity between the two lots [123]. The measurements included:

- strip's AC pad to chuck (figure 4.12). A three needles setup was used to connect the sensors: the high voltage bias was provided through one needle on the bias ring and one on the bulk and the capacitance was measured between the strip's AC-pad, connected through a needle, and the chuck. The back side of the sensor is isolated from the chuck through a layer of kapton; therefore the capacitance measured is not exactly the body capacity c_b, which can only be acquired through the probe PCB setup, but it is a good approximation [124].
- global I-V curve, acquired through the high voltage power supply (figure 4.13);
- coupling capacitance, measured between the AC and the DC pad of the same strip (figure 4.14);
- interstrip capacitance between first and second neighboring strips, measured between the respective AC pads (figure 4.15).

The following figures compare the results obtained for the two sensors; the left and right figures refer to lots n. 330005 and 330352, respectively.

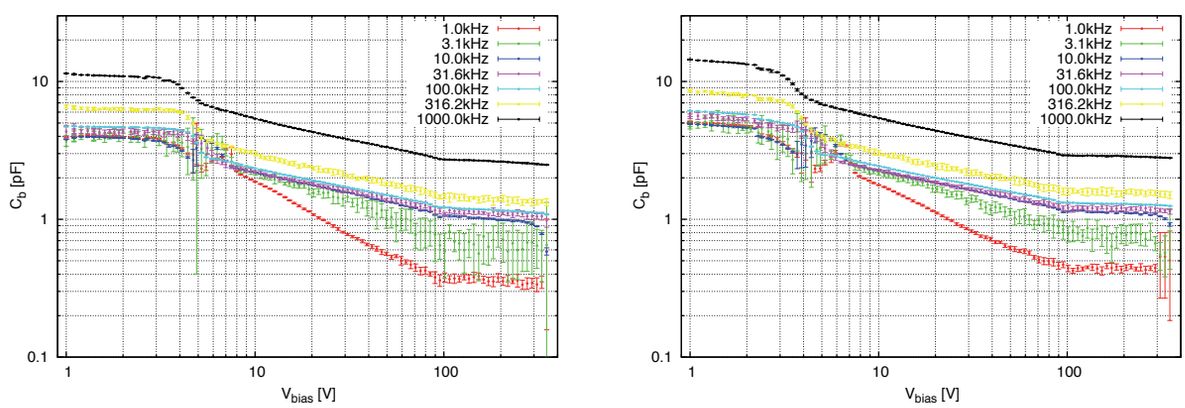


Figure 4.12: Second prototype run - strip to chuck capacitance. In both cases, the depletion voltage occurs slightly below 100 V; the two curves acquired at the lowest frequencies should be discarded because of their high D value. At the intermediate frequencies, a capacitance at the full depletion between 1 and 2 pF is observed.

The matching between the sensors from the two fabrication lots is excellent and virtually no difference can be observed.

The behavior of the sensors from the punch-through and the polysilicon biasing batches is similar, albeit with a few differences. The most important is the higher depletion voltage observed (around 100 V, instead of 50 V observed in the first batch), which is caused by the lower resistivity (5.2 $k\Omega \cdot cm$ for the first batch and 2.8 $k\Omega \cdot cm$ for the second) and does not depend on the biasing technique. The measured values of the body and coupling capacitances are very similar, as well as the leakage current, which remains well within acceptable limits.

The electrical studies therefore show that the choice of the biasing technique does not influence in an appreciable way the parameters that characterize the operation of the sensors.

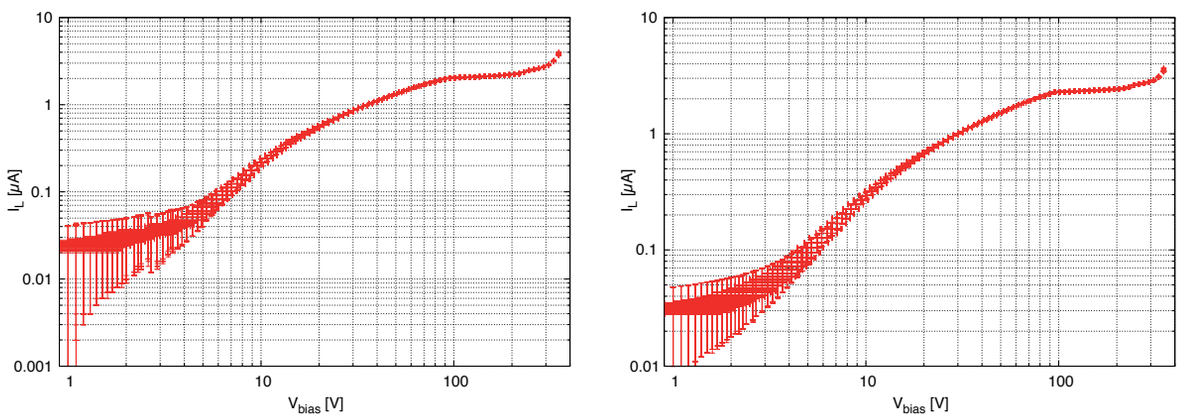


Figure 4.13: Second prototype run - leakage current. The current rises steadily until the full depletion point; after the depletion, the current is between 1 and 2 μA. On both samples, the breakdown occurs around 350 V.

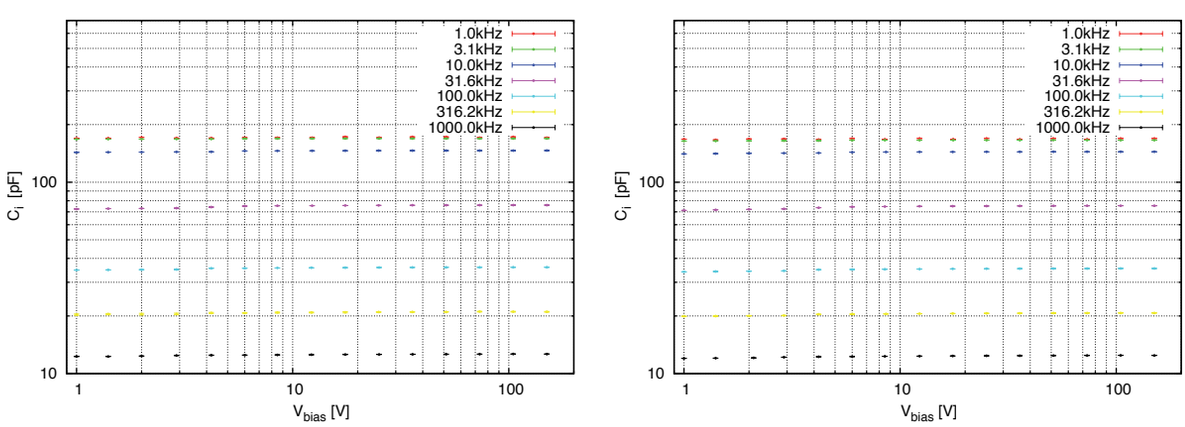


Figure 4.14: Second prototype run - AC coupling to one strip. The values, which show an excellent uniformity between the two samples, are strongly frequency-dependent but are not influenced by the value of the biasing voltage. In the low frequency limit, the capacitance is measured to be around 170 pF, corresponding to 51 pF/cm.

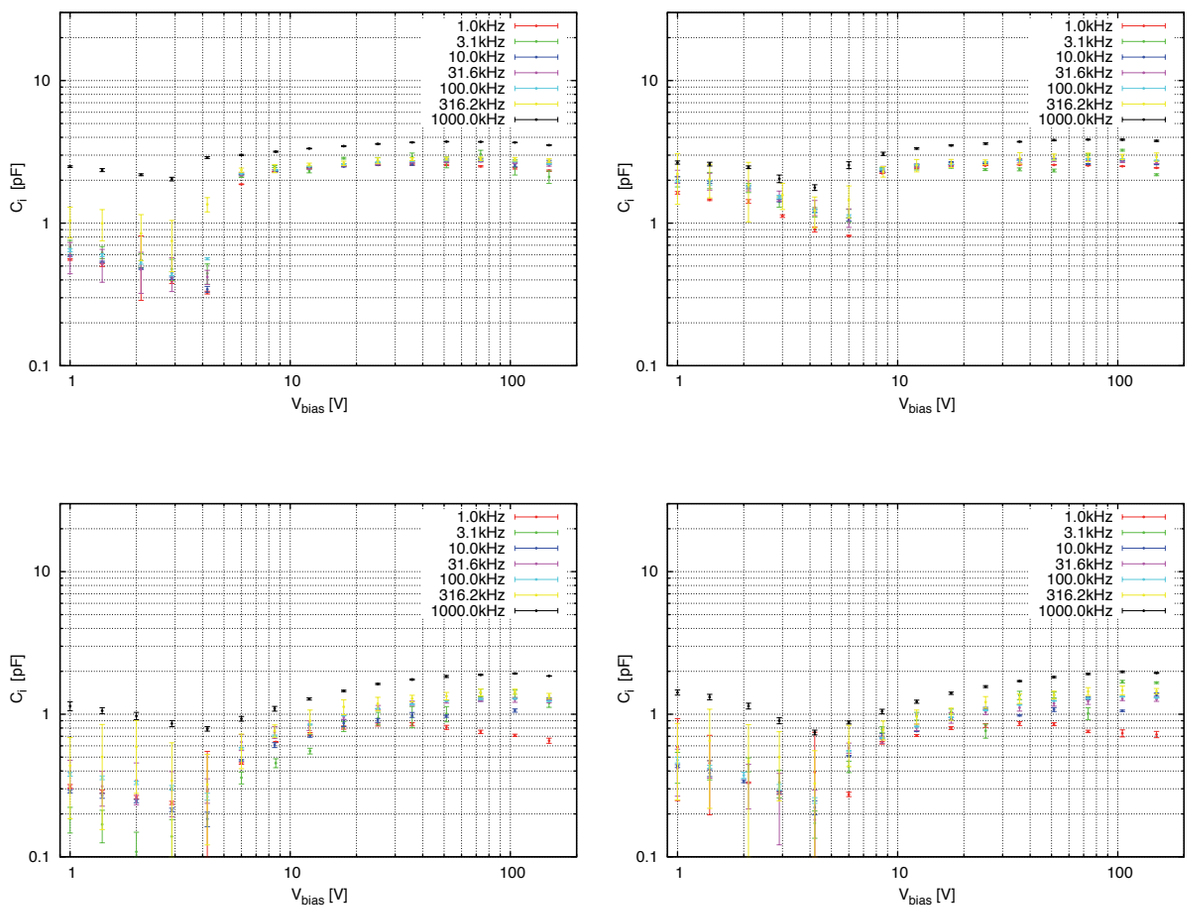


Figure 4.15: Second prototype run - interstrip capacitance. Coupling between first (*top*) and second (*bottom*) neighboring strips, measured between the respective AC pads. At the full depletion voltage, a capacitance between 2 and 3 pF and between 1 and 2 pF for first and second neighbors is observed, respectively.

4.2.2.3 *First production run (polysilicon biasing)*

Based on the results of the characterizations and in particular on the effects on the noise of the radiation damage, summarized at the end of this chapter, the polysilicon resistors biasing technique was chosen for the final production of the sensors for the $\overline{\text{P}}$ANDA MVD. A first run of production-grade sensors was therefore manufactured in 2015. The delivered sensors belonged to three separate production lots; in a test designed to evaluate the uniformity among the lots, selected measures have been conducted on two square sensors per lot (except for one lot from which only two sensors were available; only one was therefore picked for testing).

The measurements, performed at the probe station setup, included a global I-V and single-strip C-V measurement on six p-side strips per sensor out of the 512 available: two towards one edge (n. 19 and 23), two in the middle (n. 255 and 257) and two towards the other edge (n. 495 and 497). The capacitance is measured between the AC pad of one strip to the chuck, with the three needles setup used in the measurements of the samples from the second prototype run.

Wafer	V_{break} [V]	$I_{leakage}$ @100 V [μA]	V_{depl} [V]	C_{depl} @100 kHz [pF]
Lot 341774, wafer 3	350 ± 20	2.48 ± 0.03	108 ± 6	1.41 ± 0.03
Lot 341774, wafer 12	325 ± 20	3.30 ± 0.08	77 ± 7	1.11 ± 0.03
Lot 341775, wafer 22	380 ± 20	1.52 ± 0.02	107 ± 3	1.04 ± 0.09
Lot 341776, wafer 3	318 ± 20	3.79 ± 0.05	94 ± 6	1.04 ± 0.06
Lot 341776, wafer 9	321 ± 20	1.73 ± 0.02	107 ± 5	1.14 ± 0.03

Table 4.2: Values of breakdown voltage, leakage current, depletion voltage and capacitance measured on five sensors from the first production batch [124].

The I-V curves measured on the five sensors under test are reported in figure 4.16. The main parameters measured are reported in table 4.2; at a biasing voltage of 100 V, the measured leakage current ranges from 1.52 to 3.79 μA. The breakdown voltage can be also identified directly from these curves; it must be high enough to leave a sufficient margin to reach the depletion voltage even at the end of the $\overline{\text{P}}$ANDA lifetime when, as demostrated in the last section of this chapter, the accumulated radiation requires the bias voltage to be raised up to 200 V and beyond. In the five sensors studied it occurs between 318 and 350 V, on average 24% earlier than reported by the manufacturer.

The depletion voltage can be estimated from the strip to chuck C-V curves. A typical curve is shown in figure 4.17; the depletion voltages, obtained on each sensor as the average among the six strips measured, ranges between 77 and 108 V. The maximum variation among the six strips on the same sensor is in the order of 10% and there is no clear relation to the position of the strip. The capacitance at the depletion voltage, measured with an LCR frequency of 100 kHz, ranges between 1.04 and 1.41 pF.

Each of the five sensors tested satisfies the acceptance requirements for the production-grade components of the MVD; specifically, all the sensors exhibit a C-V characteristic which allows to identify

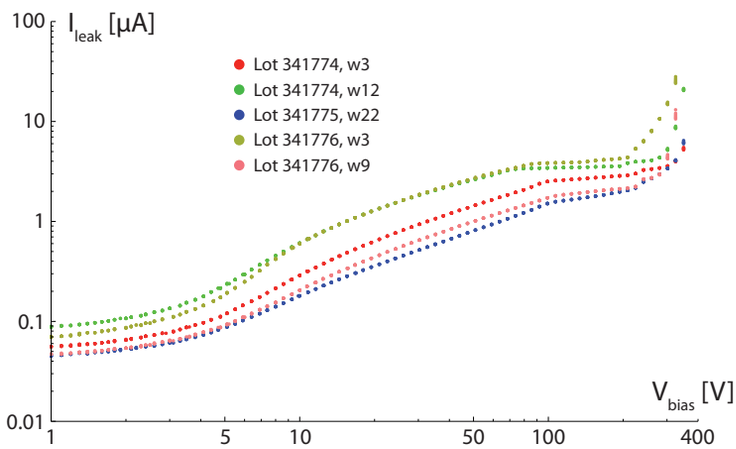


Figure 4.16: I-V curves measured on five sensors from three different lots in the first production batch. The temperature was monitored during the measurement and was (23.5 ± 0.5)°C. Values between 1 and 5 μA are observed at the full depletion voltage.

clearly the full depletion voltage and feature a leakage current at the depletion voltage below 10 μA. The reverse breakdown occurs always at a biasing voltage at least 200 V higher than the full depletion. However, the biasing voltage required to deplete the sensors increases significantly with the accumulated radiation, as demonstrated in the next section. Breakdown voltages around 300 V might therefore become too close to the full depletion when approaching the end of the $\overline{\text{P}}$ANDA lifetime. Additionally, the large differences between the breakdown voltages provided by the manufacturer and those measured in the laboratory are a source of concern. Further studies are required to track down the source of such differences, as well as to characterize more extensively the production sensors and to identify other eventual critical points.

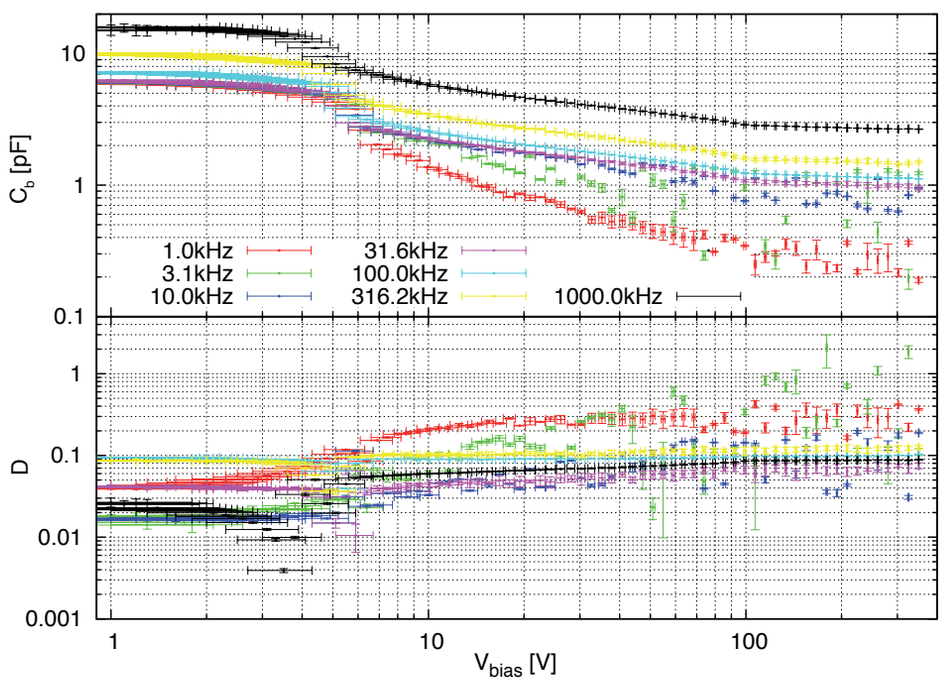


Figure 4.17: Strip to chuck capacitance of one of the production-grade sensors tested with the probe station setup (Lot 341774, wafer 3, strip 19). The curves are acquired at seven different frequencies, of which the first three should be discarded because of the high fluctuations and of the high D value. At frequencies below 1 MHz and above 10 kHz, values of capacitance between 1 and 2 pF are observed.

4.2.3 *Radiation hardness studies*

The investigations of the sensor radiation hardness were performed by irradiating several "Baby" sensors from both prototype runs with 14 MeV protons, using the setup at the Bonn cyclotron described in section 4.1.2. The aim of the tests is to investigate whether it is still possible to operate the sensors after the accumulated fluence of ten years of experiment operation. In particular, the ability to fully deplete the sensor and to keep the leakage current at acceptable levels must be retained for the entire $\overline{\text{P}}$ANDA lifetime.

The alteration of the sensor behavior after the exposure to the radiation was evaluated by comparing the C-V and I-V curves acquired after the irradiations with the reference ones measured before it. The standard annealing procedure of 80 minutes at 60°C recommended in [125] was applied on each sensor after the irradiation and before the new measurement.

The plots in figure 4.18 represent the measured values of the full depletion voltage and of the global leakage current, for different fluences in the range between 2 and $7 \cdot 10^{13}$ $n_{1\text{MeV eq}}\,\text{cm}^{-2}$, for sensors from the first prototype batch (i.e., those with punch-through biasing). The value of the full depletion voltage before the irradiation is added for comparison.

The full depletion voltage, calculated from the C-V curves, increases significantly at the higher levels of radiation exposure. Additionally, the correct determination of the full depletion voltage is rendered difficult by the significant deterioration of the shape of the C-V curve; this is reflected by the large uncertainties attributed to the voltage values. The uncertainties on the fluence are similarly large because of the difficulty in measuring the beam profile and of its unevenness, as described in section 4.1.2.

The measured values of the leakage current increase with the applied equivalent fluence. The studies in [125] predict a linear rise with a slope of $\alpha = 4 \cdot 10^{-17}\ \text{A} \cdot \text{cm}^{-1}$; this parametrization is represented in the plot and the experimental measurements show a good agreement with the model over the entire fluence range explored.

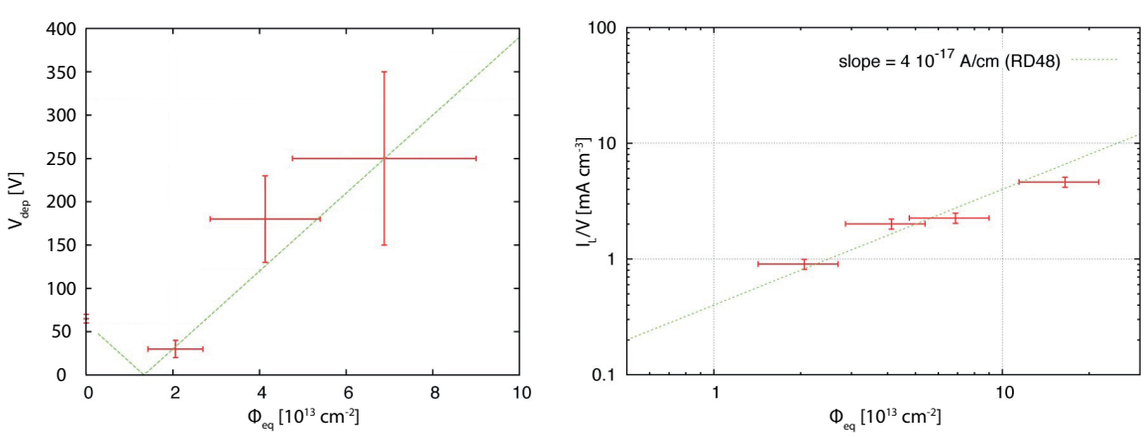


Figure 4.18: Irradiation studies on sensors from the first prototype run (punch-through biasing): behavior of the full depletion voltage (*left*) and of the leakage current (*right*) for different equivalent fluences.

A similar study was performed on five "Baby" sensors from the second prototype batch, i.e., sensors with polysilicon resistor biasing. The behavior of the full depletion voltage and of the global leakage

currents for five fluences between $5 \cdot 10^{12}$ and 10^{14} $n_{1MeV\,eq}\,cm^{-2}$ is shown in figure 4.19. As in the previous study, the measurements were performed after the standard annealing procedure of 80 minutes at 60°C.

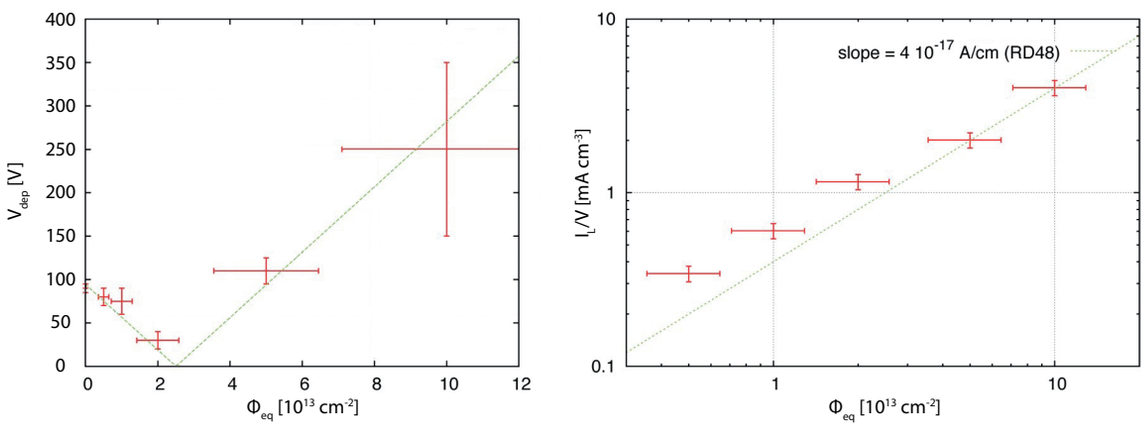


Figure 4.19: Irradiation studies on sensors from the second prototype run (polysilicon biasing): behavior of the full depletion voltage (*left*) and of the leakage current (*right*) for different equivalent fluences.

The behavior of both the full depletion voltage and of the leakage current does not differ significantly from the one observed on the punch-through biased sensors: for comparable equivalent fluences, the sensors from the two different prototype runs exhibit very similar values. Therefore, the choice of the biasing technique does not have a direct influence on the radiation hardness achievable on the sensors.

There are however other factors to take into account when choosing a sensor technology. In particular, the use of punch-through biasing, while simplifying the design and the fabrication of the sensor, introduces an additional term in the current noise, with a magnitude equal to the leakage current noise and a voltage spectral density proportional to the leakage current [100]. While this effect is negligible on non-irradiated sensors, the additional noise can become unbearable for the higher levels of leakage current observed after the exposure to radiation and lead to unacceptably low values of the signal to noise ratio [126]. Given the comparable results of the electrical characterization and of the intrinsic sensor radiation hardness, the use of polysilicon biasing has been therefore favored for the production-grade strip sensors for the $\overline{\text{P}}$ANDA MVD.

5

MECHANICAL AND ELECTRICAL INTEGRATION OF A BARREL STAVE

In addition to the sensors and the readout electronics, described in the previous chapters, the barrel staves require several additional elements. The first of them is the carbon fiber mechanical support, schematically described in chapter 3. This chapter is devoted to other detector components and ancillary systems, and specifically to the Flexible Printed Circuit (FPC), the stave cooling system and the detector powering and cabling apparatus. These elements collectively provide the electrical and mechanical integration of the strip detectors into the experiment and are a prerequisite for the correct operation of the MVD.

5.1 Flexible Printed Circuit

The Flexible Printed Circuit (FPC) is a crucial component of the barrel staves. Its function is to provide the electrical connection between the sensor strips and the front-end channels, as well as to connect the various front-end chips to the MDC and the MDC to the outside world. The distribution of the power supply to the front-end chips and to the sensors must be also managed through the FPC.

In this section, the specifications and requirements of the FPC are presented, together with the description and the study of the various prototypes realized.

5.1.1 *FPC specifications*

5.1.1.1 *Geometrical and routing constraints*

As a bridge component connecting all the different parts of the barrel staves, the layout of the FPC is closely derived from the layout of the carbon fiber stave, of the sensors and of the readout electronics.

As described in the previous sections, the concept foresees one flexible board per barrel stave, folded around its long edge. As shown in figure 5.1, the fanouts of the p-side are implemented in the small part of the FPC in front of the readout chips, overlapping with the sensors. On the n-side, the fanout of each sensor is implemented on a flap, designed to be inserted in the matching stave sensor cutout. Since the rows of the n-side bondpads on the sensors are perpendicular to the long edge of the stave, the lines on the fanout are used to route those signals to a location next to the chips.

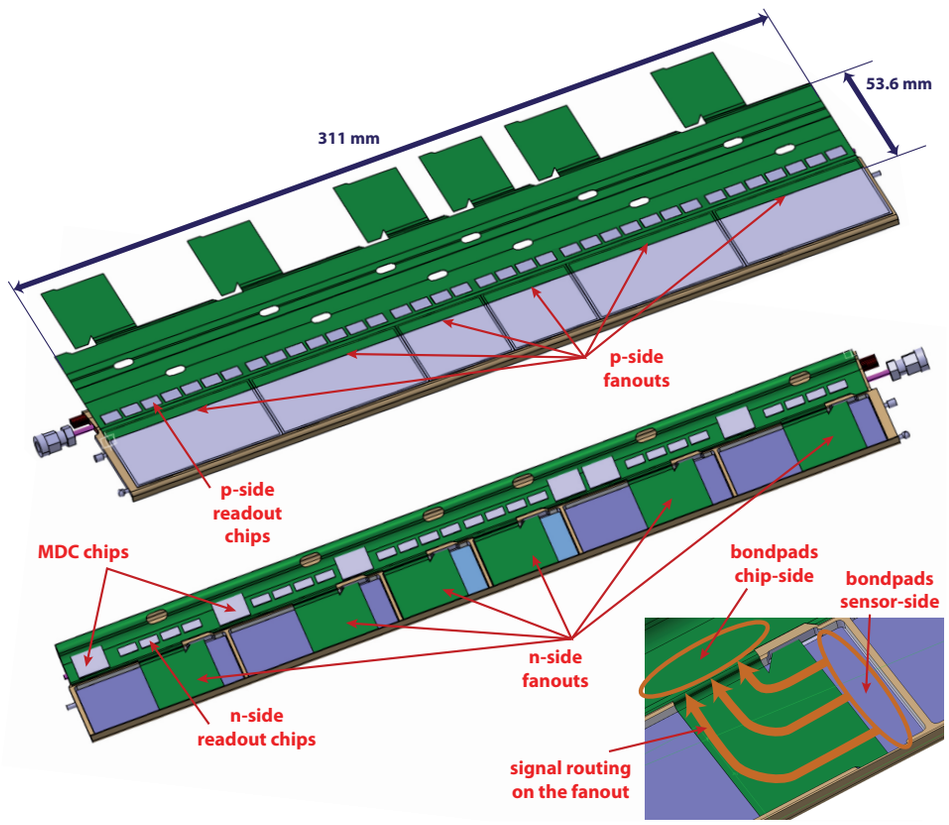


Figure 5.1: Concept of the FPC for the staves of the outer strip barrel (BL4). *Top:* unfolded FPC, placed on the p-side of the stave and equipped with the readout electronics. *Center:* the FPC is folded around the long edge of the stave and equipped with the n-side readout electronics. *Bottom:* detail of one n-side fanout structure, placed in the recess of the stave sensor cutout.

The central area of the FPC, approximately 18 mm wide, is to be folded around the edge of the stave. In order to do this, it must be kept free from components. Similarly, small keepout areas are foreseen in the bend regions of the fanout structures. The cable duct in the stave, through which the power supply cables are routed, can be accessed through several oval holes (two per sensor, one on each side of the stave); matching holes must therefore be implemented in the FPC.

The constraints on the outer dimensions of the FPC, as well as on the location of the keepout regions and of the cable duct holes, are presented in figure 5.2.

In addition to the dimensional constraints inherited from the carbon fiber stave layout, the electrical requirements of the FPC play an important role on the design. These include the placement of a large number of components, the routing of the signal lines between the chips and the power and ground distribution. The most complex layout, i.e., a standard stave of the outer barrel (BL4), will be considered in the following. The remaining five designs feature fewer chips and fewer connecting lines and are therefore less demanding. A possible distribution of the chips and of the data lines is shown in figure 5.3.

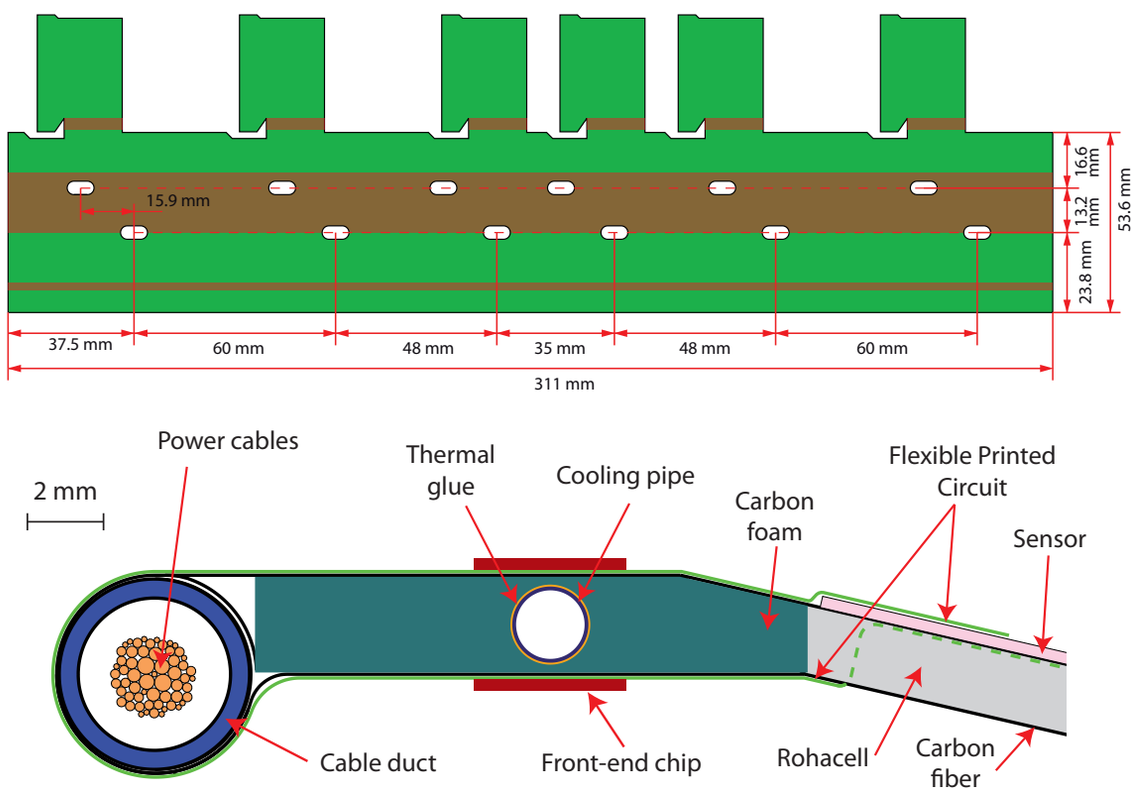


Figure 5.2: Outline of the FPC and constraints given by the dimensions of the carbon fiber stave. *Top:* dimensions of a BL4-type stave FPC; the areas highlighted in darker color represent the component keepout regions reserved for the FPC bends. *Bottom:* transverse view of a generic stave with its different components highlighted. The FPC, folded around the stave, is depicted in light green.

With each rectangular sensor requiring eleven PASTA chips (seven on the p-side and four on the n-side) and each square sensor requiring eight PASTA chips (four on each side), a total of 36 and 24 chips must be placed on the p-side and n-side, respectively. Additionally, each sensor requires one MDC chip, placed on the n-side.

For what concerns the signal lines, each PASTA chip is connected through an e-link (physically implemented with three differential pairs) to the corresponding MDC. Another e-link connects the MDC to the GBT boards on the outside, leading to a total of 18 differential pairs on the data cable that leaves the stave.

In addition to the data lines, the power supply of the chips and the high voltage for the sensor biasing are also provided through the FPC. The powering scheme, which is described in detail in section 5.3, requires four separate power domains per sensor, i.e., a total of 24 domains on a six-sensor stave. The required cables are lead along the cable duct and to the FPC through the holes on the stave; two holes per sensor are built in the stave, each one serving the two power domains of the n- and p-side, respectively.

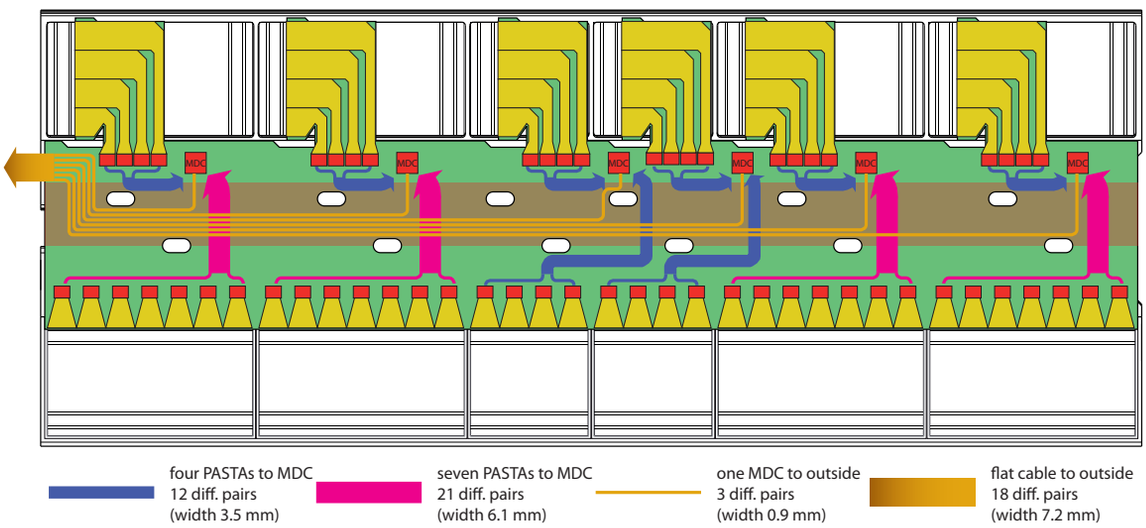


Figure 5.3: Concept of the equipped FPC for a BL4-type stave; the p-side is at the bottom. The signal input/output connections are provided through an aluminum flat cable with 18 differential pairs, placed at the upstream edge of the stave (on the left in the drawing). These are connected exclusively to the MDC chips, on the n-side of the stave, which are in turn connected to all the corresponding PASTA chips. The data connections between the PASTA chips and the MDC and from the MDC to the outside are represented in the drawing with colored arrows; the thickness of the lines represents the foreseen width of the bundle of differential pairs. The chips are drawn in red; the trapezoidal-shaped yellow structures next to them on the p-side and the more complex L-shaped ones on the n-side represent the chip fanouts.

Despite the power supply of the chips being implemented as low voltage lines, the presence of the sensor biasing causes a high voltage potential between the lines on the p-side and those on the n-side. Particular care must be therefore taken during the design phase to ensure that the n-side lines never get too close to the p-side lines. The recommended minimum spacing for external, coated conductors and voltages up to 300 V is 0.4 mm [127].

5.1.1.2 *FPC material*

The materials used for the FPC must satisfy several requirements. The first and most important is the low material budget: this is achieved by using low density, low Z materials, as well as reducing as much as possible the thickness of the layers. The material must be radiation tolerant up to the target values of $\overline{\text{P}}$ANDA and should allow the design and fabrication of dense electrical structures with very small features. Additionally, it should be possible to handle the FPC with relative ease, in order to simplify the assembly procedure: good mechanical stability is therefore a must.

The material of choice for this application is the polyimide film, commercially sold as Kapton, with chemical composition $(C_{22}H_{10}N_2O_5)_n$. It is sold in a wide variety of products, both as standalone substrate, as coverlay and as copper-clad laminates; different types of films were used in the fabrication of the prototypes described in the next sections.

Property	NEMA G10 FR4 60% SiO_2 + 40% epoxy	Polyimide film (DuPont AP9111)
Dielectric loss tangent	0.017	0.003
Dielectric constant	4.2 – 4.8	3.4
Thermal conductivity, in-plane [W/m·K]	0.27	0.12
Density [g/cm^3]	1.85	1.42
Breakdown voltage [V/μm]	20	230 – 280
Coefficient of Thermal Expansion (CTE), in-plane [ppm/K]	14	25
Tensile strength [MPa]	275	>345
Radiation length [g·cm^{-2}]	33.0	40.58
Young's modulus [GPa]	21	4.8

Table 5.1: FPC substrate properties [128]. Typical values for FR4, a common substrate material for printed circuit boards, are shown for comparison.

The most important properties of polyimide film relevant for its use as FPC substrate are reported in table 5.1. Its large radiation length, combined with the low achievable thickness, makes it a very suitable material in applications where low material budget is required.

The largest drawback of the polyimide film is its high thermal resistance. At 0.12 W/m·K, the thermal conductivity of the film is much lower than that of the other materials used in the stave construction. Since the FPC is placed directly between the readout chips and the cooling system embedded in the stave, its low thermal conductivity can be detrimental to the cooling performances. To mitigate this effect it is mandatory to keep the thickness of the film as low as possible, as well as to employ dedicated techniques, such as thermal vias across the substrate thickness, to increase the thermal conductivity. An evaluation of the effects introduced by the FPC on the cooling system can be found in section 5.2.

For what concerns the conductor material, the choice is usually limited to copper and aluminum. Copper is the default solution in most research and commercial applications; however, thanks to its lower material budget, aluminum represents an attractive alternative.

With a radiation length of $X_{0_{\mathrm{Al}}} = 24.01\ \mathrm{g\cdot cm^{-2}}$ and a density of $\rho_{\mathrm{Al}} = 2.70\ \mathrm{g\cdot cm^{-3}}$ (compared to $X_{0_{\mathrm{Cu}}} = 12.86\ \mathrm{g\cdot cm^{-2}}$ and $\rho_{\mathrm{Cu}} = 8.96\ \mathrm{g\cdot cm^{-3}}$ for copper), the use of aluminum can decrease the material budget by a factor of approximately 6. The possibility of manufacturing aluminum-based flexible printed circuits has been explored for the multilayer busses in the pixel part of the $\overline{\mathrm{P}}$ANDA MVD, as well as for the data transmission cables [66, 129, 130] and in other high energy physics experiments [131, 132, 133].

However, there are several other factors to be taken into account. The conductivity of copper is almost twice as large as that of aluminum ($\sigma_{\mathrm{Cu}} = 5.96 \cdot 10^5\ \mathrm{S/cm}$ compared to $\sigma_{\mathrm{Al}} = 3.50 \cdot 10^5\ \mathrm{S/cm}$). Therefore, the use of aluminum requires larger traces for power transmission and partially counterbalances the gain in the material budget. The manufacturing of copper-based flexible circuits is highly

developed and is available from a large number of commercial vendors; by contrast, very few companies offer the possibility to have aluminum-based circuits, using costly and time-consuming processes. Additionally, the manufacturing of very small structures in aluminum is more difficult and less reliable. For this reasons, it was chosen to focus the efforts on the design and production of copper-based flexible circuits.

5.1.2 *FPC prototype v1*

The first series of prototypes of FPCs was designed in order to explore various technological options, as well as to test the manufacturing reliability of small-size structures and the performance of flex-based sensor readout. A large variety of designs were prepared, grouped in three main categories:

- pitch adapters, designed to replace the thin-film ceramic models used in the early sensor test L-boards [120];
- one-chip carrier boards with integrated pitch adapter;
- flat cables, to connect the chip carrier board to the test system.

The designs in each of the three categories were produced on an independent sheet, therefore allowing to optimize the technology parameters and in particular the layer stackup. Three different stackups were available:

- PA-type, for the pitch adapters;
- PA-C-type, for the pitch adapters (with coverlay);
- PCB-type, for the cables and the chip carrier boards.

The "PA" and "PA-C" cross sections feature the same substrate, an adhesiveless copper-polyimide-copper laminate (Dupont Pyralux AP7164E [128]) and differ only for the bottom insulator layer: in

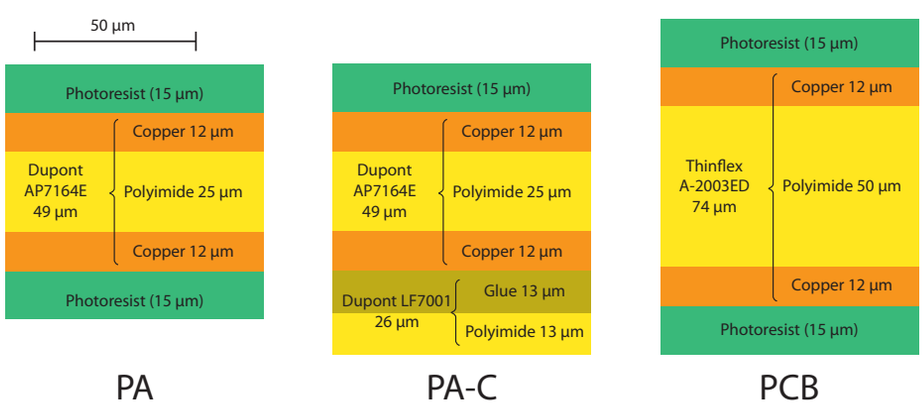


Figure 5.4: Available cross sections for FPC v1 prototypes.

the first case it consists of a NPR-80-ID100 photoresist, while in the second case it is made of an acrylic adhesive-polyimide coverlay laminate (Dupont Pyralux LF7001 [134]). The top layer insulation is realized in both cases with the photoresist. The "PCB" cross section uses a thicker adhesiveless copper-polyimide-copper laminate (Thinflex A-2003ED [135]) and features photoresist insulation on both sides. In both of the copper laminates employed, the copper layers are 12 μm thick and are realized via electrodeposition (ED). The properties of the two substrates and of the insulation materials are summarized in tables 5.2 and 5.3, respectively. The detailed composition of the three stackups is described in figure 5.4.

Property		Dupont AP7164E	Thinflex A-2003ED
Thickness	ED-copper	12 μm	12 μm
	polyimide	25 μm ± 10%	50 μm ± 10%
	ED-copper	12 μm	12 μm
Radiation length [X/X0]		0.176%	0.185%
Dimensional stability [%]		-0.05 to -0.08	-0.1 to 0.1
Dielectric loss tangent		0.003	0.002
Dielectric constant		3.4	3.3
Breakdown voltage [kV/mil]		$6-7$	6.8
Volume resistivity [$\Omega-$cm]		10^{16}	10^{12}
Surface resistivity [Ω]		$> 10^{16}$	10^{11}
CTE, in-plane [ppm/K]		25	19.3
Peel strength [N/mm]		1.6	> 1.2
Young's modulus [GPa]		4.8	4.2

Table 5.2: Comparison of the properties of the two substrate materials used for the FPC v1 prototypes [128, 135]. Electrodeposited (ED) copper is used in both materials.
Volume resistivity (in ohm-centimeters) is defined as the electrical resistance through a cube of insulating material of one-centimeter cube. Surface resistivity is defined as the electrical resistance of the surface of an insulator material, measured on a square [136]. Peel strength is defined as the load force needed to disbond the laminate, divided by its width, in accordance with [137].

5.1.2.1 *Pitch adapters*

The requirement of the pitch adapters is dictated by the large difference between the bond pitch on the sensor and that on the readout chips. While wire bonding can be in principle performed successfully even between misaligned pads, by means of placing the bond with a certain angle, in practice this poses a limit on the density of bonds and on their reliability. The earlier L-boards in the test setup used pitch adapters realized with thin-film technology on a ceramic substrate [120]. Because of the cost of this technology, the use of flexible pitch adapters was envisaged as a replacement. Twelve different designs

Property	Coverlay Dupont LF7001	Photoresist NPR-80-ID100
Thickness	13 μm (adhesive) 13 μm (polyimide)	15 μm
Dimensional stability [%]	+0.07	N/A
Dielectric loss tangent	0.02	0.026 – 0.021 (1 MHz – 1 GHz)
Dielectric constant	3.6	3.98 – 3.53 (1 MHz – 1 GHz)
Peel strength [N/mm]	1.8	N/A
Volume resistivity [Ω – cm]	10^{15}	$1.2 \cdot 10^{16}$
Surface resistivity [Ω]	10^{14}	$3.5 \cdot 10^{13}$
Density [g/cm^3]	1.42	1.37

Table 5.3: Comparison of the properties of the photoresist and of the coverlay material used for the FPC v1 prototypes [134, 138].

were implemented, accounting for different sensor size and bond pitch and for different front end chips [139]. The sheet containing the various layouts is shown in figure 5.5; a detail of one of the pitch adapters is visible as well. Several sheets were manufactured using both the PA-type and PA-C-type cross sections.

Since the sensor test setups make extensive use of the APV25 readout chip, most of the pitch adapters were designed for it. There is however also a small number of pitch adapters compatible with the n-XYTER [140] and the FSSR2 [141] chips. The sensor pitch is either 65 μm or 130 μm, corresponding to the pitch of the $\overline{\text{P}}$ANDA sensors with every strip bonded or with one intermediate floating strip, respectively. Additionally, two designs have a pitch of 50 μm, to be compatible with the older ITC sensors as well as with the S3-type CiS sensor, described in section 4.2.1.

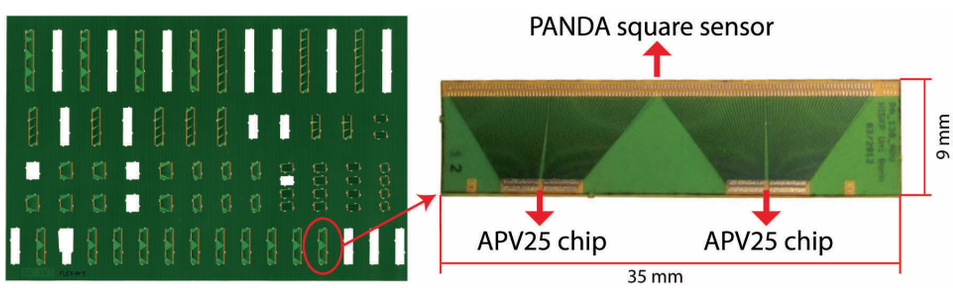
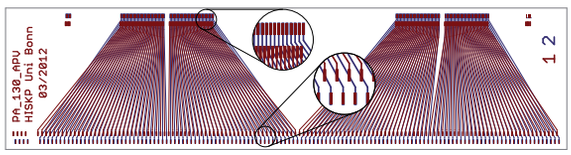
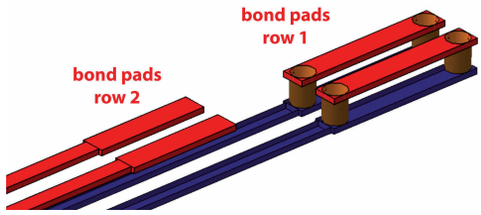


Figure 5.5: *Left:* photograph of a sheet containing the various designs of flex-pitch adapters. *Right:* detail of one of the pitch adapters; the type in the picture, which has been extensively used for tests on the L-boards based sensor characterization setup, connects two APV chips to one sensor with a 130 μm bond pitch, for a total of 256 channels.



(a) Fanout structure implemented on the flexible pitch adapters. The red and blue traces represent the top and bottom layers, respectively.



(b) Schematic of the bond pads, showing the connection between the layers by means of 50 μm laser microvias.

Figure 5.6: Details of the layout of the flexible pitch adapters.

Because of the 44 μm pitch on the APV frontend pads, the fanout structure implemented on the pitch adapters is very dense. The pads on the frontend side are placed in two rows, mimicking the structure present on the APV, with each row having a pitch of 88 μm between the pads. A detail of the fanout structure is shown in figure 5.6a. In the row closer to the chip (corresponding to the even pads of the APV), the bond pads on the top layer are connected with mirrored pads on the bottom layer; the routing to the sensor is then performed entirely on the bottom layer. The signals from the odd pads, i.e., those farther away from the chip, are routed directly on the top layer. The dense structure does not allow the use of standard vias to connect the two layers; laser-drilled microvias with a diameter of 50 μm placed at the edges of the bond pads are used instead. The structure of the bondpads with the microvias is shown in figure 5.6b. On the sensor-side of the pitch adapter there are again two parallel rows of pads, simmetric to the ones on the chip-side; the bond pads are also identical. The pitch adapter does not implement any power pad for the APV, thus simplyfing significantly the design. These are implemented on the rigid L-boards onto which the pitch adapter is glued. There is however a number of test pads, which can be used to calibrate the bonding procedure.

5.1.2.2 *One-chip carrier boards*

The second category of designs produced in the FPC v1 series consists of the one-chip carrier boards. In contrast to the flex pitch adapters, which complement the L-boards setup, the chip carrier boards represent an alternative and independent system to read out a strip sensor.

Four different designs were implemented, in order to fit different readout chips and different data connectors. All designs host one 128-channel readout chip and the fanout structure to connect it to a sensor. On the APV-based boards, an S3 sensor with 384 strips and a pitch of 50 μm was chosen; in order to cover the whole sensor with just one chip, only one third of the strips are connected to the chip, thus leaving two floating strips for each connected one. The bonding pitch is therefore 150 μm. On the n-XYTER-based boards, the pads allow to connect a sensor with 128 strips and a pitch of 130 μm. The input/output lines of the chip are routed to a fine-pitch connector; the power supply lines for the chip and the high voltage bias lines for the sensor are implemented as well and connected to soldering pads at the edge of the flex circuit. The sheet, containing twelve carried boards in total, was manufactured using the PCB-type cross section.

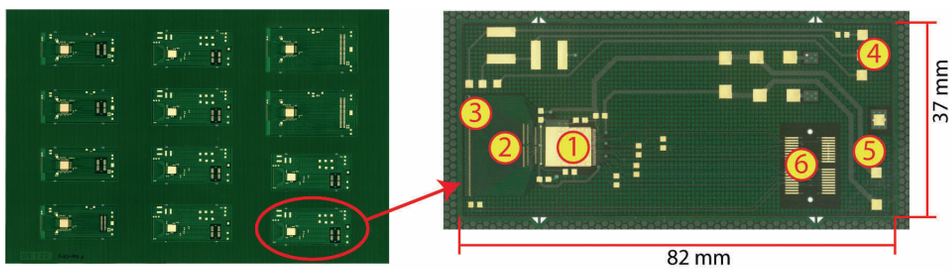
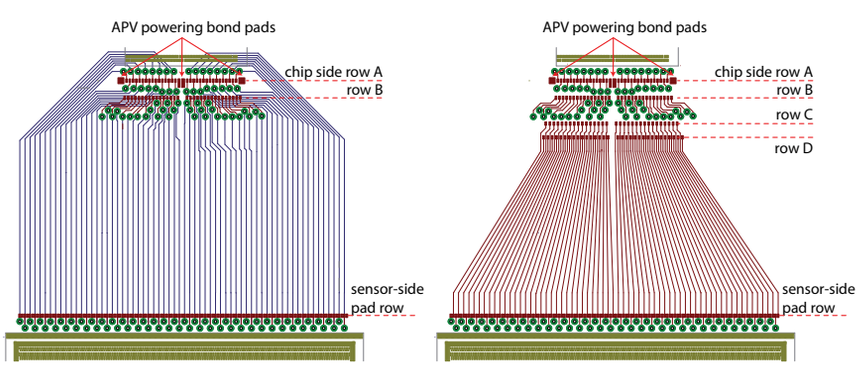
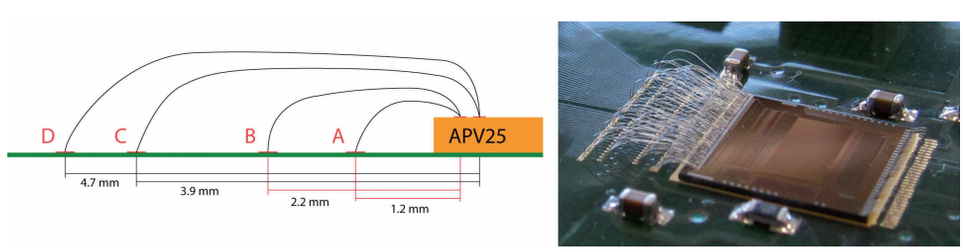


Figure 5.7: *Left:* photograph of a sheet containing the various designs of flex chip carrier boards. *Right:* photograph of a chip carrier board. The type in the picture hosts one APV chip and connects it to one sensor with a 150 μm bond pitch. (1) pad for one APV readout chip; (2) fanout structure; (3) bonding pads for the sensor; (4) sensor biasing connectors; (5) APV power supply connectors; (6) fine pitch data cable connector.

An example of a chip carrier board prototype is visible in figure 5.7 on the right; this type hosts one APV chip and one Samtec LSH-020-01 connector. The fanout structure implemented is radically different from the one in the pitch adapters and, from a technological point of view, is much simpler, since standard vias with a diameter of 200 μm were employed. On the other hand, the greater space required by the transition between the layers required a more intricate layout, considering also the



(a) Fanout structure implemented in the flexible chip carrier board. *Left:* bottom layer; *right:* top layer.



(b) Side view of the bonding scheme between the APV chip and the fanout structure, showing the four rows of bonds placed one on top of the other, and photograph of an assembled prototype. The figures refer to the distance between the two rows of pads, i.e., to the length of the shortest, straight bonds.

Figure 5.8: Fanout structure in the flex chip carrier board.

necessity to integrate the APV power pads, as visible in figure 5.8a. On the sensor side, a single row of 128 pads with a pitch of 150 μm was implemented. On the chip side, the 128 pads are distributed over four rows of 32 pads each, designated with the letters A, B, C, D in the drawing, with a pitch of roughly 200 μm. The even pads from the sensor side are routed directly to rows C and D, with the lines laying entirely on the top layer. The odd pads of the sensor side row are connected through standard vias to the bottom layers and from there routed to rows A and B, requiring a second via nearby the chip-side pads. The intricate layout imposed a reshuffling of the sensor-to-chip channel connection, i.e., the numbering of the channels in the sensor does not correspond to the numbering on the chip, but a lookup table is needed instead to reconstruct the proper strip position.

The layout of the fanout structure imposes a complex arrangement of wire bonds on its chip-side, as visible in figure 5.8b. Four rows of bonds have to be performed, one above the other, connecting the front pad row of the APV to rows A and B on the board and the back row of the APV to rows C and D, with the longest bonds exceeding 6 mm in length.

5.1.2.3 *Flat cables*

The last category comprises the flat cables, required to connect the chip carrier boards to the existing readout architecture. The connector on the supply boards is a through-hole device which is not suitable for mounting on a flexible board; in order to avoid a redesign of the supply boards, an intermediate transition board was designed instead; the layout is visible in appendix B.

Three flat cables with different length (5, 10 and 15 cm) were produced. Each cable features twenty differential pairs, referenced to a common ground; the pairs run between two identical LTH-020-01 Samtec connectors. The connectors were produced on sheets with the "PCB" cross section. An example of a prototype of the shortest kind of cables is visible in figure 5.9.

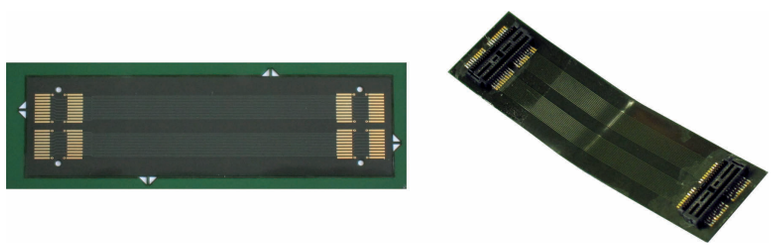


Figure 5.9: Photograph of two flex cables; the connectors have already been soldered on the prototype on the right. The nominal length of 50 mm refers to the distance between the center of the two connectors; the actual board is about 11 mm longer and 17 mm wide.

5.1.2.4 *Assembly of a test module*

In order to test the functionality and the assembly procedure of the chip carrier board prototypes, a module with two such boards has been designed and produced. The module, which is shown in figure 5.10, consists of one double-sided S3-type strip sensor, read out on both sides with one-chip carrier boards. The S3 sensors, described in section 4.2.1, feature 384 strips per side with a pitch of 50 μm and have a size of 2.095×2.095 cm^2.

The module is supported by a fiberglass square support, 2 mm thick and 12 cm wide, onto which a cutout for the sensor was manufactured. The sensor rests on a thin edge inside the cutout, at an equal distance from the two sides of the fiberglass plate (see detail on the left of figure 5.10). In this way, the bond pads on both sides of the sensor are easily accessible and are situated approximately 1 mm below the level of the corresponding chip carrier board, which is glued on the surface of the fiberglass plate. The two boards are glued on the opposite side of the plate, perpendicular to each other. The assembly features also the two transition boards required to connect the module to the acquisition system; these are placed directly behind the back end of the flexible boards and connected to them through one 50 mm flat cable like the one shown in figure 5.9, plus some wires for the power supply.

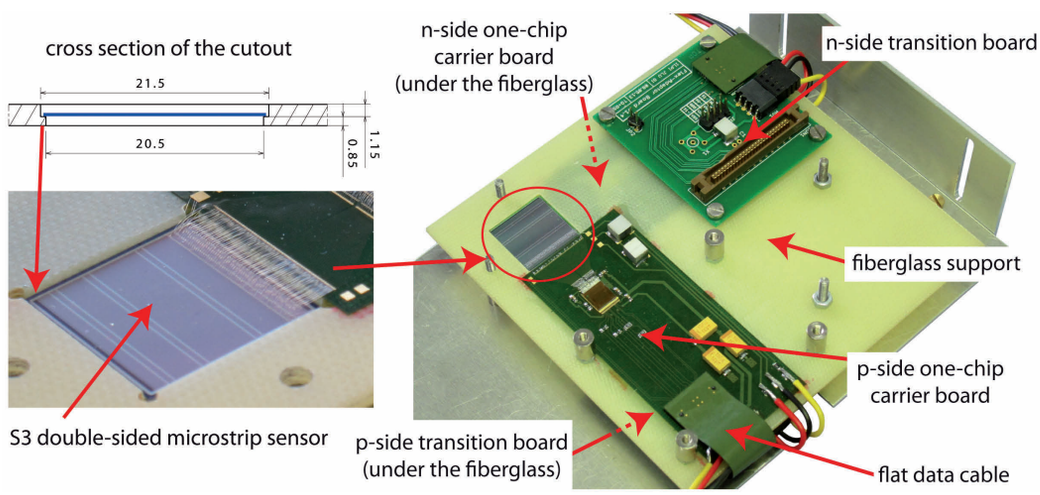


Figure 5.10: One-chip carrier board module. *Right:* photograph of the assembled module. The n-side flex board and the p-side transition boards are located under the fiberglass support and are therefore not visible (though the flexible board can be partially seen through the fiberglass). *Left:* cross section of the sensor cutout through the fiberglass support (with the sensor pictured in blue), and photograph of the sensor in its final position. All figures are in mm.

5.1.3 *FPC prototype v2*

The successful manufacturing and testing of the first batch of flexible printed circuits led to the development of a second version with a new design. The design, representing a step towards the final layout which will be employed in the $\overline{\text{P}}$ANDA MVD, includes a chip carrier board, a cable and new pitch adapters; the detailed specifications of these structures are described in the following paragraphs. Since the design had to be manufactured on a single flexible sheet, there was not the possibility to employ different layer stackups and design rules for the different structures. It was therefore important to compare the various technology options already explored in order to choose the ones to be used, also bearing in mind the implications on their final use in the MVD.

5.1.3.1 *FPC cross section*

The choice of the FPC cross section among the three options explored in the first batch (namely PA, PA-C and PCB) is the most important parameter to be optimized. It has an impact on several factors including the bending radius, the design of differential lines with controlled impedance and the material budget.

- **Bending radius:** the total thickness and the choice of the layer stackup has an influence on the minimum achievable bending radius of the flexible printed circuits.

  An estimation of the minimum bending radius for a double-sided, flexible section with adhesiveless substrate and coverlay can be obtained with the guidelines stated in [142]. For a double-sided circuit with a coverlay, as represented in figure 5.11, the minimum bending radius is given by

$$R = \left(\frac{d}{2} + C\right) \cdot \left(\frac{100 - E_B}{E_B}\right) - D, \tag{5.1}$$

  where d is the dielectric thickness, C the copper thickness, D the coverlay thickness and E_B the allowed copper deformation in percent. The recommended values for E_B are 11% for a one-time crease (value for electrodeposited copper, which increases up to 16% in case of rolled annealed copper), 10% for flex-to-install designs [143] and 0.3% for dynamic applications [142].

Figure 5.11: Minimum bending ratio for a double-sided flexible circuit with coverlay: definition of the layers.

  Another possible value for the bending radius is given by DuPont, the manufacturer of one of the copper-polyimide-copper substrates, which recommends a minimum radius-to-thickness ratio of 6 for the entire stackup, regardless of the layer composition [144]. In table 5.4 the minimum bending radii obtained with the three different layer stackups and with different criteria are shown.

- **Differential impedance:** a careful control of the impedance of the single ended and differential lines is of the upmost importance when designing data transmission circuits. The basic structure is the microstrip, i.e., a rectangular trace placed at the interface between two dielectrics and

Layer stackup	D_{top}	D_{bot}	C	d	T	Criterion	R	R/T
PA	15 μm	15 μm	12 μm	25 μm	79 μm	IPC, one-time:	183 μm	2.32
						IPC, flex-to-install:	206 μm	2.60
						DuPont:	474 μm	6
						IPC, dynamic:	8127 μm	103
PA-C	15 μm	26 μm	12 μm	25 μm	90 μm	IPC, one-time:	183 μm	2.04
						IPC, flex-to-install:	206 μm	2.28
						DuPont:	540 μm	6
						IPC, dynamic:	8127 μm	90
PCB	15 μm	15 μm	12 μm	50 μm	104 μm	ICP, one-time:	284 μm	2.73
						IPC, flex-to-install:	318 μm	3.06
						DuPont:	624 μm	6
						IPC, dynamic:	12281 μm	118

Table 5.4: FPC bending radius. In case of different values for the thickness of the upper and lower coverlays D_{top} and D_{bot}, the smaller of the two was chosen as D for the calculation of the radius. The total thickness T is the sum of all the layers, i.e., $T = D_{top} + D_{bot} + d + 2C$.

referred to a solid conductor plane. Assuming air as the dielectric above the microstrip ($\varepsilon_r = 1$), the characteristic impedance Z_0 of a microstrip, measured in Ω, is given by

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \tag{5.2}$$

where ε_r and h are the dielectric constant and the thickness of the insulator between the trace and the reference plane and w and t are the width and the thickness of the strip, respectively [127].

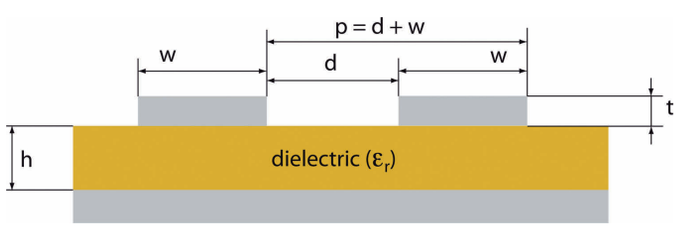


Figure 5.12: Cross section of an edge-coupled microstrip.

For the routing of differential pairs, edge-coupled microstrips are commonly used; these consist of two parallel traces spaced by d and referenced to the same conductor plane, as shown in

figure 5.12. In this case the coupling between the two lines must be taken into account and the differential impedance Z_{diff} can be calculated with the following [145]:

$$Z_{\text{diff}} = 2\,Z_0 \cdot \left(1 - 0.48 e^{-0.96\frac{d}{b}}\right). \tag{5.3}$$

On the three layer stackups available, the thickness of the traces, as well as the dielectric constant and the thickness of the insulator, are fixed. Thus, the strip width and the spacing between coupled lines are the only free parameters which can be tuned to to control the impedance of the traces. In figure 5.13 the differential impedance obtained for different combinations of track width and spacing is shown. An increase in the trace width causes a decrease in the differential impedance; conversely, an increase in the trace spacing causes an increase in the impedance, although the effect is strongly visible only when the traces are close to each other and tends to disappear when the spacing becomes much larger than the dielectric thickness.

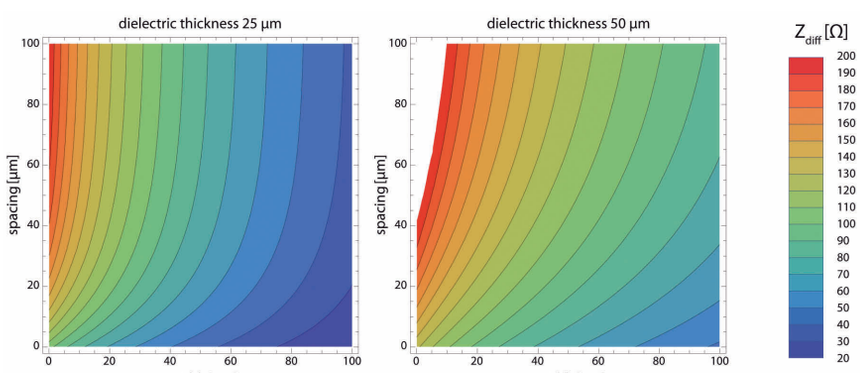


Figure 5.13: Differential impedance as a function of the trace width and spacing, for different dielectric thicknesses, calculated with the equation 5.3, with $\varepsilon_r = 3.4$ and $t = 12$ µm. The figure on the left represents the PA- and PA-C-type cross sections; the one on the right represents the PCB-type cross section.

The results obtained with the formulae represent a first approximation; numerical simulations, as those provided by several PCB design softwares, can provide more accurate results, including also e.g. the effect of the photoresist coating. However, in most of the cases the difference is in the order of a few percent: the values given by the formulae can be therefore used as a starting point and slightly adjusted with the help of the simulations. Following this approach, a target impedance of 100 Ω can be achieved on all available cross sections, using for instance 35 µm traces spaced by 100 µm ($Z_0 = 51.7$ Ω, $Z_{\text{diff}} = 98$ Ω) on the cross sections with a 25 µm dielectric, or 55 µm traces spaced by 60 µm ($Z_0 = 62$ Ω, $Z_{\text{diff}} = 99$ Ω) on the cross section with a 50 µm dielectric.

- **Material budget:** the total material budget of the FPC can be calculated by summing the contribution from the individual layers, using the equation 2.2.

  The largest part of the material budget comes from the two copper layers, which are identical in the three layer stackups. In the worst case, i.e., where a trace is present on both the top and

the bottom layer, the 24 μm of copper contribute with approximately 0.17% X_0. The polyimide layers have a radiation length approximately 20 times greater than that of copper and a slightly larger thickness. Their contribution to the material budget is therefore smaller and is in the order of 0.02% X_0.

The values of the material budget for the three layer stackups are summarized in table 5.5. Since most of the material budget comes from the conductor layers, which are not homogeneously filled with copper over the whole circuit board, the values stated in the table represent the regions where the material is maximum and large deviations from these values are to be expected.

Layer stackup	X/X0 (Cu layers)	X/X0 (PI layers)	Total X/X0
PA	0.167%	0.019%	0.186%
PA-C	0.167%	0.023%	0.190%
PCB	0.167%	0.028%	0.195%

Table 5.5: FPC material budget evaluation for the three layer stackups available in the FPC v1 series.

The previous considerations, together with the experience from the FPC v1 series, allowed to choose the layer stackup to be used in the second prototype production. The impact on the material budget is not a deciding factor, since the layer stackups differ only in the dielectric layers, whose contribution to the material is almost negligible. On the contrary, the use of a thinner cross section is preferred when looking at the achievable bending radii: compared to the PCB-type layer stackup, the thinner solutions allow for a bending radius up to 35% smaller. For what concerns the differential impedance control, all three cross sections allow to design 100 Ω differential lines; the layer stackup with a thicker dielectric would be slightly preferred, since it allows for larger and therefore more robust traces.

On the whole, the greater ease of handle and bending achieved through thinner boards plays the most relevant role and, because of this, it was decided to design the FPC v2 prototypes using the layer stackup with thin dielectric and with the added coverlay for increased robustness (PA-C type).

5.1.3.2 *Chip carrier board layout*

The second version of the chip carrier board is conceived to simulate as closely as possible the final layout required for the $\overline{\text{P}}$ANDA MVD, albeit on a smaller scale and with some limitations. The board can be folded around the long edge of the carbon fiber stave, thus allowing the readout of both sides of one sensor with a single printed circuit.

The layout is presented in figure 5.14. The board is divided in two areas: a sensor-readout part on the right and a service part on the left. The pads for the readout chips and all their fanout structures, as well as the signal lines to the outside and the power supply lines are implemented in the right part. The layout of the sensor-readout part is centered around a rectangular $\overline{\text{P}}$ANDA sensor, with a size of

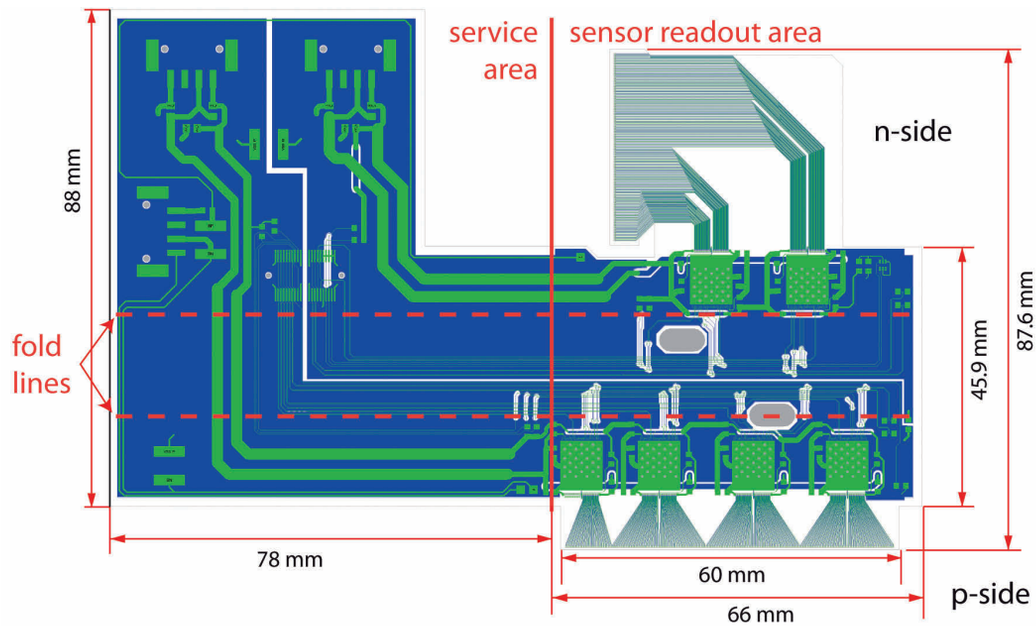


Figure 5.14: Layout of the second version of the chip carrier board.

6×3.5 cm^2 and featuring 896 strips on the p-side and 512 strips on the n-side with a pitch of 65 μm (these sensors are described in section 4.2.1). When using the floating strip technique, a total of 448 channels on the p-side and 256 channels on the n-side have to be read out. If the 64-channels PASTA chip is used, seven and four chips are required on the p-side and on the n-side, respectively. However, at the time the design of the chip carrier board was finalized, PASTA was still in a development phase. In order to be able to test the board with a known-functional chip, the APV25 was chosen instead. The APV has 128 channels, which means that four and two chips are needed for the p-side and for the n-side, respectively, with 64 channels of one of the p-side chips left unused.

In the left part, the data and power lines are routed to four standard connectors; cables are then used to connect the board to the test system. This part is intended for test purposes only and will not be implemented in the final layout.

The layout of the sensor-readout part is very close to the final one. In principle, a larger flex for the readout of several sensors could be designed by replicating the sensor-readout part as many times as needed, and by routing the lines to the outside to appropriate connectors. However, the use of the APV instead of PASTA poses some limitations and makes the design of a larger flex harder:

- the length of the APV (8.055 mm) is much larger than that of PASTA (3.4 mm); this leads to a smaller area available on the back end for the routing;

- the position of the power pads on the two chips is different; in particular, the APV features three blocks of power pads on the front side, complicating significantly the fanout structure. With this problem in mind, PASTA has been explicitly designed to avoid this by having all the power pads on the back side;

- the APV requires more data lines to connect to the outside, making the back end side of the board more crowded. In particular, the APV requires three differential pairs and three single-ended slow-control lines, while the e-link-based PASTA output will require only three differential pairs (this is however not true for PASTA_v1, which uses standard LVDS drivers for the input/output and requires a total of ten differential pairs).

Another important difference with respect to the final design is the lack of the MDC chip. The presence of this chip will change significantly the routing of the back end side by reducing drastically the number of lines that have to be connected to the outside. For these reasons, it was decided that a board with more than one sensor will only be built once the final readout components will be available.

The sensor-readout area of the board, excluding the fanout structures, is 64 mm long (slightly larger than the long edge of the sensor) and 46 mm wide. The width, obtained from the carbon fiber stave geometry, takes into account the space for the readout chips, as well as the area required to fold the board around the stave. The latter is delimited by two fold lines, placed 18 mm apart; because of the folding requirement, no components are allowed in this area. Two oval holes, 8 mm long and 4 mm wide, are placed above the openings of the cable duct on the stave. The cable duct will not be used in the prototype assembly, but the holes are there nevertheless to account for the occupied board space.

Each of the six chips is surrounded by the passive components required for its operation, i.e four filtering capacitors and one resistor. The chip is glued on a 8.8×7.5 mm^2 copper pad, connected to a similar pad on the bottom layer by means of an array of 28 vias with a diameter of 400 μm; the system acts both as a ground and as a heat sink.

The fanout structures are implemented on both the p- and the n-side, with a considerably different layout. On the chip side, the pad arrangement follows the same technique employed in the flexible pitch adapters and shown in figure 5.6, with 50 μm vias on the pads of the back row. Additionally, the four APV power pads are implemented as well. On the p-side, the overall structure is almost identical to the one of the pitch adapters, whereas on the n-side the traces follow an L-shaped path which is necessary to reach the bond pads on the sensor. The n-side structure is implemented on a flap with dimensions compatible with the final MVD barrel stave layout. All the lines in the fanout structures

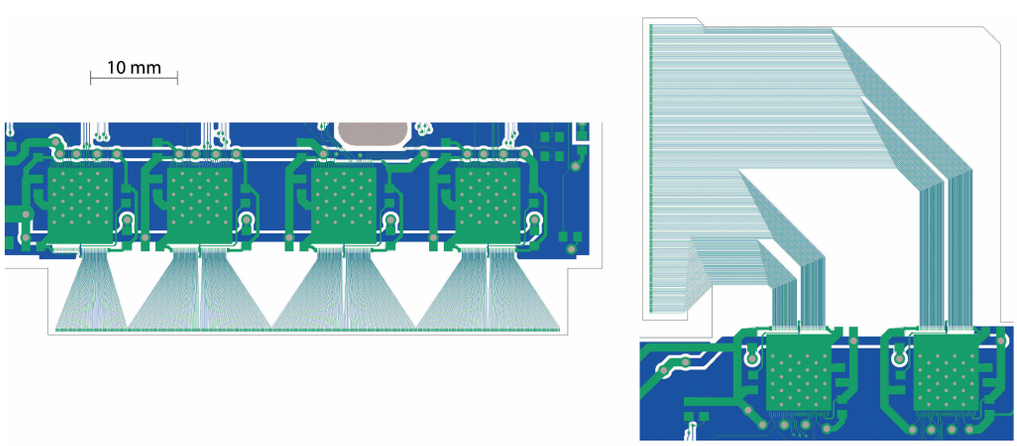


Figure 5.15: Layout of the p- and n-side fanouts on the second version of the chip carrier board.

are 35 μm wide, with a length ranging from 8.8 to 10.9 mm on the p-side and from 19 to 62 mm on the n-side. A detail of the two fanout structures is visible in figure 5.15.

To comply with the differential pair impedance control, the back-end lines are 35 μm wide and have a spacing of 100 μm, leading to a nominal impedance of 98 Ω. The single-ended lines are 100 μm wide. The clock and trigger lines are shared among all the chips on the same side of the sensor; the same applies for the two single-ended lines for the I^2C slow-control and for the reset line. In total, ten differential pairs (six on the p-side and four on the n-side) and six single-ended lines (three on each side) are therefore needed for the entire sensor.

In addition, two temperature sensors are implemented on the board, as close as possible to the silicon sensor. One is an NTC resistor, placed on the p-side and connected directly to two dedicated pins on the data connector; the other is a Texas Instrument TMP102 device [146], connected to the n-side I^2C bus.

Two separate p- and n-side ground planes share most of the area on the bottom layer of the board; coupling capacitors between the two grounds are foreseen in two different areas of the board.

To limit the board to a double-layer layout, power planes are not foreseen. Instead, the power supply lines for the readout chips are routed on the top and bottom layers. Four traces (for VDD and VDD/2 for both p- and n-side) run on the top layer from the connectors in the service part to the edge of the sensor-readout part; here the traces continue on the bottom layer, passing under the row of chips. In this way, every power line encounters a maximum of two vias, thus limiting the resistance. The high voltage sensor biasing is achieved through three traces running at the edges of the board to bonding pads placed close to the sensor.

On the service part of the board, three 4-pole connectors are used to route the power supply lines for the p-side chips, for the n-side chips and for the sensor high voltage, respectively. A Samtec LSH-020-01 fine pitch connector carries all the signals to and from the chips; the connector is placed across the edge between the two board grounds, with the left and right parts of the connector referenced to the p- and n-side grounds, respectively.

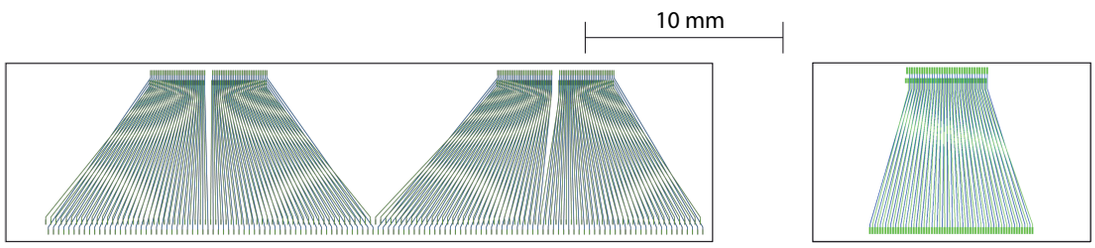
5.1.3.3 *Additional structures*

In addition to the chip carrier board described above, several additional structures were designed and placed on the same sheet, including different pitch adapters and a flexible cable. These are shown in figure 5.16.

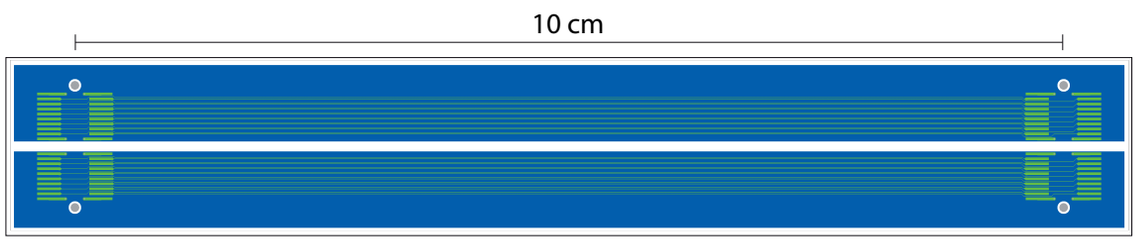
The redesign of the flexible cable was required by the double-sided readout implemented in the chip carrier board. The older cables featured twenty differential pairs referenced to a common ground; in the second version, the pairs are divided in two groups of ten pairs each, referenced to separate p- and n-side grounds. Only the 10 cm version of the cable was produced in this series. A redesign of the transition board, in order to implement the necessary data lines and the two separate grounds, was required as well (see appendix B).

Two different pitch adapters were implemented: a new version of the two-APV, 130 μm type shown on the right in figure 5.5, and a pitch adapter designed for PASTA. The layout of the newer APV-PA is almost identical to the old one, except for the presence of wider bond pads (70 μm instead of 50 μm on both the chip- and the sensor-sides) to facilitate the wire bonding procedure.

The second pitch adapter is part of the first evaluation test system for PASTA and is conceived to connect one 64-channel chip to an S4 "Baby" strip sensor, described in section 4.2.1 and connected with a floating strip scheme. It features a fanout structure between the 130 μm pitch on the sensor-side and the 63 μm pitch on the chip-side; the pads to the chip are staggered in two rows, symmetric to the pad rows present on PASTA, while the sensor pads are in one single row. (see also section 3.2.1); all the pads are 70 μm wide and have a length between 250 and 350 μm. The fanout concept follows closely the one used for the newer chip carrier boards and for all the other pitch adapters, described in section 5.1.2.1.



(a) *Left:* two-APV pitch adapter; *right:* PASTA pitch adapter.



(b) 10 cm flat cable.

Figure 5.16: Additional structures designed with the chip carrier board v2.

5.2 STAVE COOLING SYSTEM

The stave cooling system, described in section 3.3 and integrated in the general MVD cooling system, must be able to remove the heat dissipated by the active components of the detector and to keep the temperature of the sensors under control. This is especially important for the operation of the strip sensors, since their leakage current increases exponentially with the temperature. The detection of small signals is therefore quickly degraded with a rise of the sensor temperature; the design goal for the maximum temperature is in the order of $35 - 40°C$ [66].

This section is devoted to two different tests required for the validation of the cooling system of the strip barrels, performed at the ZEA-1 institute of the Jülich research center:

- the evaluation of the pressure drop along the cooling lines;
- the cooling tests of equipped stave prototypes.

5.2.1 *Pressure drop tests*

The location of the MVD at the heart of the experiment and the use of water as cooling fluid impose an underpressure operation within the detector volume to avoid any water leak in case of a damage to a cooling circuit. In order to guarantee the underpressure in the detector, the pressure of the water is regulated at the entrance of $\overline{\text{P}}$ANDA. The water enters the detector with a pressure equal to the ambient one, so that in all the subsequent parts of the circuit the pressure can only be lower. However, the pressure drops along the lines must be carefully controlled, so that the water can reach the circuit outlet with sufficient residual pressure. Since the properties of the pipes in the cooling circuit are fixed, the only parameter that can be tuned to control the pressure drop is the volume flow. A higher flow increases the cooling performances of the system, but introduces also a higher pressure drop; a compromise must thus be found, considering a maximum accepted drop along the entire line of 500 hPa.

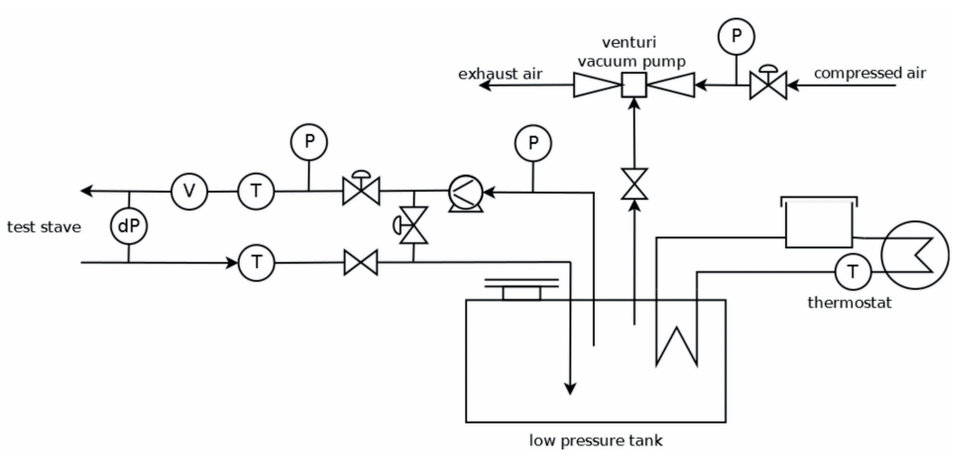


Figure 5.17: Scheme of the cooling circuit.

An experimental setup was developed in order to study the behavior of the underpressure flow of water through the stave and different type of pipes, as well as to perform the thermal tests on the stave described in the next section. The circuit is schematized in figure 5.17. In a closed, underpressure circuit, the water flows from a low pressure tank, through the device under test and back into the tank, where the water temperature is controlled in the range of 5 – 80°C by means of a heat exchanger. Along the circuit, several sensors allow to measure the temperature and pressure difference of the water between the stave inlet and outlet. The volume flow is measured as well and can be controlled in the range of 15 – 1000 mL/min. The underpressure is maintained in the water reservoir by means of a venturi vacuum pump.

A test to study the pressure drop through the entire cooling circuit of a stave was devised. In the strip staves, pressure drops are introduced by the flexible pipe from the manifolds to the barrel upstream edge, by the metal pipe embedded in the stave, as well as by all the connectors and bends. The circuit under test is composed of a metal U-tube with an inner diameter of 1.8 mm and a length of approximately 70 cm, connected on both ends to a flexible tube with an inner diameter of 2.5 mm and a total length of 2 m. This corresponds to the cooling circuit of a double stave in the outer strip barrel. Additionally, the pressure drop along different lengths of flexible pipe alone was evaluated.

The pressure drop at various water flows is shown in figure 5.18. At a water flow of 300 mL/min, a pressure drop along the entire circuit of 620 hPa is observed; at the same water flow, the 2 m flexible pipe causes a drop of 260 hPa. This allows to calculate the drop in the U-tube alone, which is in the order of 360 hPa.

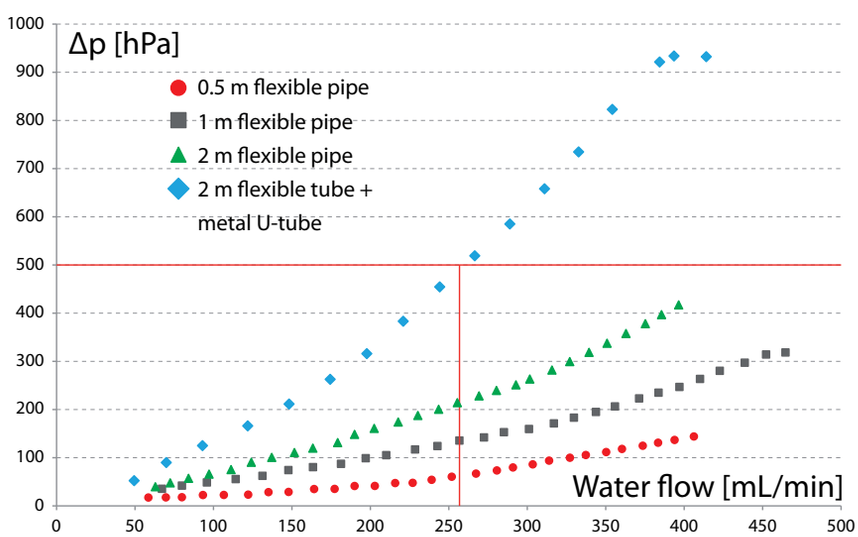


Figure 5.18: Pressure drop in the full stave cooling circuit, as well as in different sections of flexible pipe, for various water flows. In order to keep the pressure drop below 500 hPa, the volume flow cannot be higher than approximately 250 mL/min.

5.2.2 *Stave cooling tests*

An important step of the validation of the strip barrel cooling system is the measurement of the temperatures reached on the elements on the staves during operation. To achieve this, a carbon fiber stave, complete with the carbon foam block and the cooling pipe, is mandatory. The prototype must be then equipped with appropriate sources of heat, as well as with all the passive materials foreseen in the final design, such as the FPC between the chips and the stave.

For what concerns the readout electronics, each stave in the final layout foresees several 64-channel PASTA chips, described in section 3.2.1, each with a nominal power of 4 mW/ch, i.e., 256 mW per chip, and a size of 4.5×3.4 mm^2. The nominal power density is therefore expected to be in the order of 1.67 W/cm^2. The heat dissipation from the MDC chips, described in section 3.2.2, must also be taken into account; their expected power consumption is in the order of 200 mW for a size of 6×6 mm^2 (nominal power density 0.56 W/cm^2).

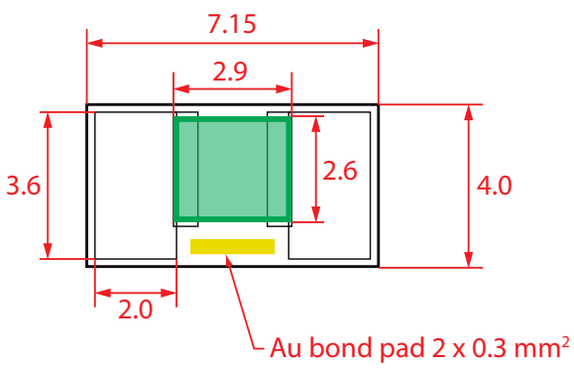
As described in section 2.5.3, the concept of the strip barrels cooling foresees a total of 24 circuits, each but two at the bottom of the outer barrel serving two adjacent staves. The power that has to be drained though these circuits depends on number of chips on the relevant staves. A review of all the circuits for the two barrels, with the expected figures for the number of chips and for the power consumption, is shown in table 5.6. The circuits for the central staves of the outer barrel, which have to drain the heat from 132 chips, are the most demanding ones, with a total expected power of 33.1 W (to which the heat dissipation in the sensors and in the cables must still be added). The power requirements for the other circuits, which serve fewer chips, range between 26.4 and 30.9 W per circuit (except the two bottom circuits of the outer barrel, which serve only one stave and, at 14.3 W, have a much lower power rating). The total electric power on the 46 staves of the two barrels is in the order of 700 W.

	Cooling circuit	Number of chips		Number of sensors		Power [W]		
		PASTA	MDC	square	rect.	chips	sensors	cables
Barrel 3	middle (6x)	104	10	2	8	28.6	0.5	7.17
	top/bottom (4x)	96	9	1	8	26.4	0.45	6.65
Total:	*10x*	*1008*	*96*	*16*	*80*	*277.2*	*4.8*	*69.6*
Barrel 4	middle (10x)	120	12	4	8	33.1	0.6	8.27
	top/bottom type A (2x)	112	11	3	8	30.9	0.55	7.75
	top/bottom type B (2x)	52	5	1	4	14.3	0.25	3.61
Total:	*14x*	*1528*	*152*	*48*	*104*	*421.4*	*7.6*	*105.4*

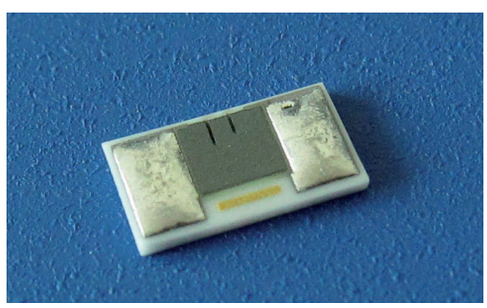
Table 5.6: Review of the cooling circuits. From the point of view of the cooling circuits the detector has a complete left-right symmetry, i.e., each category of circuit is equally split between the two detector halves. The power dissipated by the sensors assumes a post-irradiation scenario with a leakage current of 200 μA and a bias voltage of 250 V. The evaluation of the power dissipation in the cables, from which the values reported in the table are derived, can be found in section 5.3.

5.2.2.1 *Experimental setup*

At the time of the testing, neither the final readout electronics nor the full-sized FPC were available. It was therefore decided to simulate them by means of alternative components. Since there are many more PASTA chips than MDCs on the stave, and since both the power consumption and the power density of the MDC are lower than those of PASTA, within the scope of the thermal tests it was decided not to make any distinction between the two. All the chips on the stave were therefore replaced by dummy chips implemented with custom resistors and operated in order to simulate the behavior of PASTA. A layout and a photograph of the resistors are visible in figure 5.19, while their main properties are listed in table 5.7.



(a) Dimensions of one resistor with its soldering and bonding pads; all figures are in mm. The resistive element is pictured in green; most of the heating power is therefore concentrated in the center of the resistor [147].



(b) Photograph of a resistor. The black markings on the top are used by the manufacturer to fine-tune the value of the resistor down to 1%; however, they have the drawback of reducing the effective area of the resistive element, thus introducing large variations in the power density among the resistors.

Figure 5.19: Details of the dummy chip resistors.

Value	$100\,\Omega \pm 1\%$	Dielectric strength	8.3 kV
Power	600 mW	Dielectric constant	10 @ 10 MHz
TCR‡	$100 \cdot 10^{-6}/\mathrm{K}$	Number of layers	3
Material:	Al_2O_3 Alumina	Solder Pads	2 (PdAg + Tinned SnPb)
Thickness	0.7 mm	Bonding Pad	1 (Au)
Thermal conductivity:	$21\,\mathrm{W/m \cdot K}$	Encapsulation	Glass
CTE†	$7 \cdot 10^{-6}/\mathrm{K}$		

Table 5.7: Main properties of the dummy chip resistors. ‡Temperature Coefficient of Resistance; †Coefficient of Thermal Expansion.

The FPC is simulated with scrap material remaining from the FPC v1 prototype run, described in section 5.1.2; the cross section of the scraps used is the PCB-type, since it is the one with the thickest insulator and therefore the highest thermal resistance.

Several different tests have been done, with two stave prototypes: one reduced scale, 12 cm long stave, equipped with 10 dummy chips, and one full scale stave for the outer barrel, equipped with 66 dummy chips.

The experimental setup consists of two parts: the hydraulic circuit, described in section 5.2.1, to control and monitor the temperature and pressure of the water, and an infrared camera to measure the temperature on the stave prototypes. The electrical power dissipated by the resistors can be controlled as well. A photograph of the setup is visible in figure 5.20.

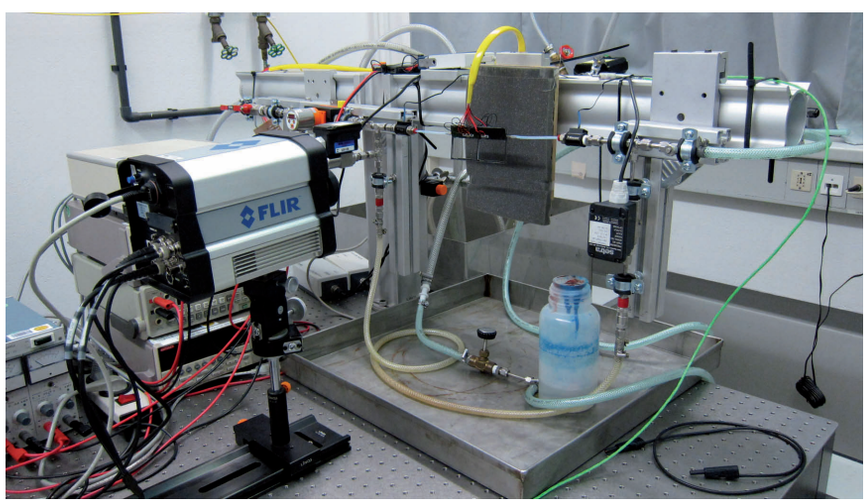


Figure 5.20: Photograph of the experimental setup for the stave cooling tests. In the picture, the reduced scale prototype is visible.

By knowing the temperature difference ΔT of the water between the stave inlet and outlet, the power carried away by the water can be calculated with the following:

$$P_{\text{hydr}} = \Delta T \cdot C_{\text{water}} \cdot \Phi / 60, \tag{5.4}$$

where Φ is the water mass flow in g/min and $C_{\text{water}} = 4.186\ \text{J}/(\text{g}\cdot\text{K})$ the heat capacity of the water.

Since the electrical power dissipated by the resistors is well known, the ratio between the hydraulic and the electrical power can be calculated with

$$R = P_{\text{elec}} / P_{\text{hydr}} \tag{5.5}$$

and it gives an idea of how efficiently the cooling system is removing the heat dissipated on the stave.

The temperature of the elements of the stave is measured through a FLIR SC6000 infrared camera, which has a spectral range of $8 - 9.2\ \mu\text{m}$, a resolution of 640×512 pixels and a frame rate of $1 - 125$ Hz [148].

The image from the camera is acquired on a PC-based system, which allows to set several measurement points and record and analyze their temperature over time. The temperature of the environment is controlled through the air conditioning system of the room. Since this method gives only an approximate information of the temperature of the air around the stave prototypes, for the last stage of the experiment the setup was improved by enclosing the prototype in a sealed polystyrene box, equipped with a heating plate and several temperature sensors.

5.2.2.2 *Short prototype*

The first stave prototype with integrated cooling system is a small-scale, 12 cm long stave, featuring the cutouts for two rectangular sensors. The prototype is visible in figure 5.21.

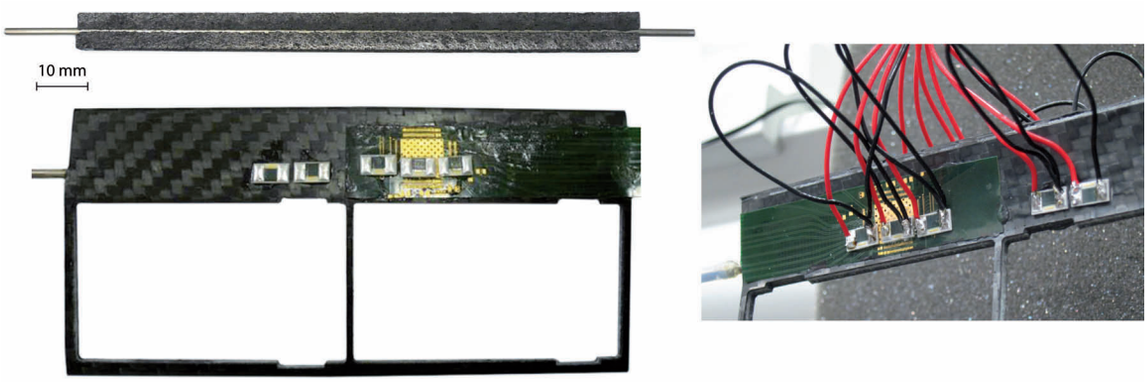


Figure 5.21: Short cooling prototype. *Top left:* cooling block (pipe, carbon foam); *bottom left:* entire stave with the resistors, seen from the top side; *right:* detail of the stave, seen from the bottom side, with the supply cables attached to the resistors.

A first test, conceived to study the distribution of the heat on the stave components, was performed before glueing the resistors and the FPC on the stave. Warm water at a temperature of 35°C was run in

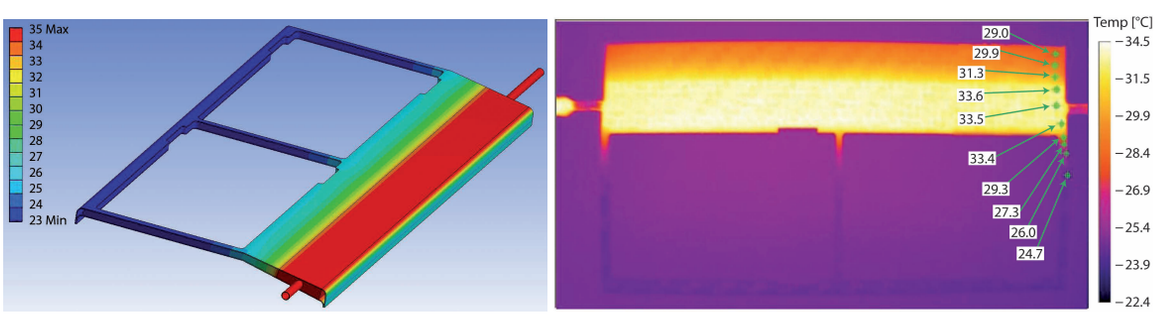


Figure 5.22: Short stave heating test: comparison of FEM analysis (*left*) and experimental results (*right*). The position of the block and of the pipe is defined differently in the two cases; despite this, the agreement is rather good. The shape of the carbon foam block embedded in the stave is clearly visible as a markedly brighter area, with the temperature sharply decreasing towards the room temperature in the sensor cutout part of the stave. All temperatures are in °C.

the pipe and the temperature of the stave, located in an environment at 23°C, was measured in several points. The experimental results were compared with the values obtained with a finite element method (FEM) analysis; both are presented in figure 5.22. The higher thermal conductivity of the carbon foam results in a region with a considerably higher temperature; this area, though not as sharply defined as in the FEM study, is clearly visible in the infrared thermal image.

Ten resistors, five on each side, were placed on the stave in the region above the cooling pipe. In order to study the effect of the FPC on the cooling performance, two of the resistors on each side were glued directly on the carbon fiber, while a piece of FPC was interposed between the other three resistors and the stave. Among the resistors placed on the FPC, one was glued on a large copper heat sink, one in a region where no copper was present and one in an intermediate location; in all cases, a silver-loaded conductive epoxy glue was used under the resistors [149].

A heating test with warm water at 35°C was repeated with the FPC and the resistors in place. The result is visible in figure 5.23; the copper structures on the FPC are clearly visible due to the different thermal conductivity of the materials. The temperature on the left half of the stave, where the FPC is present, are slightly lower than on the right. This is because the FPC is acting as a partial thermal shield between the carbon foam block with the warm water and the resistors; in the final application, however, this will translate in a worsened capability of the cold water to drain the heat away from the chips.

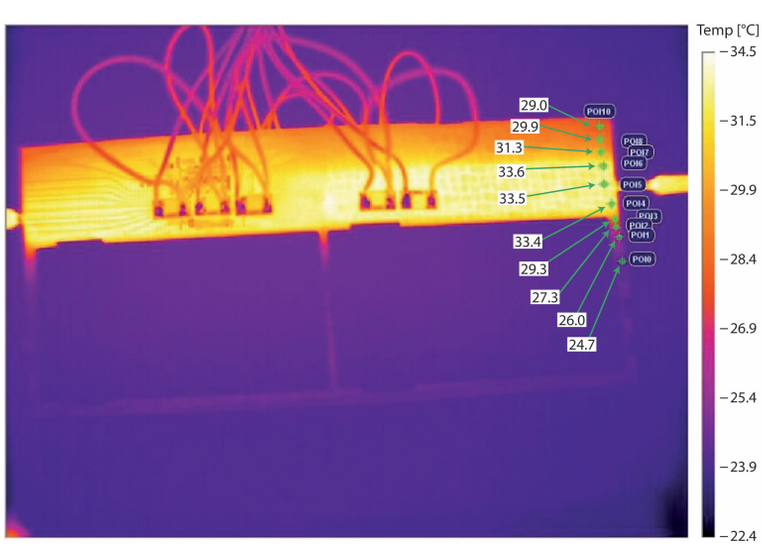


Figure 5.23: Short stave heating test: structural analysis; all temperatures are in °C. The FPC, as well as the copper structures implemented on it, are clearly visible as areas with a lower temperature.

A first evaluation of the cooling system with the resistors as heating elements was carried out by running cold water at a temperature of 20.2°C in the pipe, with a volume flux of 40 mL/min. The resistors were powered with a voltage of 4.61 V and a current of 0.452 A, resulting in an electrical power of 208 mW per resistor. The thermal image of the stave during the test is shown in figure 5.24; the temperature of the five resistors on the back side, as well as some measuring points on the stave, are indicated. The temperature rise of the water between the inlet and the outlet ports of the stave was

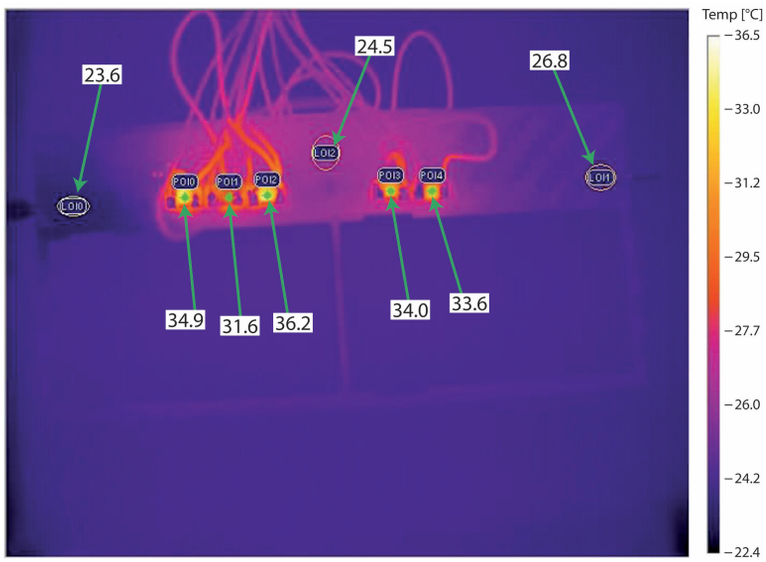


Figure 5.24: Short stave cooling test: temperature of the five resistors on the back side, as well as of some points on the stave; the water flows from left to right. The highest temperatures are measured on the first and third resistors from left, which are placed on the non-conductive part of the FPC. The second resistor from left is glued on the copper heat sink on the FPC and has the lowest temperature among all resistors. The two dummy chips on the right are glued directly on the carbon fiber and their temperature is between those of the other resistors. The rightmost point on the stave is measured directly on the carbon fiber; the two points on the left are measured on the FPC and feature lower temperatures, since they are partially shielded from the heat dissipated in the carbon foam block underneath. The environment has a temperature of 24°C; all other temperatures are also in °C.

measured to be 0.62 K; the resulting power that the cooling system is carrying away through the water is therefore 1.73 W, for an efficiency of 83%.

5.2.2.3 *Long prototype*

The second stave prototype is a full size, barrel 4 standard stave with a length of 31.5 cm and the cutouts for six sensors. The completed prototype is visible in figure 5.25.

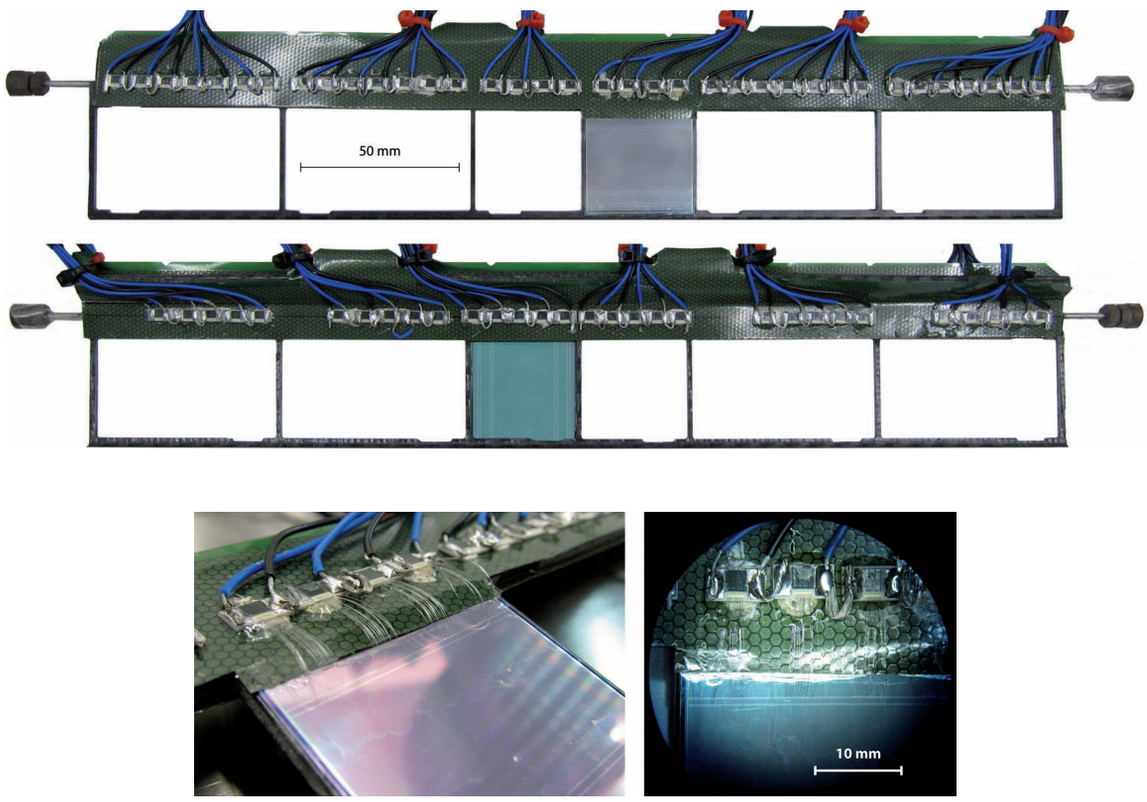


Figure 5.25: Long stave cooling prototype. *Top:* entire stave, top side with 36 resistors; *center:* entire stave, bottom side with the six groups of five resistors; *bottom:* details of the wire bonding between the sensor and the resistors.

It is equipped with 36 resistors on the top or p-side, uniformely distributed along the stave length, and with 30 resistors on the bottom or n-side, to simulate the 24 PASTA chips and the six MDCs; the resistors on the bottom are grouped in six groups of five chips, each group close to one sensor. Assuming for each resistor the nominal power consumption of PASTA, i.e., 256 mW, the total power dissipated on the stave is 9.2 W on the top side and 7.7 W on the bottom side. The resistors are cabled in twelve groups, one for each side of each sensor, which can be turned on independently.

As in the short stave prototype, the FPC is simulated with PCB-type scrap material from the FPC v1 prototype run, described in section 5.1.2. Additionally, in order to study the effect of the resistors on the temperature of the sensors, one square sensor was glued in its final position on the stave and wire bonded to the corresponding resistors. Because of its high reflectivity, an infrared measurement of the temperature of the sensor is difficult. This was partially mitigated by spraying a thin powder on the sensor, thus increasing its opaqueness.

In the first two tests, the temperature of each resistor on the stave surface was measured in order to study the temperature profile and variations along the stave length. The results for the front and back side are presented in figures 5.26 and 5.27, respectively.

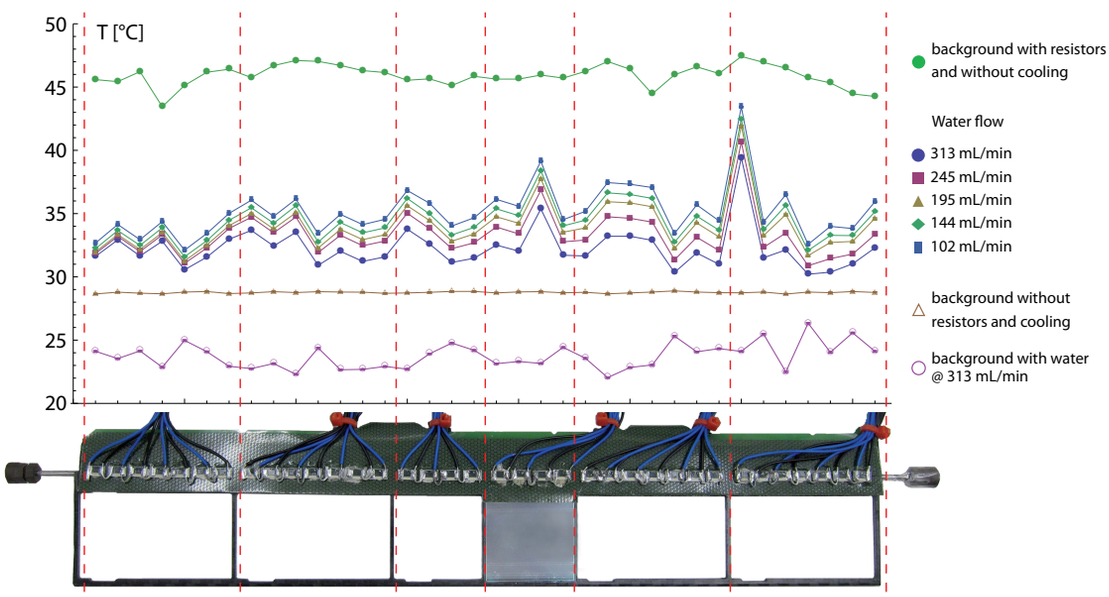


Figure 5.26: Profile of the temperature on the resistors on the long stave front side. The prototype is shown at the bottom of the picture indicating the position of the resistors. Five profiles measured with different water flows, as well as three background profiles, are shown in the plot. For all the profiles, the environment temperature is (28.5 ± 0.2)°C and the water at the stave inlet has a temperature around 20°C.

The measurements on the front side were performed with five different water flows, from 102 to 313 mL/min; additionally, three reference profiles are plotted for comparison. In the first, recorded without turning on neither the resistors nor the cooling system, the temperature is very uniform along the stave length and close to the environment temperature. A second background profile, measured without the resistors but with a cold water flow of 313 mL/min, shows lower temperatures with large variations among the resistors (the temperatures are between 22 and 26°C, with an average of 23.7°C and a standard deviation of 1°C). In the third reference profile, the cooling system was not running but the resistors were turned on, albeit with an electrical power of only 60 mW per chip. The variations in the temperature among different resistors are rather large, with temperatures between 22 and 26°C.

These reference plots suggest that a certain spread in the temperature of the resistors can be expected, due to both differences among the resistors (with the deviations caused by the fine-tuning engravings on the heating element of the resistors playing the biggest role) and to deviations in the properties of glue layer between the resistors and the FPC.

In the further measurements, the 36 resistors on the front side and the 30 resistors on the back side are connected in parallel and powered with a voltage of 3.28 V and a current of 5.15 A, corresponding to the nominal electrical power of 256 mW per resistor, or 16.89 W in total. Also in this measurement, the temperature profiles show large variations among the resistors, with standard deviations exceeding 2°C. As visible in figure, the variations are consistently replicated on each temperature profile: the effect of

the different water flows is to shift the entire profile to lower temperatures as the flow increases. The temperature of the seventh resistor from the right is between 7 and 9°C higher than the stave average; this is due to a defective glue layer under the resistor. The values for this resistor where therefore excluded in all the subsequent analyses. A summary of the results obtained in these measurements is presented in table 5.8.

Water flow [mL/min]	Water temperature [°C] inlet	outlet	$T_{out} - T_{in}$	Pdrop [hPa]	Hydraulic power [W]	P_{hydr}/P_{elec}	Average temperatures [°C] resistors *	sensor	stave
‡N/A	N/A	N/A	N/A	N/A	N/A	N/A	28.77 ± 0.06	29.07 ± 0.06	28.76 ± 0.08
†319.9 ± 0.8	19.743 ± 0.002	19.803 ± 0.001	0.060 ± 0.002	226.67 ± 0.11	1.33 ± 0.05	N/A	23.7 ± 1.0	27.51 ± 0.12	24.9 ± 1.2
312.7 ± 0.4	20.066 ± 0.003	20.828 ± 0.002	0.762 ± 0.003	208.51 ± 0.15	16.63 ± 0.08	0.985 ± 0.006	32.1 ± 1.1	28.80 ± 0.07	27.2 ± 0.9
244.5 ± 0.3	19.897 ± 0.001	20.882 ± 0.009	0.984 ± 0.009	113.6 ± 1.1	16.79 ± 0.16	0.994 ± 0.010	33.1 ± 1.3	29.28 ± 0.08	27.9 ± 0.8
195.0 ± 0.4	19.843 ± 0.001	21.055 ± 0.001	1.212 ± 0.002	75.9 ± 0.3	16.49 ± 0.04	0.976 ± 0.004	33.8 ± 1.4	29.61 ± 0.09	28.5 ± 0.9
143.9 ± 1.4	19.985 ± 0.002	21.628 ± 0.002	1.643 ± 0.003	50.5 ± 0.2	16.50 ± 0.16	0.977 ± 0.010	34.3 ± 1.5	29.90 ± 0.09	28.9 ± 0.9
101.8 ± 1.0	20.166 ± 0.001	22.400 ± 0.003	2.233 ± 0.003	46.13 ± 0.09	15.86 ± 0.16	0.940 ± 0.010	35.0 ± 1.6	30.15 ± 0.11	29.3 ± 0.9

Table 5.8: Results of the cooling test. The environment temperature is (28.5 ± 0.2)°C and the electric power dissipated in the 36 resistors is (16.89 ± 0.06) W.
*The average of the resistor temperatures does not take into account one resistor with a defective glue layer (see text). ‡Background profile with resistors and cooling switched off. †Background profile with resistors switched off and with water cooling running.

On the back side, the 30 resistors are not distributed uniformely, but are grouped in six groups of five resistors, as visible in figure 5.25. The temperature profiles, measured with two different water flows, show variations among the resistors even larger than on the front side, with a temperature range spanning over 8 and 10°C for the high and low water flow, respectively. The large variations, as well as the apparent rising trend from left to right in the temperatures in the central part of the stave, are probably caused by an uneven structure of the carbon foam block, or by an irregular coupling between the cooling system and the resistors.

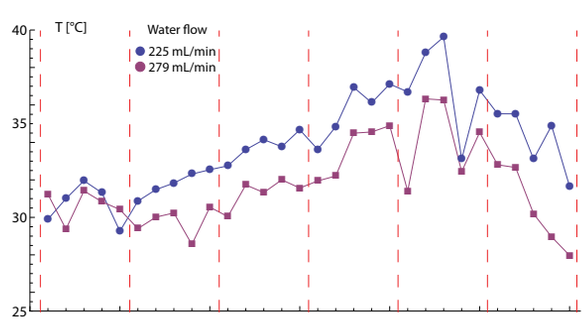


Figure 5.27: Profile of the temperature on the resistors on the long stave back side. The average temperature of the resistors is (33.9 ± 2.6)°C for the profile obtained with a water flow of 225 mL/min and (31.7 ± 2.2)°C for the profile measured at 279 mL/min.

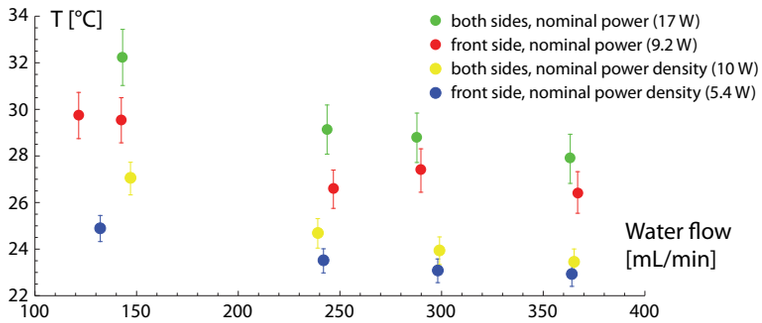


Figure 5.28: Average temperature on the front side resistors with different powering configurations: nominal power (256 mW per chip, i.e., power density of 2.84 W/cm^2) and nominal power density (1.67 W/cm^2, i.e., 150 mW per chip). Both measurements were repeated with only the 36 front-side resistors switched on. The environment temperature during the test was approximately 20°C.

The resistors used to simulate the front end chips, described in the earlier sections, were powered at the nominal chip power consumption (256 mW). They have an area of 28.6 mm^2, but the active area of the resistor is much smaller, in the order of 9 mm^2, far from the nominal size of PASTA (15.3 mm^2); this fact could introduce discrepancies because of the different power density. In order to study this effect, different measurements were performed varying the powering configuration of the resistors. Besides the standard measurement with the nominal power consumption, the nominal power density case was studied; additionally, a further test with both power configurations was done by switching off the resistors on the back side. The average temperatures on the front side resistors for several water flows in these four configurations are presented in figure 5.28.

The biggest effect is played by the variation of the power density, rather than by the total power: lower power densities lead to significantly lower resistor temperatures, regardless of the number of resistors switched on. When the back side is switched off, for a given power density a lower total power corresponds to lower temperatures; however, the nominal power, front side only-case features consistently higher temperatures than the nominal power density, both sides-case, despite having a slightly lower total power applied on the stave (9.2 versus 10 W).

The effect of the environment temperature was studied by using the possibility of controlling accurately the air temperature in the polystyrene enclosure. Five different series of measurements were performed, varying the temperature in the 26.5 – 43.3°C range; for each temperature, five water flows between 95 and 315 mL/min were applied, with the nominal electrical power settings (256 mW per resistor, i.e., 16.89 W in total). The temperature of the resistors, as well as that of the sensor and of several points on the stave, was measured; their values are reported in figure 5.29. Additionally, two examples of infrared images obtained during this measurement are shown in figure 5.30.

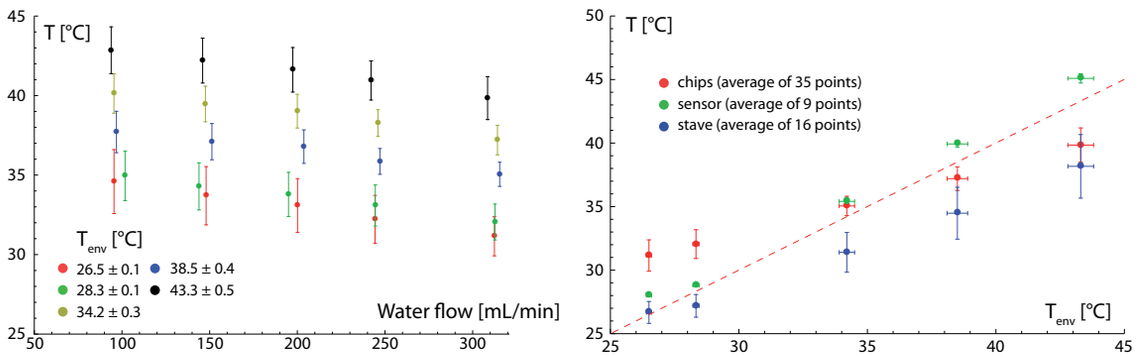


Figure 5.29: Long stave cooling test: study of the effect of the environment temperature. *Left:* average temperature of the front-side resistors, excluding the one with the defective glue layer, for different water flows and environment temperature. *Right:* average temperature of the front-side resistors, of the sensor and of the stave, for different environment temperatures and for a water flow of approximately 315 mL/min. The red dashed line indicates the points with a temperature equal to that of the environment; the stave temperature is consistently below the environment temperature, while the chips are warmer than the air for temperatures below a threshold of 35°C and colder above it. The temperature of the sensors is always slightly higher than that of the air; however, the high reflectivity of the silicon means that an accurate measurement of its temperature with the infrared camera is difficult, and the uncertainty reported in the plot is probably underestimated.

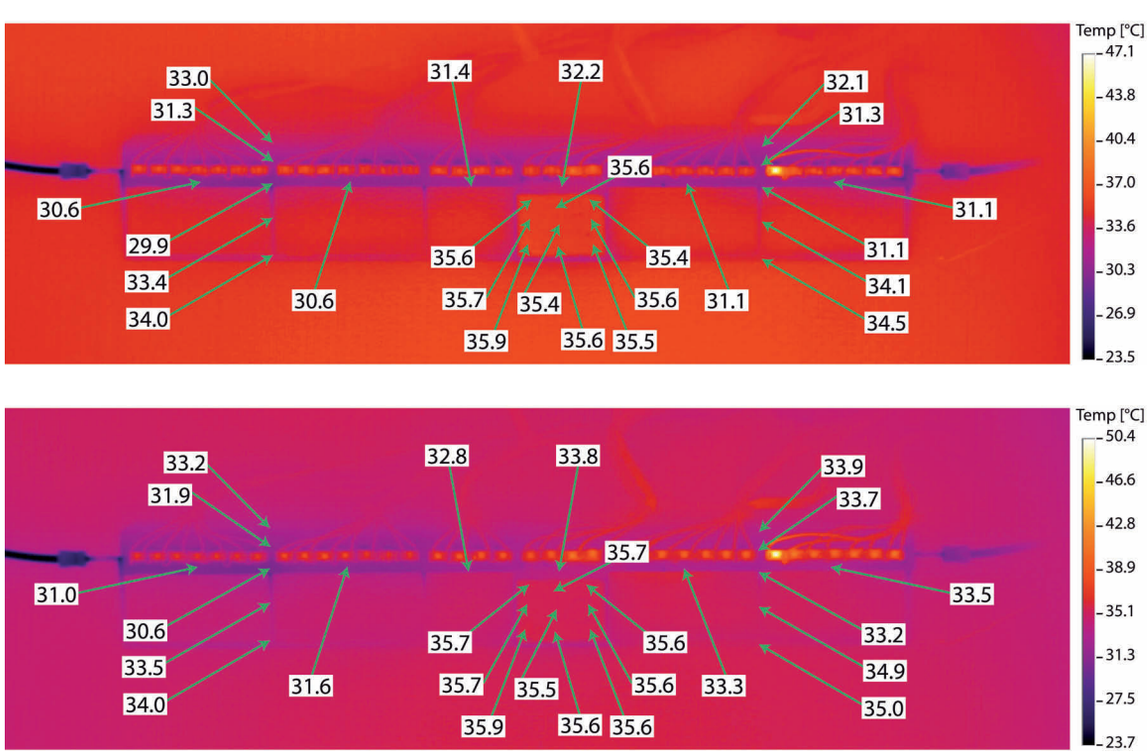


Figure 5.30: Long stave cooling test: infrared images of the stave with the test points on the sensor and on the stave, for two water flow settings. *Top:* water flow (247.1 ± 0.4) mL/min, environment temperature (34.5 ± 0.1)°C; *bottom:* water flow (96.8 ± 1.7) mL/min, environment temperature (34.1 ± 0.1)°C.

The ratio of the hydraulic power carried away by the water, calculated with equation 5.4, and the electric power dissipated in the resistors, for different water flows and environment temperatures, is shown in figure 5.31. At higher temperatures, the ratio is consistently above 1, i.e., more power is removed by the water than it is provided by the power supply. The cooling system is therefore not only removing the heat dissipated by the resistors, but is also partially cooling the air around the stave. This gives a hint that the system is, with the present settings, capable of removing heat in excess of the design values; however this is only the case when the ambient temperature is above a certain threshold. At lower temperatures, not all the electric power is removed by the cooling water, i.e., the surrounding air becomes warmer and contributes to cool the resistors down. One can therefore expect that, in the compact volume of the MVD with limited air convection and with the readout electronics as the only source of heat, the air temperature will quickly rise up to an equilibrium level at which the water cooling system will remove all the heat dissipated by the chips.

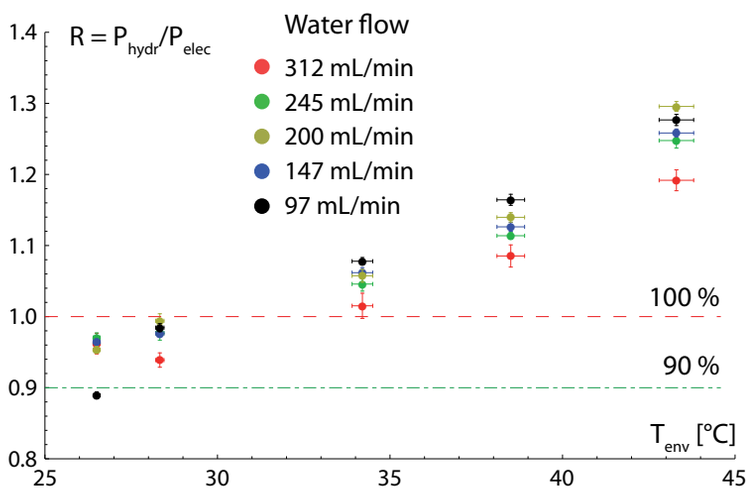


Figure 5.31: Long stave cooling test: hydraulic-electric power ratio.

5.3 POWERING AND CABLING

As described in section 2.5, the operation of the MVD requires the presence of complex systems for the power supply and for the data transmission, located close to the MVD in the services area around the beam pipe. These systems need to be connected by means of a very large number of cables to the MVD and to the outside world, avoiding at the same time any interference with the other detector and especially with the backward calorimeter. The topic of this section is the study of the requirements for the power and data cables and the layout of possible routing paths.

Despite the work in this thesis being focussed on the two strip barrels, some issues related to the routing of the services are better addressed at a detector level. The work related to the pixel detector and to the strip disks, developed in collaboration with INFN in Torino and with the Jülich research center, is therefore presented alongside the studies of the strip barrels.

5.3.1 *Detector powering scheme*

As introduced in section 2.5.2, the use of DC-DC converters is foreseen for the low-voltage powering of the front-end electronics of the detector.

The FEASTMP modules developed at CERN will provide the power supply to the ToPix chips in the pixel part and to the PASTA and MDC chips in the strip part. The converters accept an input voltage in the range 5 – 12 V; the output is limited to a maximum current of 4 A or, for output voltages higher than 2.5 V, to a maximum power of 10 W [106].

The DC-DC converters themselves are powered from the power supplies hosted in the racks located directly behind $\overline{\text{P}}$ANDA. Each power supply channel provides one Primary Supply Line (PSL), which is routed until the DC-DC services sector around the beam pipe; in order to save cables and power supply channels, it is desirable to merge the input of more DC-DC converters into a single PSL. Every PSL is kept on a floating ground with respect to all the other lines up to the power supply channels.

The current that has to be carried by the PSLs can be calculated from the required DC-DC output current, divided by the voltage conversion factor and by the DC-DC efficiency. The latter depends on

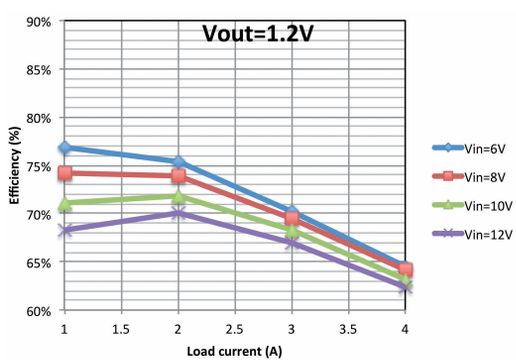


Figure 5.32: Efficiency of the FEASTMP DC-DC converter modules for an output voltage of 1.2 V and different input voltages and load currents [106].

a number of factors, including the input and output voltage, the output current and the effectiveness of the cooling system to which the DC-DC module must be attached. For an output voltage of 1.2 V and for output currents between 1 and 2 A, the efficiency ranges from 68 to 77% and is higher for low input voltages and currents around 2 A, as shown in figure 5.32. No data is available from the manufacturer about the module conversion efficiency for output currents below 1 A; a test setup was therefore devised to study the conversion efficiency in this current range. The efficiency decreases first by about 10% when decreasing the output current from 1 A to 0.5 A and then drops sharply to 40% and below for currents in the order of 100 – 200 mA [150].

5.3.1.1 *Strip powering*

In the strip part, the power supply system must provide the low voltage to the PASTA and to the MDC chips, as well as the high voltage biasing to the sensors. In the final version, both chips will require a 1.2 V supply for their digital circuitry; additionally, PASTA will need also a 1.2 V supply for its analog part. On PASTA, two independent power supplies are required in order to avoid the noise from the fast-switching digital part from affecting the more sensitive analog part. Additionally, because of the high voltage biasing of the sensor, the chips on the p- and n-side must be powered separately; for the same reason, chips on different sensors cannot be powered together.

In order to evaluate the cable cross section and to allocate the DC-DC converters, the expected power consumption of the chips must be considered. The nominal values of PASTA and of the MDC, increased by a safety factor of 2 and 1.5, lead to a current of 275 mA and 150 mA for the PASTA analog and digital lines, respectively, and of 250 mA for the MDC.

The designed powering scheme is shown in figure 5.33. The line providing the analog voltage to seven PASTA chips must carry approximately 1.93 A; all the other lines have somewhat lower requirements. As a consequence, a single DC-DC can be used to supply each of the four power domains on

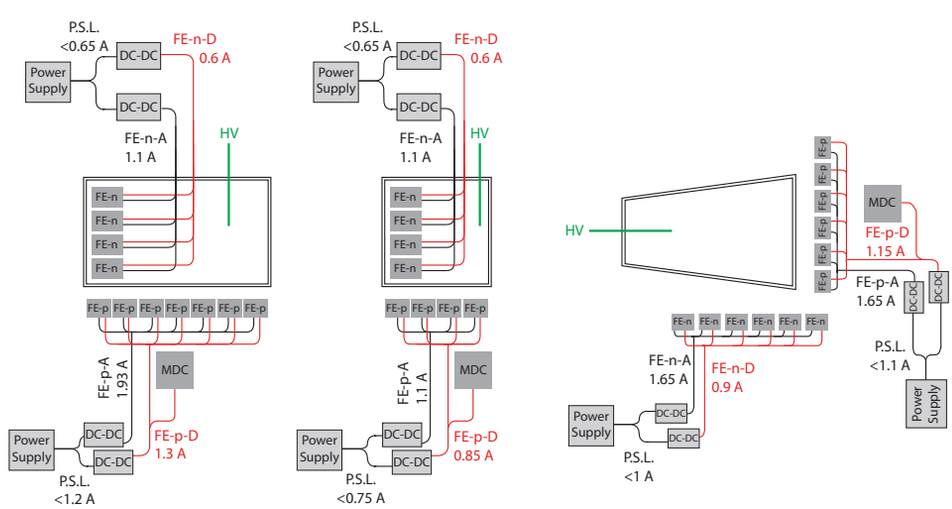


Figure 5.33: Strip powering scheme. *Left:* rectangular and square sensors for the barrel part; *right:* trapezoidal sensors for the disk part. The current carried by each powering line, as well as the upper current limit of the Primary Supply Lines (PSL) is indicated.

one sensor (analog and digital for the p- and n-side); the MDC can be easily powered from the digital supply line on the p-side. A total of four converters are therefore needed for each sensor, both in the barrels and in the disks; the 296 strip sensors in the MVD thus require 1184 DC-DC converters.

Not all of the 1184 converters require an individual PSL; however, there are some limitations in the possibility of merging the DC-DC input lines. The most severe is that, because of the high voltage biasing of the sensor, DC-DC converters powering different sensors, or different sides of the same sensor, must remain completely independent from each other. It is however possible to merge the DC-DC input lines for the analog and digital domains on the same sensor side, since the DC-DC converters provide a sufficient shielding to decouple the analog part from the noise generated in the digital part. This leads to a reduction of the number of PSLs by a factor 2, down to 592 lines.

The output currents required for the strip power lines lie between 0.6 and 2 A. Considering a worst-case efficiency of 65%, the necessary input current for different input voltages can be calculated. The results are presented in table 5.9: with the lowest input voltage, the currents range from 220 to 710 mA, while for an input voltage of 12 V the highest current is 300 mA. At the PSL level, the highest current with a 5 V input is in the order of 1.2 A and decreases to 0.5 A for an input voltage of 12 V.

With the above mentioned worst-case efficiency of 65%, a considerable amount of heat, ranging from 0.4 to 1.25 W per device, is dissipated in the DC-DC converter itself and must be removed with an efficient water cooling system.

	I_{out} [A]	P_{out} [W]	P_{loss} [W]	I_{in} [A] ($V_{in} = 5$ V)		I_{in} [A] ($V_{in} = 8$ V)		I_{in} [A] ($V_{in} = 12$ V)	
				DC-DC	PSL	DC-DC	PSL	DC-DC	PSL
rectangular, p-side, analog	1.93	2.32	1.25	0.71	1.19	0.45	0.75	0.30	0.50
rectangular, p-side, digital	1.3	1.56	0.84	0.48		0.30		0.20	
square, p-side, analog	1.1	1.32	0.71	0.41	0.72	0.25	0.45	0.17	0.30
square, p-side, digital	0.85	1.02	0.55	0.31		0.20		0.13	
rect./square, n-side, analog	1.1	1.32	0.71	0.41	0.63	0.25	0.39	0.17	0.26
rect./square, n-side, digital	0.6	0.72	0.39	0.22		0.14		0.09	
trapezoidal, p-side, analog	1.65	1.98	1.07	0.61	1.03	0.38	0.65	0.25	0.43
trapezoidal, p-side, digital	1.15	1.38	0.74	0.42		0.27		0.18	
trapezoidal, n-side, analog	1.65	1.98	1.07	0.61	0.94	0.38	0.59	0.25	0.39
trapezoidal, n-side, digital	0.9	1.08	0.58	0.33		0.21		0.14	

Table 5.9: Current requirements of the DC-DC converters in the strip part. The powering lines for the strip detectors can be grouped in ten categories; for each of them are listed the required output current and power, the power lost in the DC-DC due to the conversion inefficiency and the input currents for three different input voltages. The PSLs are obtained merging the analog and digital lines for each sensor side; the required currents are listed as well. A worst case efficiency of the DC-DC converters of 65% has been considered for these calculations.

5.3.1.2 *Pixel powering*

As for the strip chips, in the pixel part the ToPix chip requires two separate power supplies for the analog and the digital part, both at 1.2 V. A current of 1.4 A for the digital part and 0.25 A for the analog part, which take into account an appropriate safety factor, have been considered for the cable estimations. The powering scheme must also provide the high voltage biasing to the pixel sensors.

The current pixel powering scheme is shown in figure 5.34. As in the strip part, the powering of the chips on different sensors must be independent. The presented solution foresees one single DC-DC converter for the analog supply of all the chips on one sensor module and the digital supply shared among one to three converters, depending on the sensor size. Being limited to a current of 4 A, each DC-DC can provide the digital power supply to at most two chips, unless the digital power consumption of ToPix can be reduced slightly. In this case, three chips could be powered through the same line.

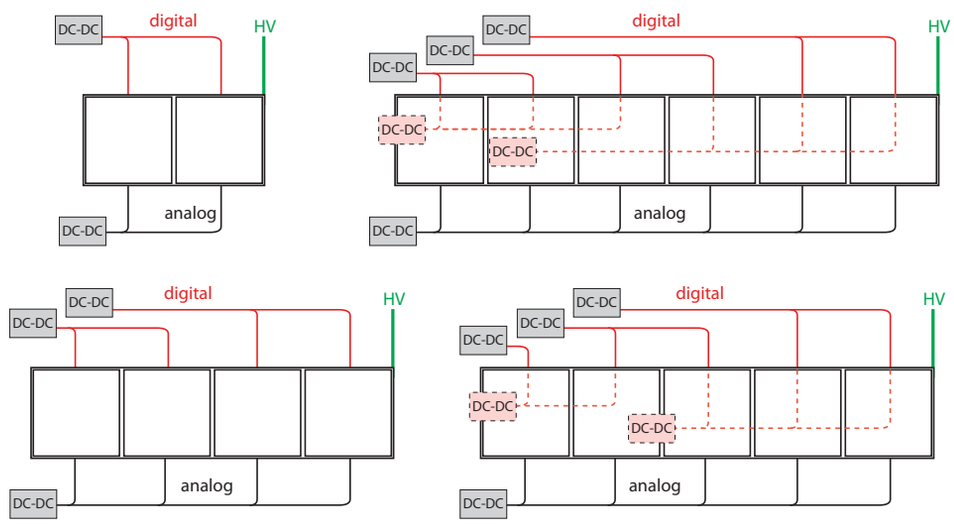


Figure 5.34: Pixel powering scheme. In the S5 and S6 modules, the solid and the dashed lines in the digital part represent the solution with two and three chips powered from the same line, respectively.

In the more conservative scenario, a total of 608 DC-DC converters are needed for the full pixel part of the MVD; the powering of three ToPix chips from the same line would lead instead to a total of 494 DC-DC converters. Each DC-DC converter is connected to a separate PSL, whose number is therefore identical to that of the DC-DC boards. Since it is more demanding for the arrangement of the services, the conservative scenario will be considered in the following.

Considering the ToPix current consumption and the DC-DC conversion efficiency, the input current of the converters ranges, in the worst case (i.e., at the lowest possible input voltage), from 0.5 A (on the analog supply line for the S2 module) up to 1 A in the two chips scenario (on the digital supply lines which serve two chips) or up to 1.5 A in the three-chips scenario (on the digital supply lines which serve three chips).

5.3.2 *Cabling and services routing*

The evaluation process of the distribution and routing of the cables for the MVD requires several steps, concerning cables of several types. The first step is therefore to point out the different cable categories and identify their connection points.

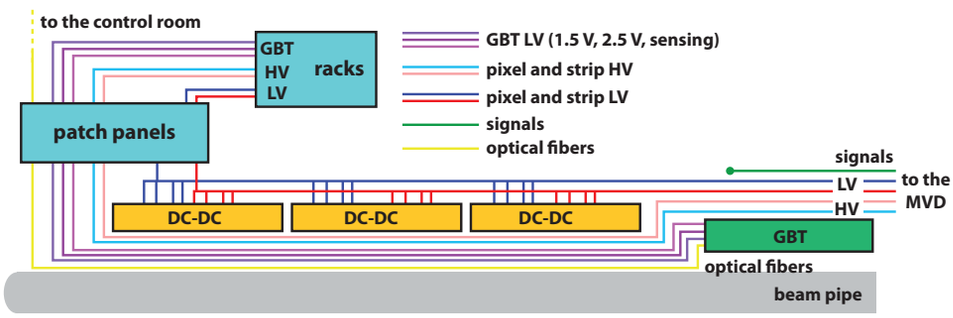


Figure 5.35: General plan of the cable routing between the MVD and the racks, with possible paths along the beam pipe through the DC-DC and GBT sectors (drawing not to scale).

With reference to the schematic presented in figure 5.35, five main categories can be identified:

1. Low Voltage (LV) cables for the pixel and strip detectors: these cables are first routed from the power supplies in the rack, to the patch panels located behind the $\overline{\text{P}}$ANDA detector, immediately next to the beam pipe, to the DC-DC converters and finally to the MVD.
2. High Voltage (HV) cables for the strip and pixel detectors: these cables are routed from the power supplies to the patch panels and then directly to the MVD;
3. signal cables: these cables transmit the electrical signals from the detector modules in the MVD to the GBT boards in the service sector around the beam pipe;
4. optical fibers: these are routed from the GBT boards to the patch panels and from there directly to the control room;
5. LV cables for the powering of the GBT boards, routed from the power supplies in the rack, through the patch panels and to the GBT boards.

Each category has individual requirements and, even within the same category, different types of cables have to be used in different regions.

5.3.2.1 *Low Voltage cables for pixel and strip detectors*

For what concerns all the LV cables, the diameter must be chosen in order to limit the voltage drop along the lines to tolerable levels. This is important for two reasons: firstly, a large voltage drop leads to a large heat dissipation in the cables, which is detrimental to the detector operation and poses additional demand on the cooling system. Secondly, the voltage drop along the cable is directly proportional to the current flowing in it. If the current consumption drops significantly, due for instance to

lower data rates or to a malfunction in one chip, the voltage drop decreases accordingly, thus leading to a higher voltage at the point of delivery, with potentially harmful consequences for the electronics. A small voltage drop at the nominal current values means that the possible voltage swing at the delivery point because of current variations is also small.

For a cable with a length L and a conductivity ρ (expressed in m and $\Omega \cdot \mathrm{m}$, respectively), the minimum diameter d, expressed in mm, can be calculated with the following formula:

$$d = 2 \cdot \sqrt{\frac{L \cdot \rho \cdot I}{\pi \cdot V_{\mathrm{drop}}}} \cdot 1000, \tag{5.6}$$

where I is the current in A and V_{drop} the maximum accepted voltage drop, expressed in V, along the entire cable length.

The path of the LV cables can be divided in three regions:

- inner cables, from the detector modules to an area immediately outside the MVD where connectors can be placed;
- outer cables, from the above mentioned connectors to the DC-DC converters;
- Primary Supply Lines (PSLs), connecting the inputs of the DC-DC converters to the power supplies in the racks, with an interruption in the patch panels.

In the inner part of the detector, in order to reduce both the cable cross section and the material budget, it is foreseen to use thin enameled cables made of Copper-Clad Aluminum (CCA). The use of enamel instead of a traditional plastic cladding provides an excellent insulation while reducing dramatically the total cross section, at the expense of a more difficult handling. As for the conductor material, CCA cables offer a good combination of the advantages of copper, such as easy solderabily and a lower electrical resistance, and the low density of the aluminum. A CCA10% cable, consisting of an aluminum core and a concentric copper cladding amounting to 10% by volume, has a density of 3.3 $\mathrm{g} \cdot \mathrm{cm}^{-3}$ (compared to 2.7 $\mathrm{g} \cdot \mathrm{cm}^{-3}$ and 8.8 $\mathrm{g} \cdot \mathrm{cm}^{-3}$ for aluminum and copper, respectively) and a conductivity of 37.5 $\mathrm{S} \cdot \mathrm{m}/\mathrm{mm}^2$ (against 35.85 $\mathrm{S} \cdot \mathrm{m}/\mathrm{mm}^2$ for aluminum and 58.5 $\mathrm{S} \cdot \mathrm{m}/\mathrm{mm}^2$ for copper) [151].

In the pixel detector, CCA cables with a diameter of 0.5 mm will be used from the detector modules up to a transition board region, located directly upstream from the MVD; copper enameled cables with a diameter of 0.8 mm will be used from there to the DC-DC boards. One copper wire pair per DC-DC converter, i.e., 608 pairs, will be used from the converters to the transition region; from there, some lines will be split into multiple cables, thus requiring a total of 1100 CCA wire pairs for the inner part.

The disk part of the strip detector will be powered through CCA cables running directly from the DC-DC boards to the sensor modules; considering a maximum voltage drop of 200 mV and a roundtrip length of 6 m, a total of 192 pairs with diameters ranging from 1 to 1.3 mm will be therefore needed. The availability of CCA cables with such a diameter is still to be verified, so that it might be necessary to split the lines into many smaller wires.

Wire diameter [mm]	Cross section [mm^2]	Number of pairs per stave			
		Barrel 4		Barrel 3	
		middle	top/bottom	middle	top/bottom
0.15	0.018	5	5	5	5
0.25	0.049	11	9	9	5
0.30	0.071	3	1	2	2
0.35	0.096	2	2	3	3
0.40	0.126	2	2	0	0
0.45	0.159	1	1	1	1
Total pairs:		*24*	*20*	*20*	*16*
Total cross section: [mm^2]		*2.89*	*2.41*	*2.24*	*1.85*
Dissipated power [W]:		*4.14*	*3.61*	*3.58*	*3.06*

Table 5.10: Specification of the LV cables to be used in the cable duct in the barrel staves. The number and the diameter of the pairs foreseen in each of the four stave types is indicated, as well as the total number of pairs per stave, the total cross section and the power dissipated in the cables.

In the barrel, thin CCA wires will be used inside the cable duct in the stave, connecting the FPC to the power connector at the edge of the stave. From there, copper wires will run up to the DC-DC boards; a total of 992 copper pairs, with diameters ranging from 0.75 to 1.3 mm, will be needed for this part. As for the cables inside the stave, the small space available in the cable duct must accommodate four pairs per sensor, i.e., between 32 and 48 wires per stave. The wire lengths involved are very small, ranging from 30 to 280 mm, thus allowing for the use of very thin wires. A detailed optimization study, taking into account the length and current rating of each individual pair and a maximum voltage drop of 100 mV (in addition to another 100 mV on the copper wires from the DC-DC boards to the connector), leads to the cable specifications presented in table 5.10. From the current rating and the chosen diameter, the amount of power dissipated in the cables due to the voltage drop can be evaluated as well; this is also presented in the table.

For the Primary Supply Lines, thick cables containing four copper pairs each with a cross section of 0.35 mm^2 per wire and an external diameter of 7.5 mm have been chosen. A total of 300 of these cables, almost equally split between pixel and strips, will be required.

A review of all the low voltage cables with the corresponding cross sections in the different detector areas is presented in table 5.11.

	Pixel part		Strip part		
	barrels	**disks**	**barrels**	**disks**	***Total***
Power supplies to DC-DC (4-pair cables, 7.5 mm ext. diam., 0.35 mm^2 per wire)					
Number of cables:	59	93	124	24	*300*
Cross section [mm^2]	2596	4092	5478	1060	*13226*
Cross section $\cdot\, 4/\pi$ [mm^2]	3305	5210	6975	1350	*16840*
DC-DC to connectors upstream from MVD (Cu enameled cables)					
Number of pairs:	236	372	992	192†	*1792*
Wire diameter [mm]:	0.8	0.8	0.75 – 1.3	1.0 – 1.3	
Cross section [mm^2]	236	372	1548	423	*2579*
Cross section $\cdot\, 4/\pi$ [mm^2]	300	474	1971	538	*3284*
Connectors to MVD (CCA10% enameled cables)					
Number of pairs:	452	648	992	192	*2284*
Wire diameter [mm]:	0.5	0.5	0.15 – 0.45	1.0 – 1.3	
Cross section [mm^2]	178	254	116	423	*971*
Cross section $\cdot\, 4/\pi$ [mm^2]	226	324	148	538	*1236*

Table 5.11: Review of the low voltage cables. The cable path is divided in three regions: from the power supplies to the DC-DC converters (through the patch panels), from the DC-DC converters to the transition connectors immediately upstream from the MVD, and from there to the detector modules. For each region, the number of cables/pairs, their diameter and the total cross section are indicated. The square cross section (which counts every cable as a square, with the side equal to the effective diameter) is indicated as well and takes into account the space wasted when packing the round cables one next to each other.
†The cables for the strip disks run uninterrupted from the detector modules to the DC-DC converters and are realized in enameled CCA10%.

5.3.2.2 *High Voltage cables for pixel and strip detectors*

The definition of the high voltage cables for the biasing of the pixel and strip sensors is considerably simpler. Each of the 176 pixel sensors and each of the 296 strip sensors requires an independent high voltage line, coming from the power supplies in the racks. Coaxial cables with a diameter of 1.3 mm have been proposed for this application; the 472 cables have a total cross section of approximately 630 mm^2 and will have to cross the entire DC-DC and GBT service region, without any interruption other than at the patch panels.

5.3.2.3 *Signal cables and optical fibers*

For the data transmission between the sensor modules and the GBT boards, flat aluminum microstrip cables will be used [129]. Each cable is composed of two aluminum layers laminated on a polyimide substrate and implements several differential pairs referenced to a common ground plane; the prototypes realized have an overall thickness of about 200 μm, a strip width and pitch of 100 – 150 μm and a total width of several mm, depending on the number of pairs implemented. A photograph of some prototypes is visible in figure 5.36.

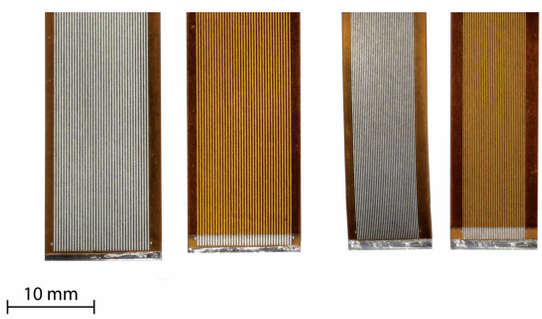


Figure 5.36: Prototypes of flat aluminum microstrip cables.

Each pixel module, as well as each barrel stave and disk quarter, will require one flat cable with a width between 10 and 14 mm. A total of 230 cables will be therefore used; their routing is particularly challenging because of the handling difficulty and of the large bending radius.

The data from the GBT boards will be transmitted to the control room through optical fibers; each board requires two fibers, with a diameter of about 1 mm each. Considering the actual MVD services design, which foresees 192 GBT boards in the service area, a total of 396 fibers will have to be routed to the outside, with an interruption at the patch panels. In case more GBT boards were needed, for the reasons explained in section 2.5.1, the number of fibers would have to be increased accordingly.

5.3.2.4 *Low Voltage cables for the GBT boards*

The powering system for the GBT boards must supply the two separate voltages (1.5 and 2.5 V) required by the electro-optical transceivers. As for the optical fiber count, this evaluation considers the actual design with 192 GBT boards on 12 bars and would have to be significantly modified in case of a different GBT boards allocation.

The preferred solution for the powering of the GBT boards would be the use of the same DC-DC converters employed for the on-detector electronics; however, the lack of space in the DC-DC sector does not allow to accommodate all the needed converters. The proposed solution requires therefore to provide the supply to the GBT boards directly from the power supplies in the racks. The powering and cabling scheme of one GBT half-bar, including the optical fibers, is shown in figure 5.37. The expected power consumption of the GBT boards is such that one power supply channel can provide the required current to two boards, connected in a daisy chain. A half-bar with eight GBT boards will therefore need four channels at 2.5 V and four channels at 1.5 V; two four-pair cables with different cross section will be used for both voltages. A third cable with 16 wires will provide the sensing to all

the voltages delivered to one half-bar; the use of sensing allows for thinner power cables with a larger voltage drop. Globally, each of the 24 half-bars will therefore require three cables with an external diameter of 6.8, 7 and 8.5 mm, or 72 cables for the entire GBT area.

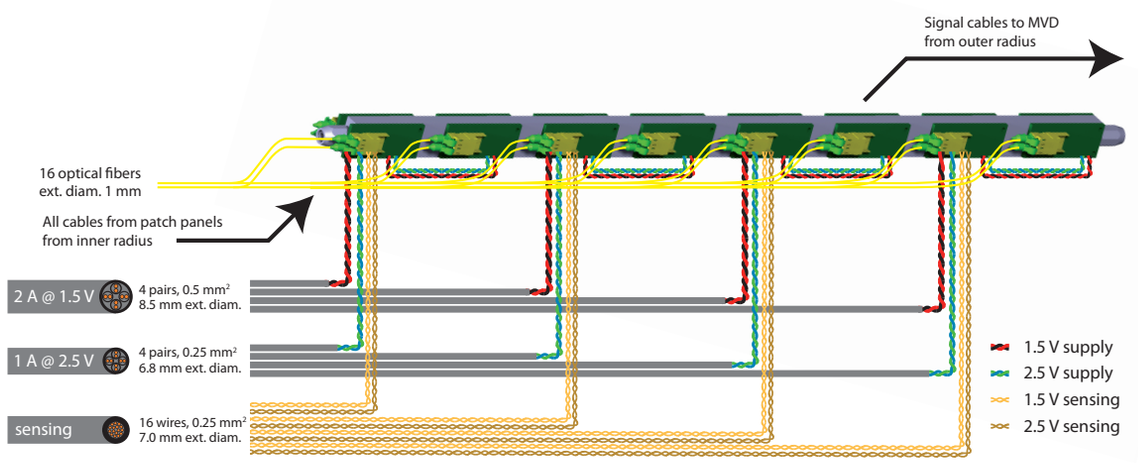


Figure 5.37: Powering and routing scheme of one half-bar with eight GBT boards. 24 of such half-bars are presently included in the MVD services design.

5.3.2.5 *Cable cross sections and routing*

Once the properties for the different categories of cables have been listed, the paths able to accommodate the expected cross sections have to be evaluated.

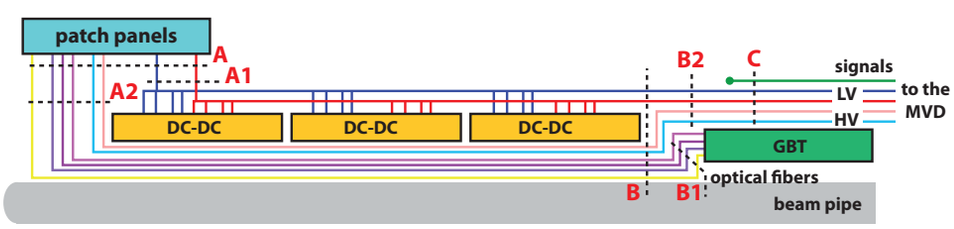


Figure 5.38: Cable routing and cross sections in the MVD service area.

A possible cable routing through the service area located between the upstream edge of the MVD and the patch panels is shown in figure 5.38.

The cable cross section varies along the length of the service area; three points have been therefore identified as critical:

- section A, including all the cables coming out of the patch panels, furtherly subdivided in A1 (the cables going to the DC-DC converters) and A2 (all the other cables, which are traversing the DC-DC area uninterrupted);
- section B, immediately downstream from the DC-DC converters, subdivided in B1 (cables terminating on the GBT boards) and B2 (cables continuing towards the MVD);

- section C, including all the cables surrounding the GBT sector.

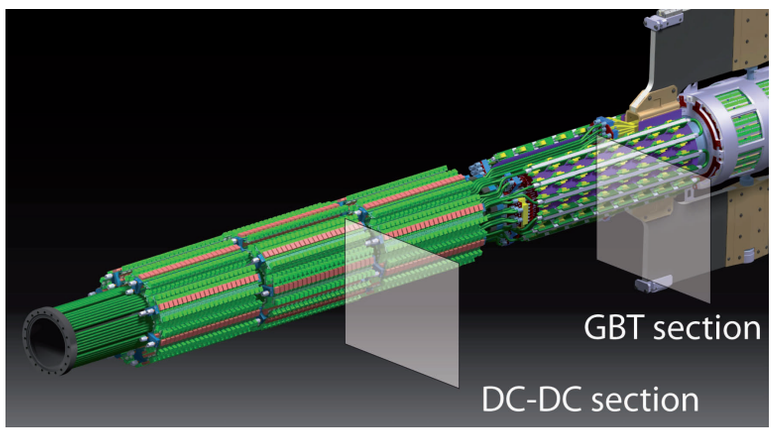
The type, diameter and cross section of the cables present in the three points listed above are presented in table 5.12.

Section name		LV FEE	HV	Signal	Optical fibers	LV GBT	Total
A	A1	300 ∅ 7.5 mm 16876 mm^2					**300 cables** **16876 mm^2**
	A2		472 ∅ 1.3 mm 797 mm^2		396 ∅ 1.0 mm 396 mm^2	72 ∅ 6.8 – 8.5 mm 4020 mm^2	**940 cables** **5213 mm^2**
B	B1				396 ∅ 1.0 mm 396 mm^2	72 ∅ 6.8 – 8.5 mm 4020 mm^2	**468 cables** **4416 mm^2**
	B2	3584 ∅ 0.75 – 1.3 mm 3284 mm^2	472 ∅ 1.3 mm 797 mm^2				**4056 cables** **4081 mm^2**
C		3584 ∅ 0.75 – 1.3 mm 3284 mm^2	472 ∅ 1.3 mm 797 mm^2	230 (0.2 × 10 – 14) mm^2 644 mm^2			**4286 cables** **4725 mm^2**

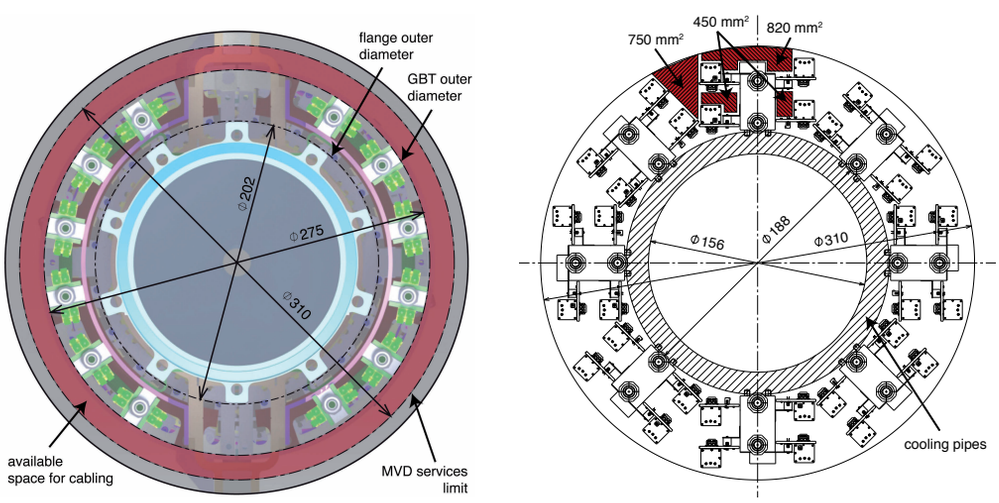
Table 5.12: Summary of the total cable cross section at several points in the detector. For each point the number of wires/cables, their individual dimension (where applicable) and the total square cross section (total cross section multiplied by $4/\pi$) are indicated.

In the GBT boards area, depicted in figure 5.39b on the left, the most critical point is close to the upstream edge of the MVD, where all the cables belonging to the section C have to be hosted. These include over three thousand thin enameled copper wires for the low voltage, the high voltage cables and the flat aluminum microstrip data cables. The cross section available in the shell between the outer diameter of the GBT boards and the outer limit of the MVD services is in the order of 16000 mm^2 and can easily accommodate all the required cables, which have a cross section of about 4300 mm^2. However, this number does not take into account the space required to bend and rotate the flat data cables. This is hard to estimate without building a life-size mock-up of the area, but one can expect that a considerably larger cross section will be required. Once again, it is worth reminding that neither the number nor the layout of the GBT boards are final and therefore the proposed layout of the GBT area could still be subject to major changes.

The cables that have to be accommodated in the DC-DC converter area belong to two categories: the LV cables connected to the DC-DC boards and the through cables (section A2), which include the optical fibers and the HV and GBT-LV cables. Concerning the first category, at the upstream edge of the DC-DC sector only 300 thick cables are present; these are gradually replaced with over 3500



(a) Overview of the MVD service area, with two cutout sections indicated.



(b) Cross section of the GBT boards area (*left*) and of the DC-DC converters area (*right*); all figures are in mm. The space available for the passage of the cables is indicated in red in the drawings: in the GBT board area it consists of the shell between the GBT outer diameter and the MVD services limit, with a diameter between 275 and 310 mm; in the DC-DC converters area the available space is split into several small regions.

Figure 5.39: Cable cross sections in the MVD service area.

thin enameled copper wires as one proceeds toward the MVD. The cross section starts from almost 17000 mm^2 at the upstream edge and becomes of about 3300 mm^2 at the downstream edge, with intermediate values between the two points.

The cross section of the DC-DC converters area is shown in figure 5.39b on the right. The total available cross section between the beam pipe and the outer limit of the MVD services is in the order of 56000 mm^2, to be shared between the DC-DC converter staves, the cooling pipes and the cables. Assuming that all the cooling pipes can stay within a 12 mm thick ring around the beam pipe, about 47000 mm^2 are left available. Within this section, the free areas are small and patchy: the largest are eight wedges located between two adjacent stave, each with an area of about 750 mm^2. All together, this areas could accommodate all the through cables (section A2); however the many LV cables composing

the A1 section, which amounts to almost 17000 mm^2 without considering the space needed for the bending and the connections, have still to be placed and the remaining free space (around 10000 mm^2) is largely insufficient for them. Possible solutions include the use of thinner cables for the power supply of the DC-DC converters and the relocation of some DC-DC boards further away, e.g. in the patch panels, as well as a redefinition of the volumes dedicated to the services of the various detectors. These solutions must be carefully evaluated against their consequences for the operation of the MVD and the possible interferences with other systems.

6

CONCLUSIONS

The research work presented in this thesis was conducted in the framework of the $\overline{\text{P}}$ANDA experiment, whose physics program and experimental setup have been introduced in chapter 1, and in particular within the group developing the Micro Vertex Detector, which is described in chapter 2.

At the core of this thesis is the design and development of the strip detector; as such, this document represents a natural continuation of the work presented in the PhD theses of Thomas Würschig and Hans-Georg Zaunick [93, 100]. With respect to these previous works, however, the focus here is on a comprehensive view towards the realization of an integrated detector, rather than on the detailed investigation of individual components.

An initial description of the barrel staves is provided in chapter 3, explaining the concept of the detector modules and presenting the active components (i.e., the sensors and the two different readout chips), with a special focus on those properties that have an impact on how the components relate to each other and to the rest of the detector at large. The chief concerns are therefore the geometry of the components, the pad location and their requirements in terms of input/output and power supply lines; equally important is also the electrical power consumption, which has major consequences in the design of the powering and of the cooling systems. The second half of chapter 3 is devoted to the mechanical hybrid support of the individual barrel staves, the support of the barrel as a whole and its integration into the rest of the MVD. The design of the carbon fiber staves, the choice of the materials and some peculiar characteristics are described there.

The electrical characterization of the sensors, initiated in previous works with the studies of the punch-through biased sensors, has been extended to include the first samples with a polysilicon resistor biasing scheme. Samples from the second prototype run, fabricated in 2013, have been characterized with the experimental setup at the probe station and have provided reliable results in agreement with the predictions and with the samples from the first prototype runs. The radiation hardness of the new samples has been studied with proton irradiations at the Bonn cyclotron; as for the electrical characterization, the results do not differ significantly from those obtained in the previous batches.

Because of the similarities in the results between the two prototype runs, the performed studies do not provide a clear indication about which technology should be selected for the production of the final sensors. However, the noise analysis of the punch-through sensors published in [100] yields unacceptably high noise figures towards the end of the $\overline{\text{P}}$ANDA lifetime, compromising the minimum accepted signal to noise ratio. For this reason, the biasing technique based on the polysilicon resistors

has been chosen for all the future sensor productions. A first production-grade set of sensors has been produced in 2015 and selected measurements have been presented.

Besides the active sensitive components, the barrel staves consist of several additional elements which are crucial for the correct detector operation. These elements are the focus of the last chapter of this thesis and include the Flexible Printed Circuit (FPC) to connect the readout electronics and the sensor, the carbon fiber stave with the integrated cooling system and the powering and cabling apparatus, to provide both power supply and data connection.

A careful evaluation of the requirements of the FPC has been carried out, including the geometrical constraints, the layout of the power and data lines, the positioning of the chips and the choice of the fabrication materials. A first set of prototypes has been designed, produced and successfully tested. The layouts implemented included twelve different pitch adapters, three flexible flat cables and four one-chip carrier boards designed for different chips and data connectors. The tests of the prototypes have provided helpful insights to identify several layout issues, as well as allowing to compare three different layer stackups and to demonstrate the feasibility of manufacturing solutions such as the laser microvias.

The validation of the stave cooling system included two different studies. The pressure drop along the cooling lines as a function of the water volume flow was evaluated in order to determine the maximum flow allowed while preserving the underpressure operation of the circuit. Secondly, two stave prototypes equipped with resistors as heating elements have been built and used to study the maximum temperatures reached by the various elements of the stave; the influence of the water flow, of the presence of the FPC and of the environment temperature have all been studied. The tests showed strong temperature variations among the heating elements, which have been tracked to an uneven profile of the glue layer between the resistors and the stave, as well as to variations among the resistors. The temperature of the other elements on the stave (i.e., the carbon fiber stave itself and the sensor) is essentially decoupled from that of the heating elements and follows the environment temperature. The efficiency of the cooling system has been evaluated to be always above 90% and, for certain experimental conditions, significantly above 100% (i.e., not only the resistors but also the surronding air is cooled down by the water). When the efficiency is below 1, the heat that is not removed from the resistors contributes to a slight warming of the surrounding air until an equilibrium point is reached. The system has therefore proved to be able to maintain the temperatures on the stave at operationally acceptable levels.

For its operation, the MVD requires a complex powering system. The requirements for the power and data cables and the layout of possible routing paths in the crowded volumes immediately around the MVD have been evaluated extensively. The study, which included not only the cabling of the strip barrels but that of the entire MVD, highlighted a number of critical regions where the available space is, in the current layout, either extremely tight or largely insufficient to accommodate all the needed cables. Further design iterations at the level of the entire MVD will be therefore required in order to be able to provide power and data connections to all the MVD elements; this optimization may require major changes in the way the detector is powered and in how the available space is shared among different detectors.

Appendices

A

RADIATION HARDNESS STUDIES OF EPITAXIAL DIODES

In order to test the radiation hardness of the strip sensors, the experimental setup at the Bonn cyclotron described in section 4.1.2 has been developed. This setup offered the possibility to perform tests on additional structures, among which two series of epitaxial diodes for the pixel detector of the MVD. The studies on these diodes and their relevance on the performance of the MVD are presented in this appendix.

A.1 Experimental Setup

The irradiations were performed at the Bonn cyclotron, using the setup described in section 4.1.2. The neutron equivalent fluence, measured in $n_{1MeV\,eq}\,cm^{-2}$, is calculated from the proton fluence measured by the Faraday cup and is given by the equations 4.1 and 4.2.

For what concerns the setup used to measure the parameters of the diodes, they are connected with a four-needles scheme on a probe station, as shown in figure A.1. A PC-controlled LCR meter is used to measure the capacitance between the two diode electrodes, while a high voltage power supply provides the biasing to the diode and measures its leakage current. An intermediate biasing box is used to decouple the inputs of the LCR meter from the high voltage.

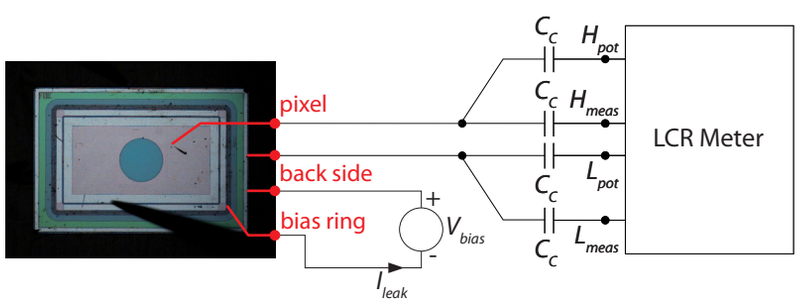


Figure A.1: Diodes connection scheme. Two needles connected to the power supply provide the biasing to the diode, while the capacitance measurement is performed with the LCR meter through another pair of needles. A bias box with four carefully matched capacitors decouples the inputs of the LCR meter from the high voltage.

A.2 BATCH 1

In the first series of tests, eight diodes from four different wafers were available. The properties of the diodes are summarized in table A.1. The diodes feature an epitaxial layer grown on a low resistivity Czochralski substrate; the wafers differ in the thickness and in the resistivity of the epitaxial layer. Additionally, the wafers n. 2 and 4 were subject to an additional oxygenation process for 12 hours in O_2 atmosphere at 1150°C and for $\sim$ 53 hours in N_2 atmosphere at 1150°C [66]. The wafer substrate and the epitaxial layer were manufactured at ITME, Warsaw; the diode production and the oxygenation were performed at FBK, Trento.

Diode general properties	
Substrate thickness	(525 ± 25) μm
Wafer diameter	(100 ± 0.5) mm
Substrate resistivity	$(0.008 - 0.02)\ \Omega \cdot$cm
Orientation	$< 100 >$
Conductivity type/dopant (substrate)	n+/Sb
Conductivity type/dopant (epitaxial layer)	n/P
Diode size	3×5 mm^2

Epitaxial layer properties		
	Wafers 2 and 14	**Wafers 4 and 15**
Thickness	$(99.34 - 100.38)$ μm	$(149.70 - 151.27)$ μm
Resistivity	$3610\ \Omega \cdot$cm	$3945\ \Omega \cdot$cm

Table A.1: Batch 1 diodes: general properties of the batch and of the epitaxial layers on the individual wafers. The oxygenation process was performed on wafers n. 2 and 4.

The diodes were irradiated with a beam of 13.510 MeV protons (corresponding hardness K factor 3.1), approximately square with an area of $(13 \pm 2) \times (13 \pm 2)$ mm^2. Each diode was irradiated indipendently, applying two different fluences:

- low fluence: measured cup charge $(13 \pm 1) \cdot 10^{-7}$ C, equivalent neutron fluence $(1.5 \pm 0.3) \cdot 10^{13}$ $n_{1MeV\,eq}\,cm^{-2}$;
- high fluence: measured cup charge $(131 \pm 1) \cdot 10^{-7}$ C, equivalent neutron fluence $(1.5 \pm 0.3) \cdot 10^{14}$ $n_{1MeV\,eq}\,cm^{-2}$;

with four diodes (one from each wafer) being irradiated with each fluence.

For each diode, C-V and I-V curves were measured and used to determine the full depletion voltage and the leakage current, respectively. The depletion voltage was calculated by performing a double linear fit on the C-V curve and by finding the intersection of the two lines. An example of a curve and of the fits performed on it is shown in figure A.2.

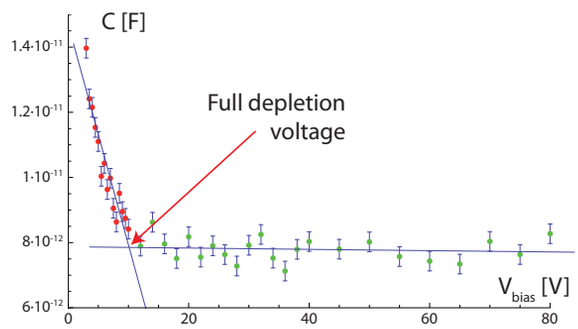


Figure A.2: Batch 1 diodes: determination of the full depletion voltage from the C-V curve of a non irradiated diode. The data points used for the two linear fits are represented in red and green, respectively.

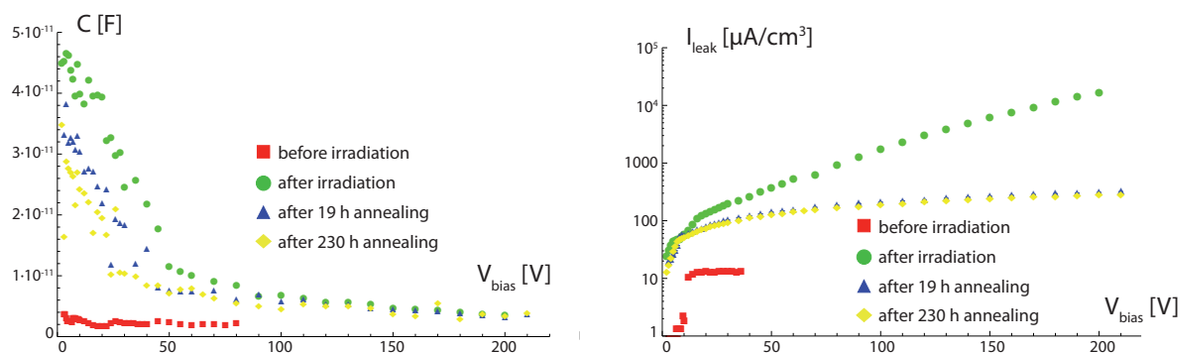


Figure A.3: Batch 1 diodes: comparison of the C-V (*left*) and I-V (*right*) curves of the same diode (w4_1) before and after the irradiation. A partial recovery can be observed after a thermal annealing phase. The leakage current is normalized to the volume of the epitaxial layer and is therefore expressed in $\mu A/cm^3$.

The choice of the data points included in the two fits is sometimes not unambiguous and is a source of uncertainty much larger than the calculated uncertainty on the fit parameters. Therefore, the fits were performed several times changing the range of data points included and reporting the average and the standard deviation of the obtained fit parameters.

The curves were measured before the irradiation, immediately after it and after two thermal annealing phases at 60°C, of $\sim$ 19 and $\sim$ 230 hours. A comparison of the I-V and C-V curves during the various phases of the measurement can be seen in figure A.3.

The initial values are reported in table A.2. No significant differences were observed among different diodes from the same wafer. Diodes with a thicker epitaxial layer consistently exhibit a slightly higher depletion voltage and a lower capacitance, in agreement with the expectations.

Wafer	Type	V_{dep} [V]	C [pF]	I_{leak} [nA]
w14	100 μm	11 ± 5	4.3 ± 0.5	< 1
w2	100 μm, ox.	9 ± 2	5.2 ± 0.5	$3 - 7$
w15	150 μm	13 ± 4	2.1 ± 0.5	< 1
w4	150 μm, ox.	15 ± 5	2.1 ± 0.5	$25 - 65$

Table A.2: Batch 1 diodes: initial values of the depletion voltage V_{dep}, of the capacitance C and of the leakage current I_{leak} (typical values for diodes from one wafer). The capacitance and the leakage current are measured at the depletion voltage.

The values of the full depletion voltage and of the leakage current at the various stages of the irradiation and annealing process are presented in figure A.4.

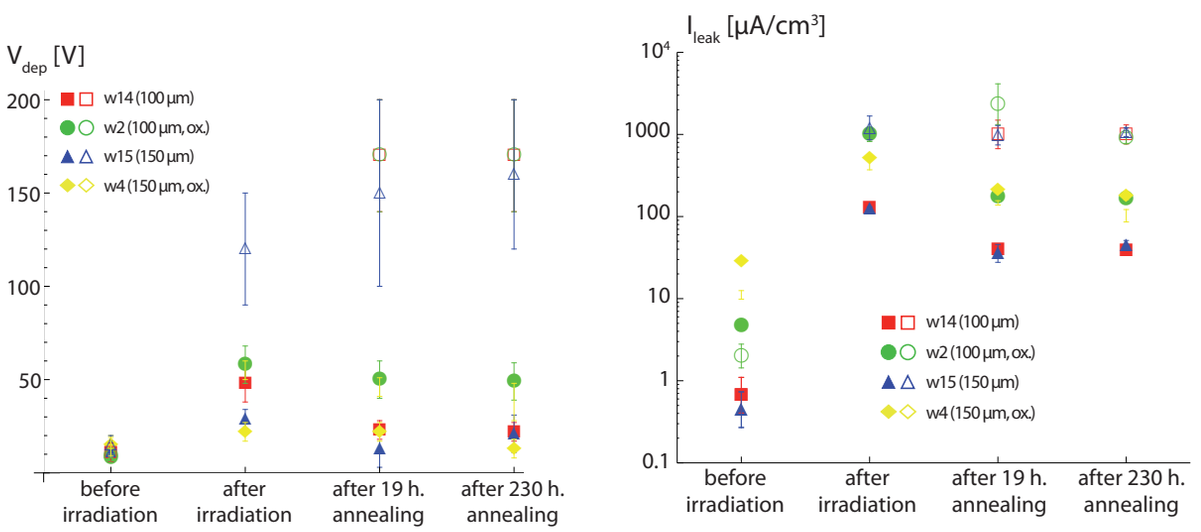


Figure A.4: Batch 1 diodes: behavior of the full depletion voltage (*left*) and of the leakage current (*right*) after the irradiation and after the annealing phases. Filled and empty markers represent low and high fluences, respectively. The leakage current is measured at the depletion voltage. The 100 μm diodes cannot be fully depleted after the high-fluence irradiation. The depletion can be achieved again after the first annealing phase, although at a very high voltage. The high-fluence 150 μm oxigenated sample (w4_1) exhibits values of the full depletion voltage and of the current similar to those of the low-fluence samples, suggesting a poor alignment with the beam which resulted in a lower applied fluence.

The depletion voltage increases from starting values in the order of 10 V up to $20 - 50$ V for the low-fluence and to 100 V and above for the high-fluence case. A partial recovery, in the order of $10 - 20$ V, can be observed after the first annealing phase for the diodes exposed to the lower fluence. For the highly irradiated diodes the depletion voltage keeps increasing, although the degradation of the C-V

curves is such that it becomes very difficult to identify the point of full depletion. The 100 μm diodes exposed to the higher fluence can only be depleted after the first annealing, by applying a bias voltage in excess of 150 V. The depletion voltage after the second annealing phase is essentially stable on the values measured after the first annealing.

In addition to the full depletion voltage, the leakage current can be studied as well. Here a similar effect can be observed, with the current values increasing by $2-3$ orders of magnitude after the irradiation and a partial recovery after the annealing. The final values reached by the highly irradiated diodes after both annealing phases are approximately one order of magnitude greater than those of the diodes exposed to a lower fluence.

A.3 BATCH 2

For the second series of irradiations, diodes from two wafers with a lower resistivity and with a 100 μm epitaxial layer were selected [66, 152]. The properties of the diodes are summarized in table A.3; the only difference between the two wafers is the oxygenation process applied to wafer 2. In addition to the standard diodes, larger (5×5 mm^2) photodiodes from were also available on both wafers.

Property	**Wafer 2 (oxygenated)**	**Wafer 6 (non oxygenated)**
Diodes irradiated	$6+1$ photodiode	$5+1$ photodiode
Epitaxial layer thickness	100 μm	
Residual substrate thickness	~ 20 μm	
Diode size	3×5 mm^2	
Epitaxial layer resistivity	1550 Ω · cm	

Table A.3: Batch 2 diodes: diode properties.

To achieve a better control over the applied fluence, the irradiation procedure was different with respect to the first irradiation campaign. The diodes were collected in two groups, each containing two or three diodes from the same wafer and corresponding to a high fluence and a low fluence irradiation. The diodes in one group were then irradiated at the same time, thus limiting to two the number of irradiations needed and reducing the chance of misalignments between the various trials; a third irradiation with an intermediate fluence was performed with two photodiodes, one from each wafer. The fluences applied are the following:

- low fluence irradiation: measured cup charge $(13 \pm 1) \cdot 10^{-7}$ C, equivalent neutron fluence $(1.0 \pm 0.2) \cdot 10^{13}$ $n_{1MeV\,eq}\,cm^{-2}$;
- high fluence irradiation: measured cup charge $(132 \pm 1) \cdot 10^{-7}$ C, equivalent neutron fluence $(1.0 \pm 0.2) \cdot 10^{14}$ $n_{1MeV\,eq}\,cm^{-2}$;

- medium fluence irradiation: measured cup charge $(67 \pm 1) \cdot 10^{-7}$ C, equivalent neutron fluence $(5.0 \pm 0.9) \cdot 10^{13}$ $n_{1MeV\,eq}\,cm^{-2}$.

The beam spot was approximately square, with a size of $(16 \pm 2) \times (16 \pm 2)$ mm^2, with protons with an energy of 13.510 MeV (corresponding to a hardness K factor of 3.1).

The diodes were arranged in a checkerboard pattern, in order to counter the effect of beam non-uniformities by averaging the values of the different diodes. The arrangement of the diodes during the irradiations is shown in figure A.6.

The I-V and C-V curves were measured before the irradiation, immediately after it and after four thermal annealing phases at 60°C of 1, 3, 10 and 17 days. During the measurements, the temperature was kept constant between 21 and 22°C. Between the irradiation and the first measurement the diodes were refrigerated at a temperature of ~ 5°C. A comparison of the I-V curves during the various phases of the measurement for three selected diodes can be seen in figure A.5.

The leakage current increases significantly after the irradiation; the magnitude of the increase show a clear dependance on the applied fluence. A partial recovery is visible after the annealing phases.

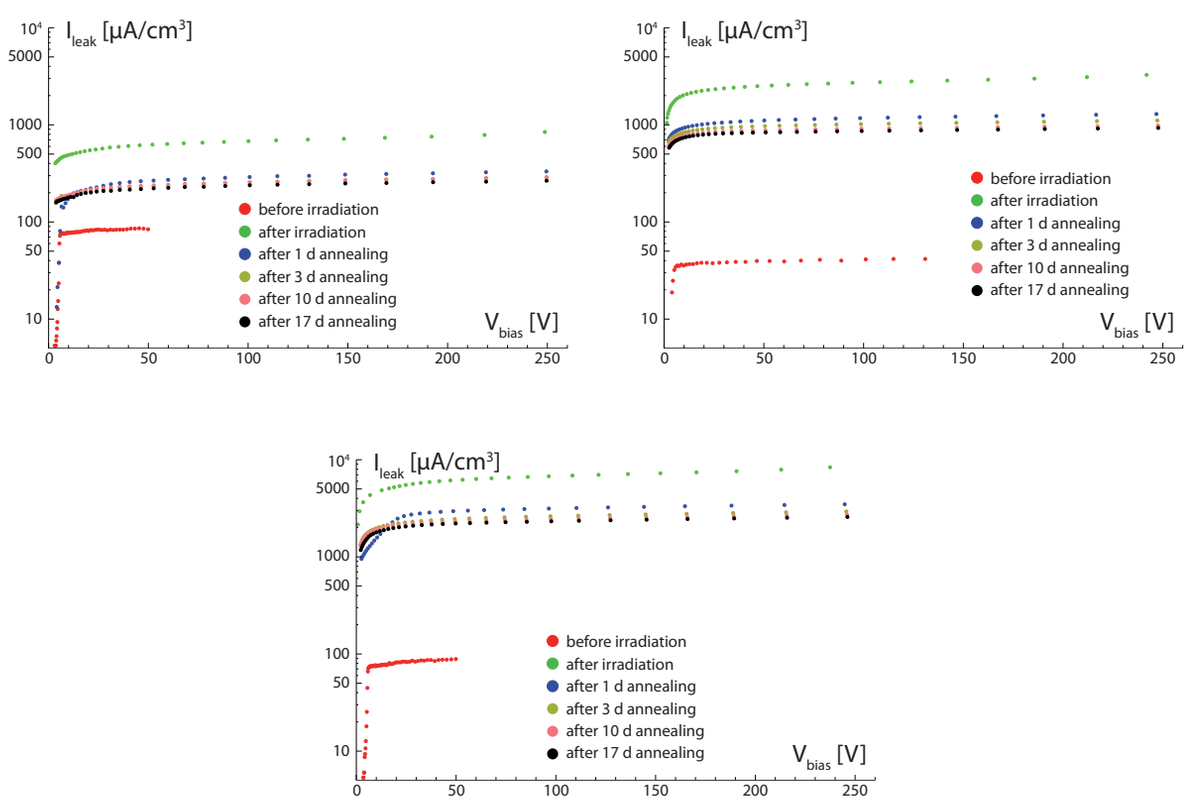


Figure A.5: Batch 2 diodes: comparison of the I-V curves of the same diode before and after the irradiation. *Top left:* low fluence oxigenated diode (w2_1); *top right:* middle fluence oxigenated diode (w2_ph); *bottom:* high fluence oxigenated diode (w2_4). The leakage current is normalized to the volume of the epitaxial layer. A partial recovery during the annealing can be observed on all diodes and its magnitude is approximately constant among them.

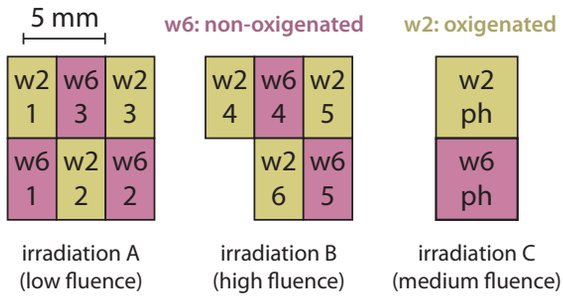


Figure A.6: Batch 2 diodes: arrangement of the diodes during the irradiations.

Table A.4 shows the values of the leakage current, measured at the full depletion voltage before and after the irradiation, for all the irradiated diodes. The measured increase of the leakage current and the applied fluence allow to calculate the current damage parameter α, defined as $\alpha = \Delta J / \Phi$, where ΔJ is the difference between the leakage current density post-irradiation values and the initial ones, measured in $\mu A/cm^3$, and Φ the equivalent neutron fluence, measured in $n_{1MeV\,eq}\,cm^{-2}$.

The obtained values of α, which are also reported in table A.4, vary significantly among the different diodes, with the most likely explanation being the lack of spatial uniformity of the beam profile. The evaluation of the fluence assumes a beam homogeneous throughout its spot area; this is in fact not true, although the experimental setup does not allow to determine the profile. However, it is possible

Diode	Fluence $[n_{1MeV\,eq}\,cm^{-2}]$	Initial I_{leak} $[\mu A/cm^3]$	Final I_{leak} $[\mu A/cm^3]$	ΔJ $[\mu A/cm^3]$	α [A/cm]
w2_1	$(1.0\pm0.2)\cdot10^{13}$	74.7 ± 1.3	514 ± 9	439 ± 9	$(4.4\pm0.9)\cdot10^{-17}$
w2_2	$(1.0\pm0.2)\cdot10^{13}$	59 ± 3	355 ± 9	297 ± 9	$(3.0\pm0.6)\cdot10^{-17}$
w2_3	$(1.0\pm0.2)\cdot10^{13}$	94.0 ± 0.7	359 ± 5	265 ± 5	$(2.6\pm0.5)\cdot10^{-17}$
w2_ph	$(5.0\pm0.9)\cdot10^{13}$	34.8 ± 0.8	1940 ± 60	1910 ± 60	$(3.8\pm0.7)\cdot10^{-17}$
w2_4	$(1.0\pm0.2)\cdot10^{14}$	72.7 ± 1.3	6060 ± 60	5990 ± 60	$(6.0\pm1.2)\cdot10^{-17}$
w2_5	$(1.0\pm0.2)\cdot10^{14}$	105 ± 3	2460 ± 13	2355 ± 14	$(2.4\pm0.5)\cdot10^{-17}$
w2_6	$(1.0\pm0.2)\cdot10^{14}$	79 ± 3	3124 ± 2	3045 ± 4	$(3.0\pm0.6)\cdot10^{-17}$
w6_1	$(1.0\pm0.2)\cdot10^{13}$	<1	283 ± 5	283 ± 5	$(2.8\pm0.6)\cdot10^{-17}$
w6_2	$(1.0\pm0.2)\cdot10^{13}$	<1	167 ± 3	167 ± 3	$(1.7\pm0.3)\cdot10^{-17}$
w6_3	$(1.0\pm0.2)\cdot10^{13}$	<1	635 ± 7	635 ± 7	$(6.3\pm1.3)\cdot10^{-17}$
w6_ph	$(5.0\pm0.9)\cdot10^{13}$	<1	2180 ± 60	2180 ± 60	$(4.4\pm0.8)\cdot10^{-17}$
w6_4	$(1.0\pm0.2)\cdot10^{14}$	<1	5200 ± 130	5200 ± 130	$(5.2\pm1.1)\cdot10^{-17}$
w6_5	$(1.0\pm0.2)\cdot10^{14}$	<1	1850 ± 70	1850 ± 70	$(1.9\pm0.4)\cdot10^{-17}$

Table A.4: Batch 2 diodes: leakage current I_{leak} before and after irradiation and current damage parameter α of all the irradiated diode.

to verify this hypothesis by looking at the α values of diodes placed in the same position in the two irradiations, as shown in figure A.7. The agreement between diodes irradiated in the same position is remarkably strong, thus supporting the fact that the discrepancies are due to a structure in the beam profile.

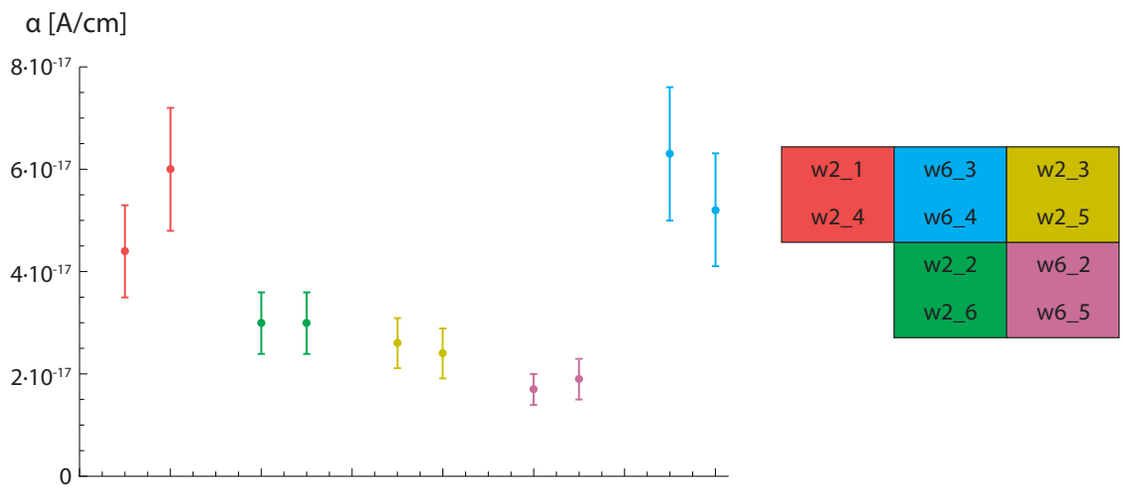


Figure A.7: Batch 2 diodes: current damage parameter α for pairs of diodes irradiated in the same location with different fluences. The color of the markers indicates the position of the pair of diodes referred to the map on the right hand side of the picture.

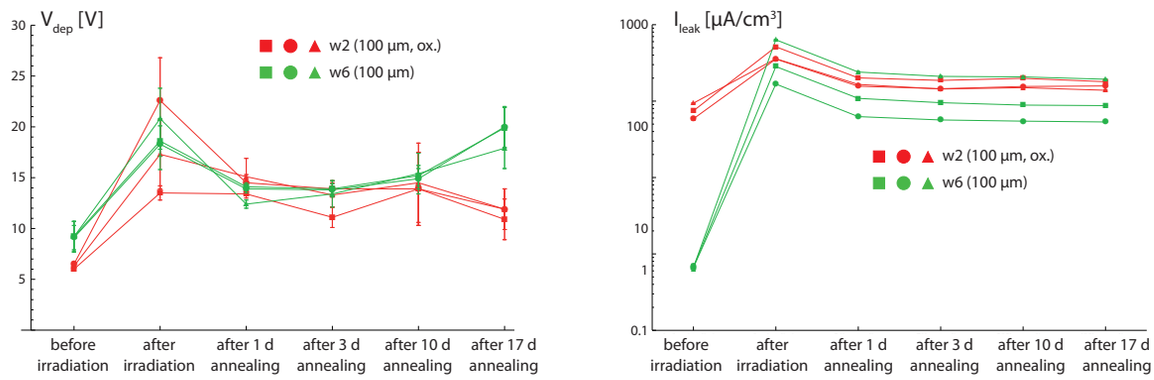
The values of the full depletion voltage and of the leakage current at the various stages of the irradiation and annealing process are presented in figure A.8.

The depletion voltage increases from starting values in the order of $5-10$ V up to $15-25$ V for the low-fluence and to $40-60$ V for the diodes irradiated with the high-fluence. Despite the simultaneous irradiation, diodes from the same group show significant differences in the values of the leakage current. This can be explained by a poor alignment with the beam, but also by the uneven beam profile. For what concerns the depletion voltage, large differences can be observed among the diodes in the high-fluence case; for the lower fluence, the differences are still present but are within the statistical fluctuations.

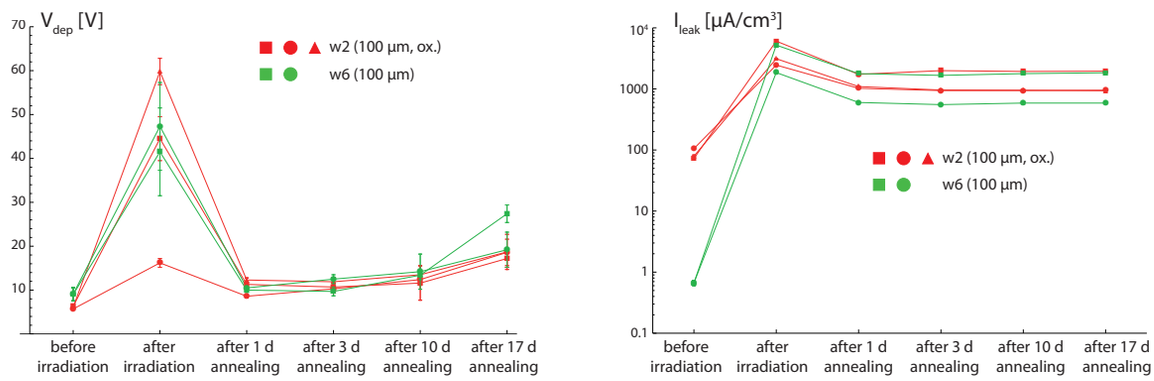
A significant recovery can be observed after the first annealing; this is especially evident in the leakage current plots and in the depletion voltage of the highly irradiated diodes. A slight increase of the depletion voltage can be seen on most diodes after the last annealing phases; the values of the leakage current are essentially stable.

In order to counter the differences among similar diodes, for each fluence an average of the values of the diodes coming from the same wafer was calculated. The results are presented in figure A.9, together with the mearurement of the photodiodes irradiated with the middle fluence.

With the exception of the pre-irradiation leakage current values, which are much lower on the diodes from the wafer 6, no significant differences can be observed between oxigenated and non-oxigenated diodes.



(a) Low fluence irradiation.



(b) High fluence irradiation.

Figure A.8: Batch 2 diodes: behavior of the full depletion voltage (*left*) and of the leakage current (*right*) after the irradiation and after the annealing phases. Red and green markers represent oxigenated and non-oxigenated diodes, respectively. The leakage current is measured at the depletion voltage. In the leakage current plots, a large difference between oxigenated and non-oxigenated diodes can be observed in the values before the irradiation; the difference however disappears after the irradiation and during the annealing. One of the diodes exposed to the higher fluence exhibits a low increase in the depletion voltage, which would suggest a lower effective applied fluence; however, the increase of the leakage current is comparable with that of the other high-fluence diodes.

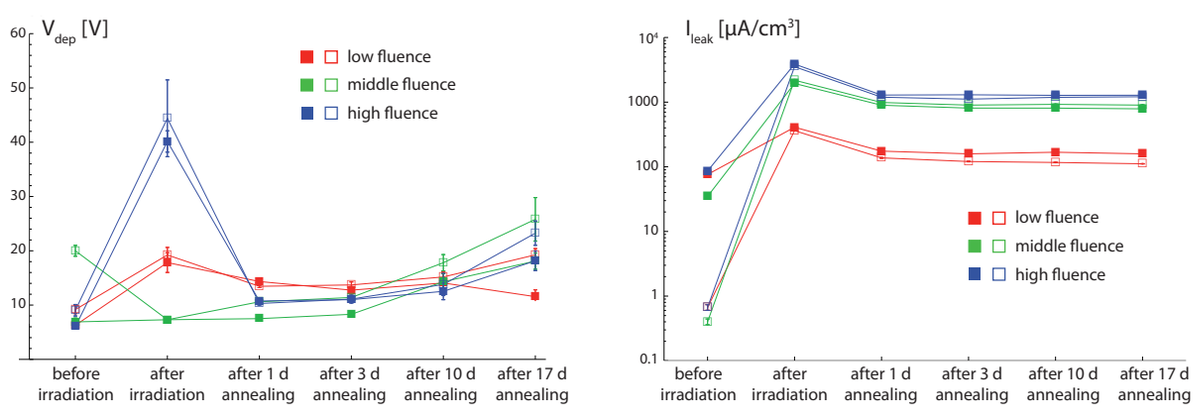


Figure A.9: Batch 2 diodes: comparison of the annealing behavior of the diodes exposed to different fluences. The points in the plot are the average of all the diodes from one wafer irradiated simultaneously with one fluence. Filled and empty markers represent oxigenated and non-oxigenated diodes, respectively; red, green and blue curves represent low, middle and high fluences, respectively.

B

BOARD DIAGRAMS

B.1 FLEXIBLE CHIP CARRIER BOARDS

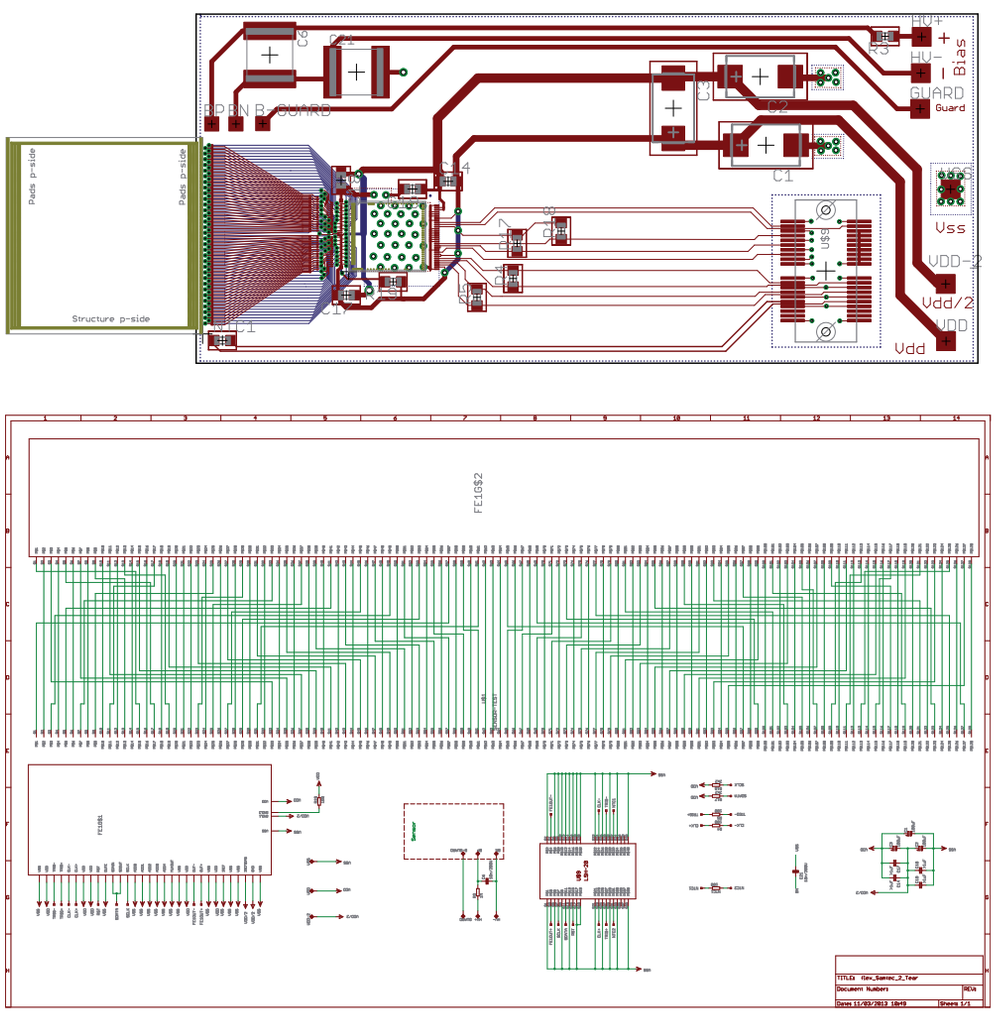


Figure B.1: *Top:* layout of the one-chip carrier board from the FPC Prototype v1; the board has a size of 82.9×37 mm^2. *Bottom:* schematic of the board.

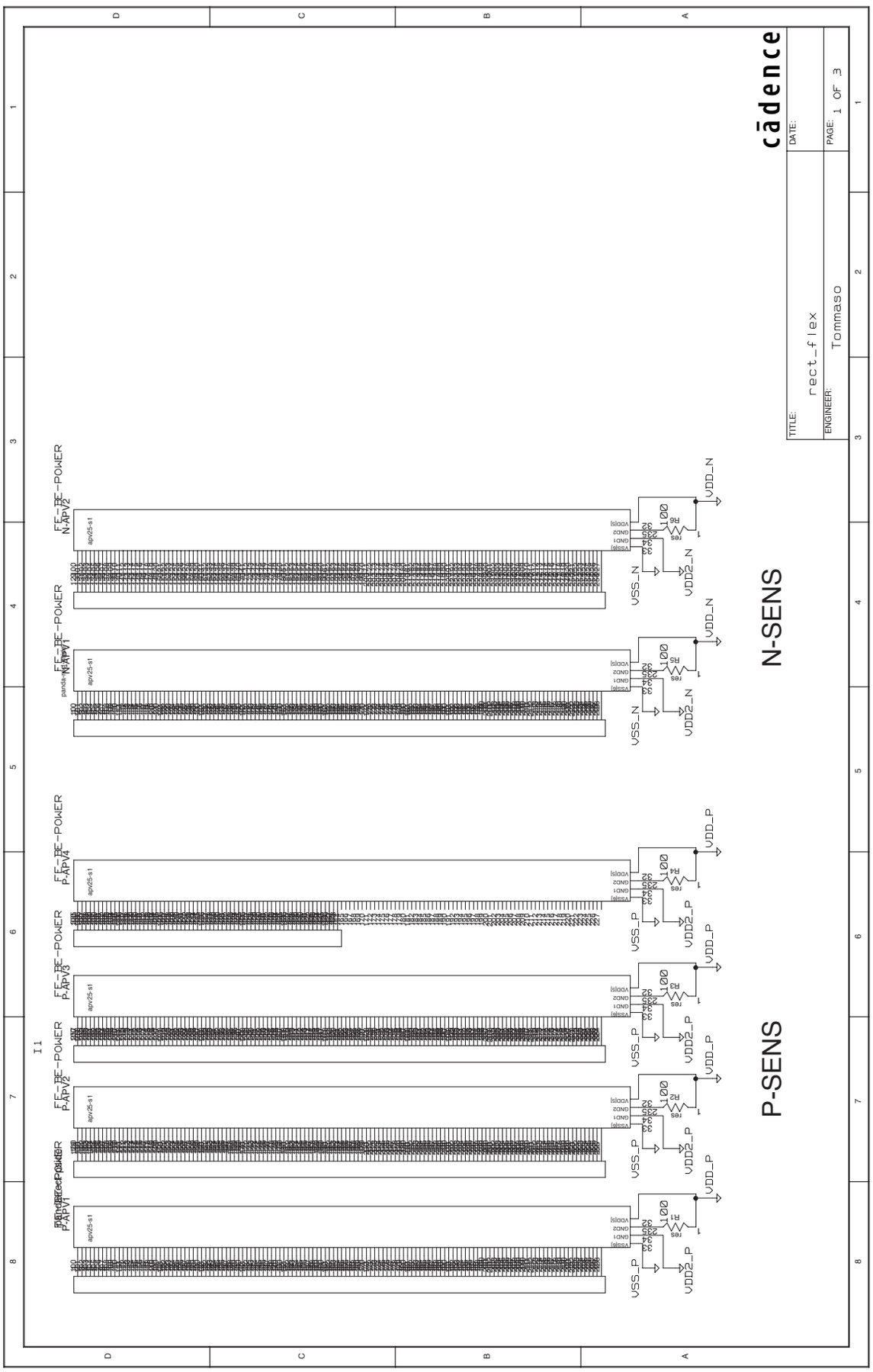


Figure B.2: FPC v2 chip carrier board schematic - page 1.

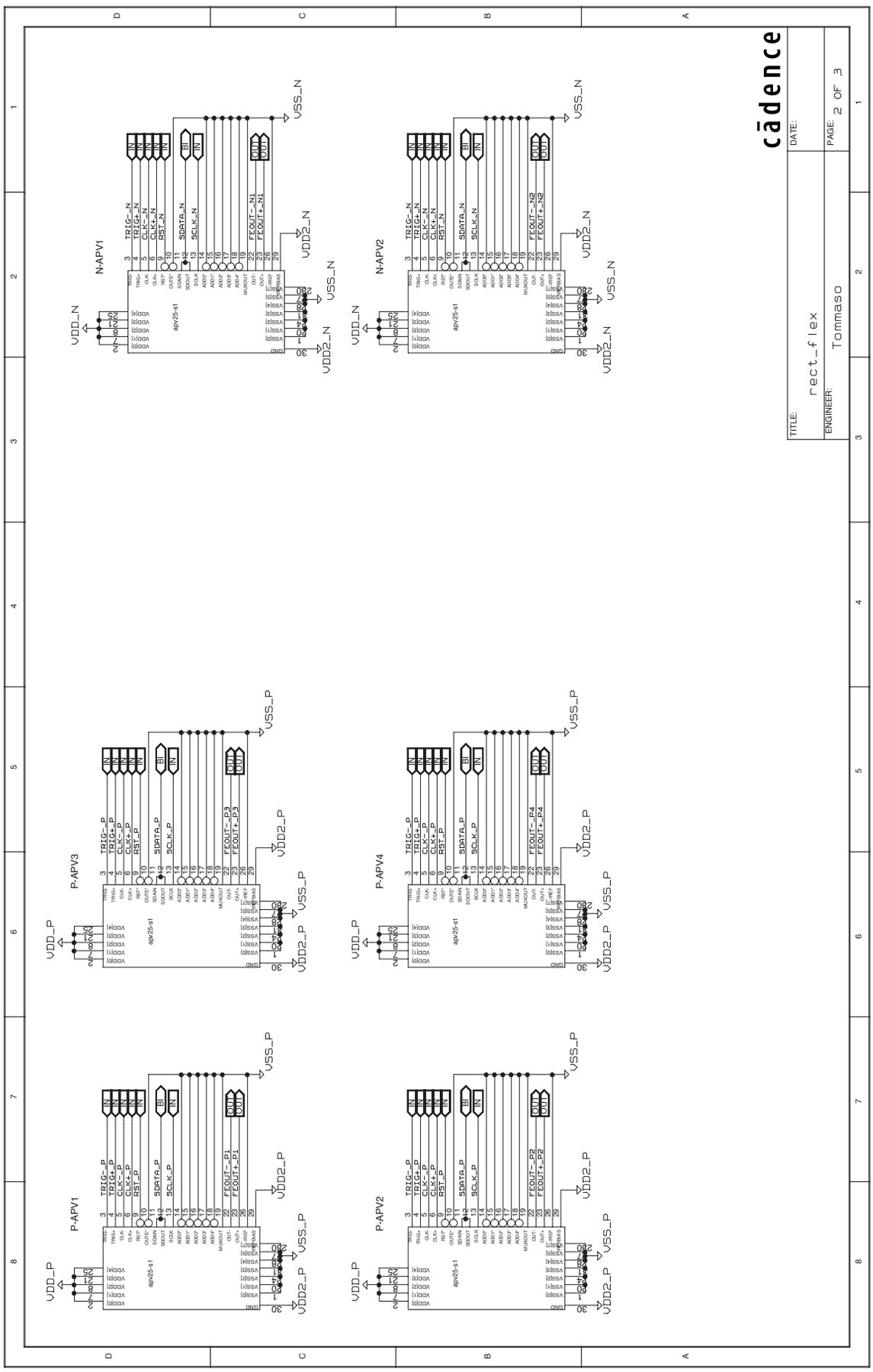


Figure B.3: FPC v2 chip carrier board schematic - page 2.

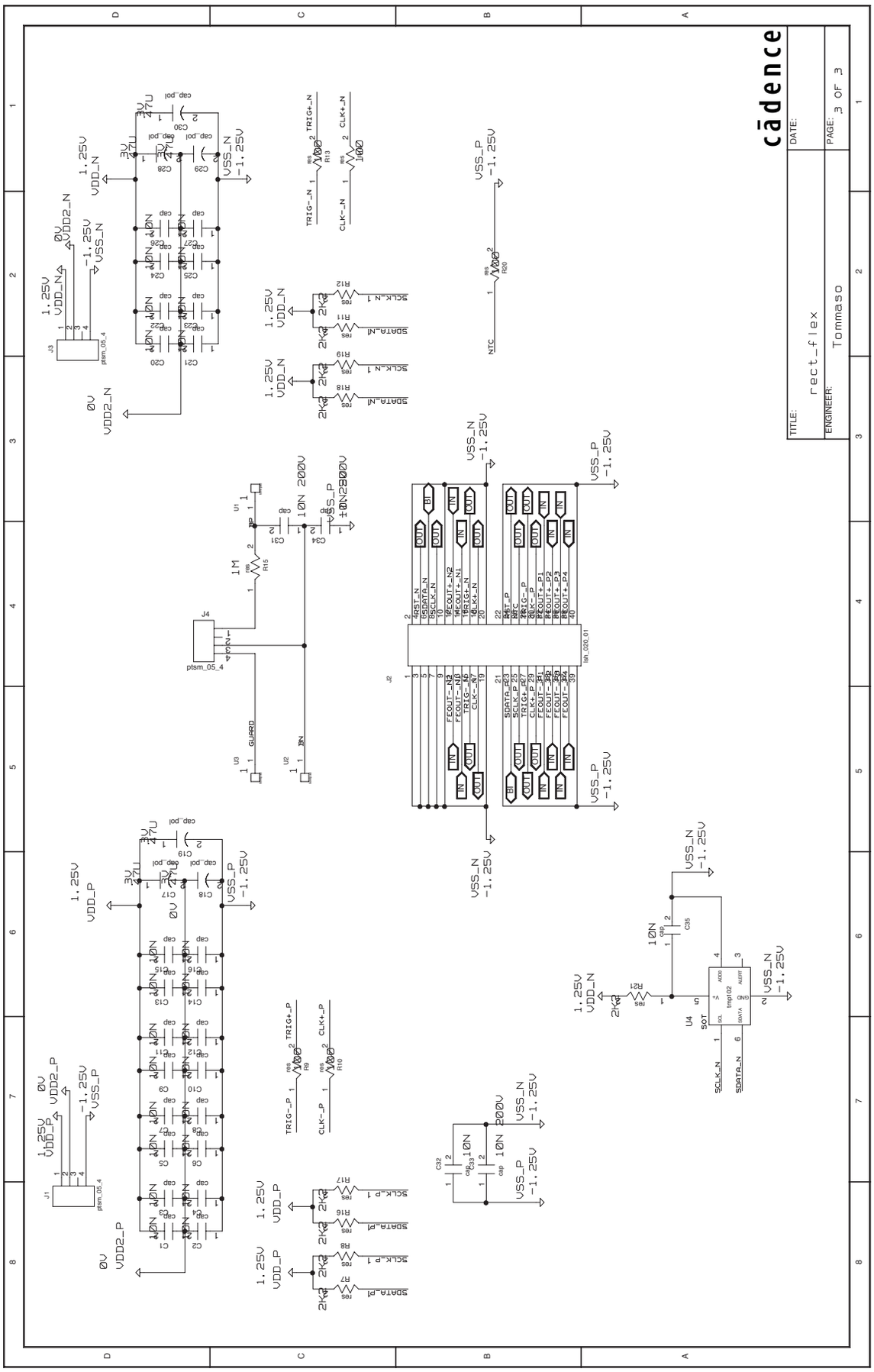


Figure B.4: FPC v2 chip carrier board schematic - page 3.

B.2 TRANSITION BOARDS

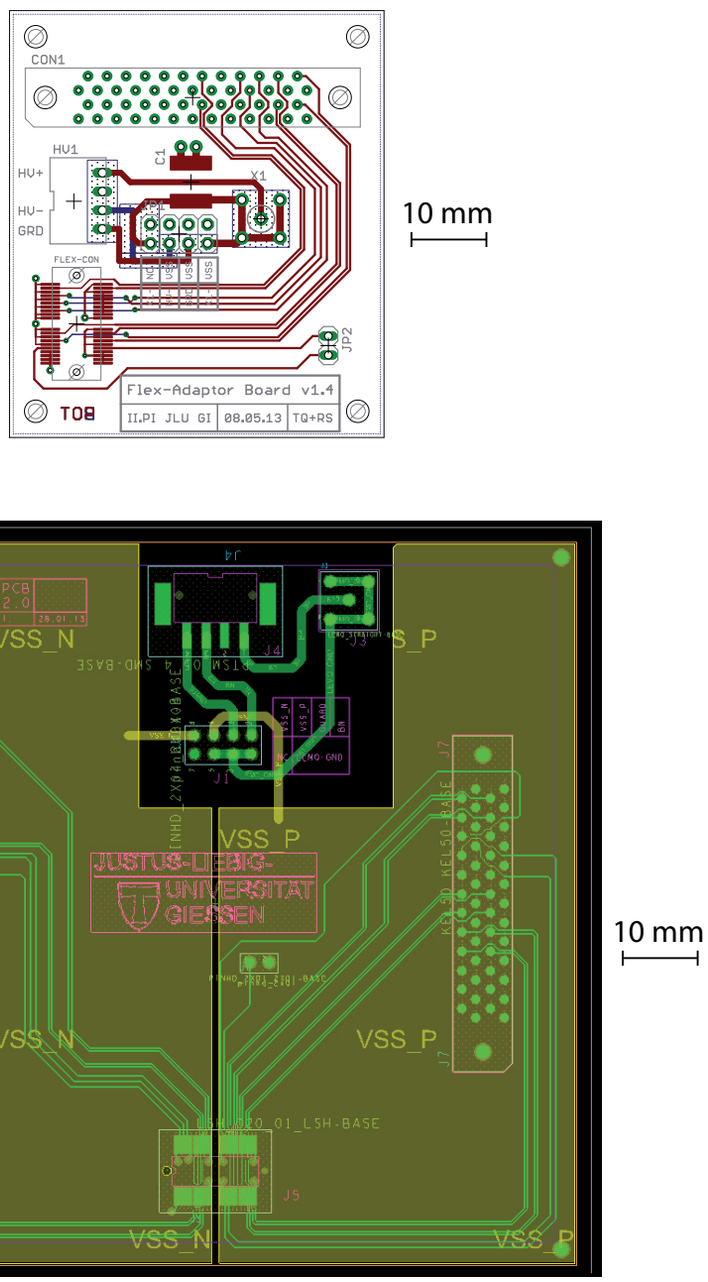


Figure B.5: Transition boards v1 (*top*) and v2 (*bottom*). The most recent version implements two independent ground planes VSS_P and VSS_N, represented in yellow, for the readout of the p- and of the n-side of the sensor. The two boards are drawn to scale and have a size of 50×57 mm^2 and 100×100 mm^2, respectively.

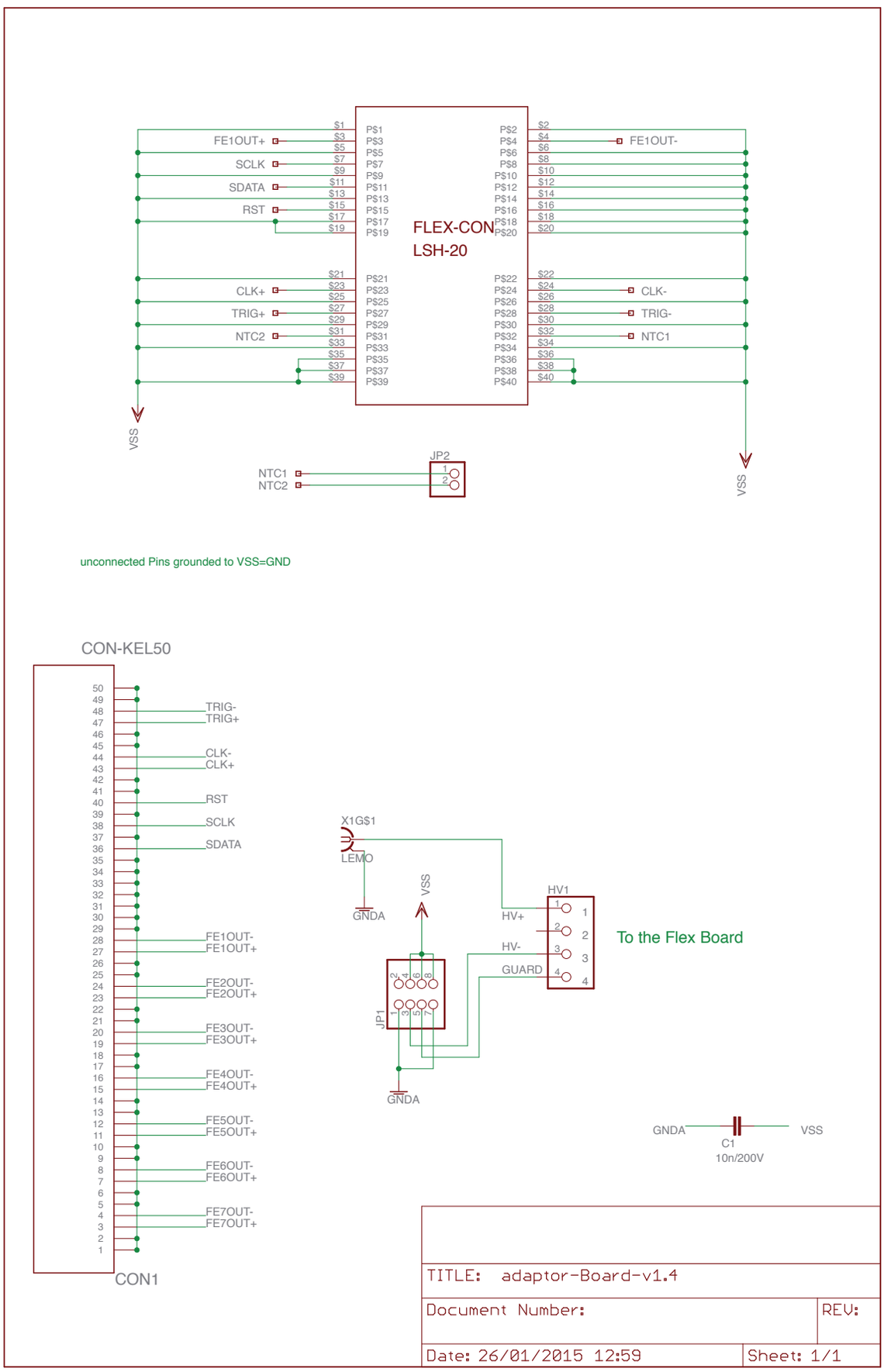


Figure B.6: Transition board v1 schematic.

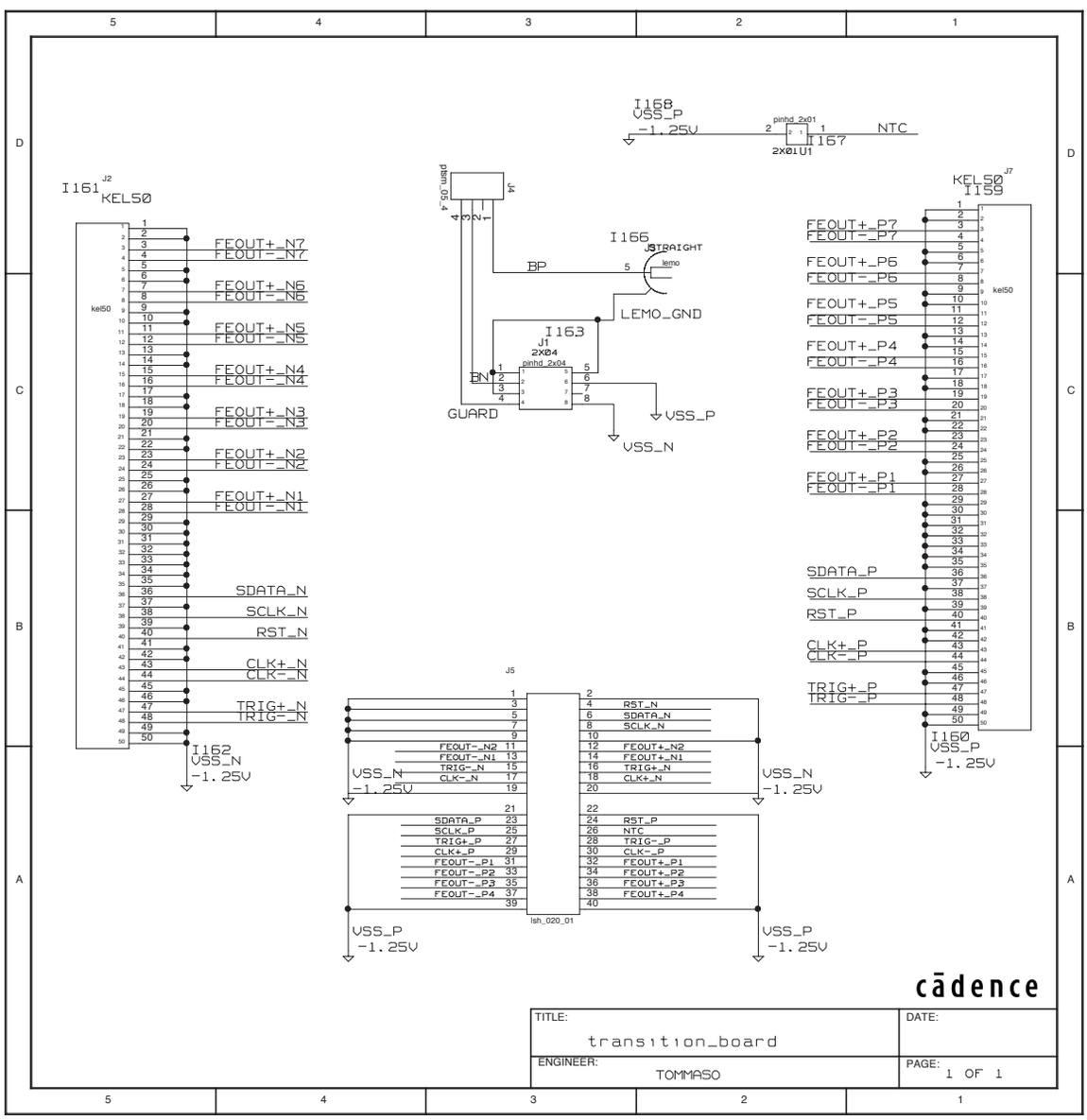


Figure B.7: Transition board v2 schematic.

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LIST OF ACRONYMS

1D	1-Dimensional
2D	2-Dimensional
3D	3-Dimensional
AC	Alternate Current
APPA	Atomic, Plasma Physics and Applications
APV	Analogue Pipeline Voltage mode
ASIC	Application Specific Integrated Circuit
BESIII	BEijing Spectrometer III
BNL	Brookhaven National Laboratory
BoPET	Biaxially-oriented PolyEthylene Terephthalate
CAD	Computer-Aided Design
CBM	Compressed Baryonic Matter
CCA	Copper-Clad Aluminum
CFRP	Carbon Fiber Reinforced Plastic
CMOS	Complementary Metal Oxide Semiconductor
CMS	Compact Muon Solenoid
COSY	COoler SYnchrotron
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapour Deposition
Cz	Czochralski
DC	Direct Current
DC-DC	DC-to-DC Converter
DIRC	Detector for Internally Reflected Cherenkov light

DPM	Dual Parton Model
DUT	Device Under Test
ED	ElectroDeposition
EMC	Electromagnetic Calorimeter
FAIR	Facility for Antiproton and Ion Research
FBK	Fondazione Bruno Kessler
FEM	Finite Element Method
FPC	Flexible Printed Circuit
FSSR2	Fermilab Silicon Strip Readout 2
FS	Forward Spectrometer
FZ	Floating Zone
GBLD	GigaBit Laser Driver
GBT	GigaBit
GBTX	GigaBit Transceiver
GEM	Gas Electron Multiplier
GPM	Generalized Parton Distribution
HESR	High Energy Storage Ring
HL	High Luminosity
HR	High Resolution
HV	High Voltage
HV-MAPS	High Voltage Monolithic Active Pixel Sensors
I^2C	Inter-Integrated Circuit
INFN	Istituto Nazionale di Fisica Nucleare
I/O	Input/Output
IP	Interaction Point
ITC	Istituto Trentino di Cultura
ITME	Institute of Electronic Materials Technology

LAAPD	Large Area Avalanche PhotoDiodes
LEAR	Low Energy Antiproton Ring
LHC	Large Hadron Collider
LINAC	LINear ACcelerator
LQCD	Lattice Quantum Chromo Dynamics
LV	Low Voltage
LVDS	Low-Voltage Differential Signaling
MCP PMT	Multi-Channel Plate PMT
MDC	Module Data Concentrator
MDT	Mini Drift Tubes
MVD	Micro Vertex Detector
MWPC	Multi Wire Proportional Chamber
NIEL	Non-Ionizing Energy Loss
NTC	Negative Temperature Coefficient
NUSTAR	NUclear STructure, Astrophysics and Reactions
PANDA	antiProton ANnihilation at DArmstadt
PASTA	PANDA STrip ASIC
PCB	Printed Circuit Board
PEEK	PolyEther Ether Ketone
PET	Positron Emission Tomography
PI	PolyImide
PMT	PhotoMultiplier Tube
PSL	Primary Supply Line
QCD	Quantum Chromo Dynamics
RESR	Recuperated Experimental Storage Ring
RICH	Ring Imaging Cherenkov Counter
SciTil	Scintillating Tiles

SiPM	Silicon PhotoMultipliers
SIS	SchwerIonen-Synchrotron
SLVS	Scalable Low Voltage Signaling
SMD	Surface Mount Device
STT	Straw Tube Tracker
TAC	Time To Analog
TCR	Temperature Coefficient of Resistance
TDC	Time To Digital
TID	Total Ionizing Dose
ToF	Time-of-Flight
TOFPET	Time-of-Flight PET
ToPix	Torino Pixel
ToT	Time-over-Threshold
TS	Target Spectrometer
UrQMD	Ultra-relativistic Quantum Molecular Dynamic
VL	Versatile Link
VTRx	Versatile TransReceiver
WASA	Wide Angle Shower Apparatus
WLS	Wavelength Shifting

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ERKLÄRUNG DER URHEBERSCHAFT

Ich erkläre: Ich habe die vorgelegte Dissertation selbständig und ohne unerlaubte fremde Hilfe und nur mit den Hilfen angefertigt, die ich in der Dissertation angegeben habe. Alle Textstellen, die wörtlich oder sinngemäß aus veröffentlichten Schriften entnommen sind, und alle Angaben, die auf mündlichen Auskünften beruhen, sind als solche kenntlich gemacht. Bei den von mir durchgeführten und in der Dissertation erwähnten Untersuchungen habe ich die Grundsätze guter wissenschaftlicher Praxis, wie sie in der "Satzung der Justus-Liebig-Universität Gießen zur Sicherung guter wissenschaftlicher Praxis" niedergelegt sind, eingehalten.

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