JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

A Time-Based Front-End ASIC for the Silicon Micro Strip Sensors of the $\bar{\text{P}}$ANDA Micro Vertex Detector

Dissertation
zur
Erlangung des Doktorgrades (Dr. rer. nat.)
der
Justus-Liebig-Universität Gießen
im
Fachbereich 07
Mathematik und Informatik, Physik, Geographie

vorgelegt von
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1. Gutachter: Prof. Dr. Kai-Thomas Brinkmann

2. Gutachter: Prof. Dr. Claudia Höhne

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Abstract

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A Time-Based Front-End ASIC for the Silicon Micro Strip Sensors of the $\bar{\text{P}}$ANDA Micro Vertex Detector

by Valentino DI PIETRO

Das $\bar{\text{P}}$ANDA-Experiment ist eines der Hauptexperimente an der geplanten Beschleunigeranlage FAIR (Facility for Antiproton and Ion Research), welche in Darmstadt errichtet wird. Mit dem Experiment soll die Erforschung der starken Wechselwirkung der Hadronenphysik mittels Antiproton-Proton Vernichtungsreaktionen ermöglicht werden. Der Antiprotonenstrahl mit Impulsen zwischen $1.5\,\mathrm{GeV/c}$ to $15\,\mathrm{GeV/c}$ erlaubt das Studium eines breiten Physikprogramms, inklusive Untersuchung von Hyperon, Open-Charm und exotischen hadronischen Kanälen.

Der Mikrovertex-Detektor (MVD) ist die dem Interaktionspunkt am nächsten gelegene Detektoreinheit des Experimentes. Er basiert auf Siliziumsensoren in Pixel und Streifengeometrien, die die Erkennung und Vermessung von primären und sekundären Spurvertizes ermöglichen.

Diese Arbeit beschreibt die grundlegenden Eigenschaften des $\bar{\text{P}}$ANDA Strip ASIC (PASTA), eines vollumfänglich für die Auslese der doppelseitigen $\bar{\text{P}}$ANDA-Streifensensoren entwickelten Chips. Die Architektur von PASTA wurde, im Sinne der Anforderungen an das Experiment, speziell für hohe Zeitauflösung und Ladungsmessung durch einen Zeit-Digitalen Ansatz entwickelt. Ein Zeit-Digitalwandler (TDC), ausgelegt auf eine Zeitbinbreite von $50\,\mathrm{ps}$, erfasst den Time-over-Threshold (ToT) des Sensorsignals nach Verstärkung durch einen dediziert für die Anwendung entwickelten Front-End-Verstärker. Insbesondere ist in der Arbeit die theoretische Vorarbeit und das Design des Chips dokumentiert, welche zu der finalen Implementierung führten sowie das Verhalten der Front-End-Stufe, welche mit professionellen Simulationstools charakterisiert wurde.

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The $\bar{\text{P}}$ANDA experiment is one of the main scientific pillars of the future Facility for Antiproton and Ion Research, currently under construction in Darmstadt, Germany. It will investigate hadron physics measuring antipron-proton annihilation reactions. The antiproton beam with momenta between $1.5\,\mathrm{GeV/c}$ to $15\,\mathrm{GeV/c}$, will allow to explore a broad physics program including hyperon, open-charm and exotic hadronic states.

The Micro Vertex Detector (MVD) is the innermost sub-detector of the tracking system of the $\bar{\text{P}}$ANDA experiment. It is based on silicon sensors with pixel and micro strip segmentation and its main task is the precise spatial identification and measurement of primary and secondary decay vertices.

This thesis describes the key features of the $\bar{\text{P}}$ANDA Strip ASIC (PASTA), a full-custom chip developed to read out the double-sided micro strip sensors of the MVD. PASTA aims at highly resolved time-stamping and charge information gathering through a time-digital approach. A Time to Digital Converter (TDC), allowing a time bin width down to $50\,\mathrm{ps}$, measures the Time over Threshold (ToT) of the sensor signals processed by a application specific, newly developed front-end amplifier. In particular, this thesis reports the theoretical studies yielding to the final implementation showing the performance of the front-end stage evaluated with professional simulation tools.

Acknowledgements

There are many people that I have to thank for the support provided during my PhD. First, my supervisor Kai-Thomas Brinkmann for his continuous help and willing to take care about any issue I had during these years. I also would like to thank the Helmholtz Graduate School for Hadron and Ion Research for FAIR and its management for making my PhD possible and offering a lot of interesting courses and workshops. Together with my main supervisor, I have to thank also my second and third HGS-HIRe tutors Angelo Rivetti and Tobias Stockmanns, respectively.

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But the biggest thank goes undoubtedly to my family. Without the gigantic support and the daily self confidence boost, especially in the toughest times, provided by my two amazing parents, I wouldn't be the person I am today and I couldn't have accomplished such an important achievement. Together with them, I owe a huge thank to my brother Alberto and my "sister" Laura for their presence in my life which is a true blessing. And last, but definitely not least, a special mention goes to a wonderful person who is already really important to me despite the relatively short time I've known her, she is my everything and without her my life wouldn't be the same, so thank you Eleonora.

Contents

Chapter 1

The $\bar{\text{P}}$ANDA Experiment

1.1 The FAIR Facility

The Facility for Antiproton and Ion Research (FAIR) is a new international accelerator facility under construction aiming at research with antiprotons and ions. It will be based upon an expansion of the GSI Helmholtz Centre for Heavy Ion Research situated in Darmstadt, Germany (see figure 1.1).

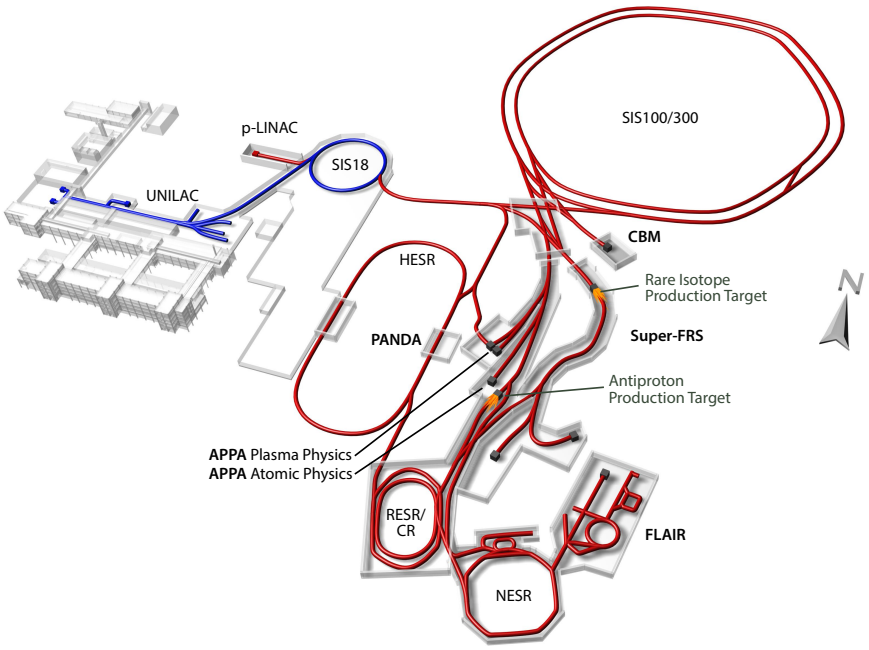


Figure 1.1: The future FAIR facility. Annotations for planned experiments are shown in bold characters together with highlights on the old (blue) and new (red) parts.

The core of this new multi-purpose accelerator facility will be the SIS100, a superconductive synchrotron ring with a circumference of $1100\,\mathrm{m}$ associated with a complex system of cooler and storage rings and experimental setups. Here, the proton beam coming from an upgraded version of the already existing SIS18 will be further accelerated up to an energy of $4\,\mathrm{GeV}$ and bunched in groups of about 2×10^{13} protons impinging on the antiproton production target. The generated antiproton beam will be then cooled down and injected in the Collector Ring (CR) before going through the High Energy Storage Ring (HESR) where the $\bar{\text{P}}$ANDA (Antiproton Annihilation

at Darmstadt) experiment will be located. The antiproton beam delivered to the experiment will have momenta in the range 1.5–$15\,\mathrm{GeV/c}$ and a maximum luminosity of $2 \times 10^{32}\,\mathrm{cm^{-2}\,s^{-1}}$. Together with PANDA, there are three more scientific pillars [1]: APPA (Atomic, Plasma Physics and Applications), CBM (Compressed Baryonic Matter), and NUSTAR (Nuclear Structure, Astrophysics and Reactions).

1.2 Physics of PANDA

PANDA is a fixed target experiment using high resolution antiproton beams. Its main goal is to investigate low energy Quantum Chromodynamics (QCD) where perturbation calculations cannot be applied. The momentum range of 1.5–$15\,\mathrm{GeV/c}$ is chosen to produce states in the overlap of perturbative and non-perturbative regimes at the intermediate energies of the beams ($\sqrt{s} = 2.25$–$5.47\,\mathrm{GeV}$). The PANDA physics program foresees four main pillars:

- hadron spectroscopy
- hadrons in nuclei
- nucleon structure
- hypernuclear physics

An overview of the potential physics program that PANDA aims at investigating is presented in figure 1.2.

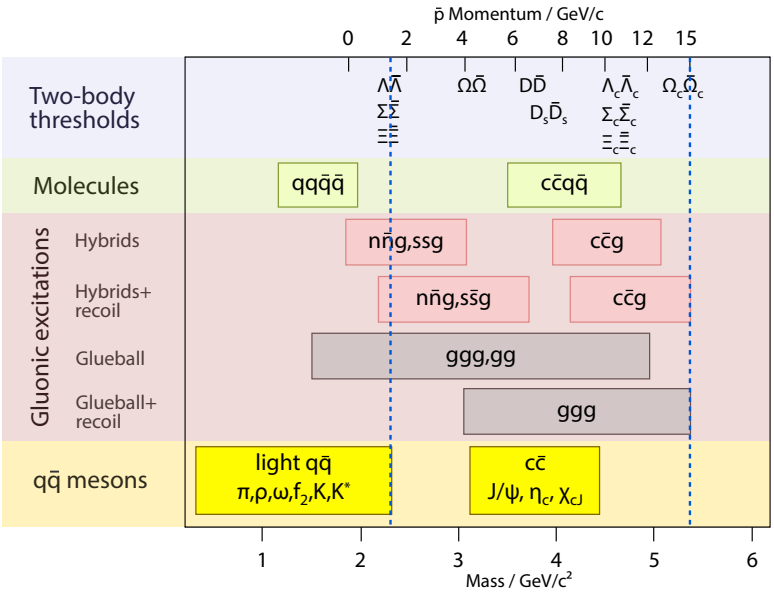


Figure 1.2: The physics spectrum available to HESR and within the blue dashed lines to PANDA. The antiproton beam momentum is given on the top axis, the according center of mass energies on the bottom axis. Image from [2].

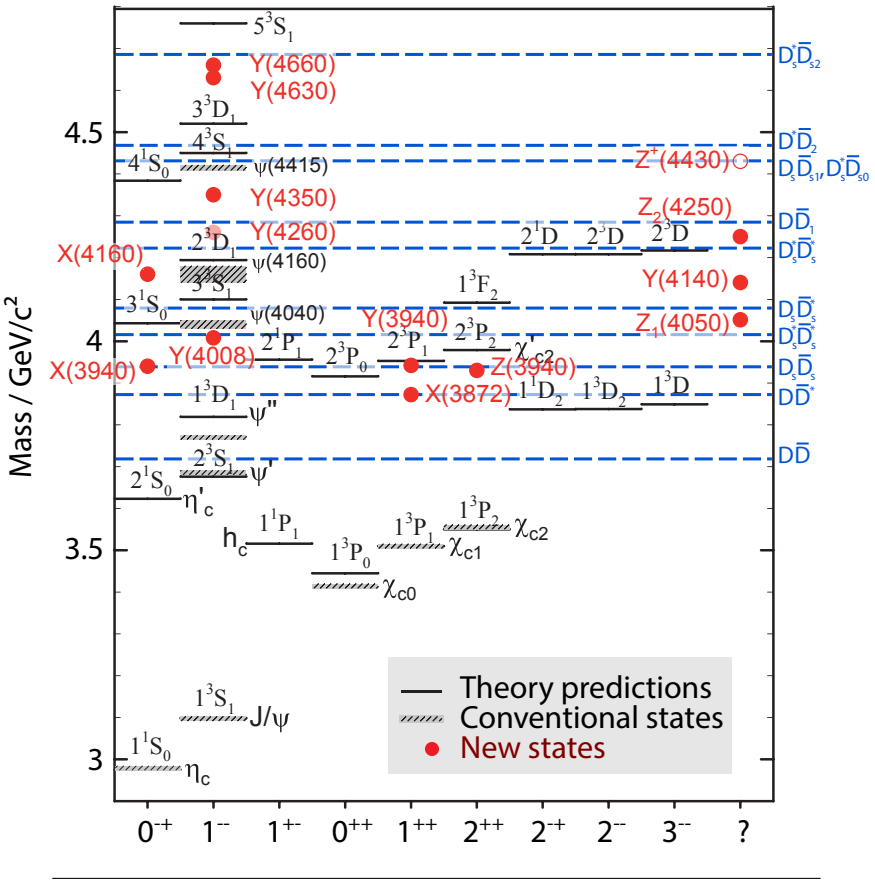


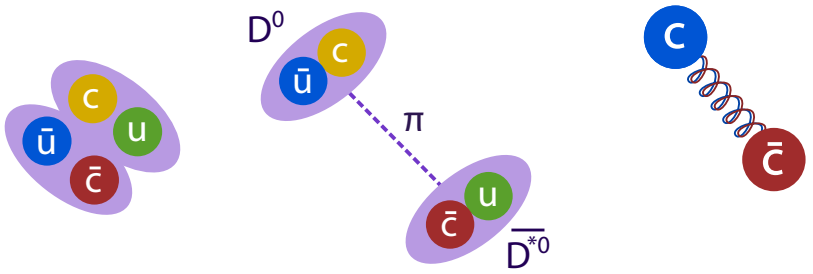
Figure 1.3: The charmonium spectrum with predicted (black solid lines) and measured states. The latter are given either as shaded black lines or red dots for conventional states and recently found XYZ states, respectively. The decay thresholds for D meson pairs are shown as blue dashed lines. Image from [2].

1.2.1 Hadron Spectroscopy

1.2.1.1 Charmonium Spectroscopy

In particle physics, the term quarkonium indicates a flavourless meson composed by a quark and its own antiquark. Thus, the term *charmonium* refers to a bound system of charm quark-antiquark. Despite the first excited charmonium (J/ψ) was detected in 1974 by two independent experiments at Stanford Linear Accelerator Center (SLAC) [3] and Brookhaven National Laboratory (BNL) [4], several open questions still need an answer and $\bar{P}$ANDA will try to succeed in this task. The charmonium spectrum is surprisingly similar to the one of the positronium (a e^+e^- bound state), thus the idea of describing the role of the charmonium in the strong interaction in the same way of the positronium in the electroweak theory was explored. However, this rough approximation cannot explain the charmonium spectrum (see figure 1.3) which has grown during the years by high-energy physics experiments.

Many states in disagreement with theoretical predictions have been observed and vice versa [5]. The majority of well established states lie below the $D\overline{D}$ threshold (also known as open charm threshold with a value of 3.73 GeV) [6]. Above the open charm threshold the opposite situation is true, many resonances have been recently found at the B-factories [7] whose



(a) Tetraquark (b) Quark molecule (c) Hybrid meson

Figure 1.4: Possible explanations of hadronic states not predicted by the common quark models of mesons and baryons. The first two use more than three quarks while the last includes gluonic excitations. Images from [2].

explanation is not univocal. A good example of this is the X(3872) first measured by Belle [8] and confirmed by other experiments [9-11] which doesn't fit any theoretical prediction. Such an exotic behaviour in terms of quantum numbers assignment, charge or decay modes, can be observed in other particles labelled as X, Y, or Z indicating that the model is still to be understood. Several interpretations have been considered (see figure 1.4):

- tetraquark: meson composed of four valence quarks
- quark molecule: two charged mesons weakly bound by the exchange of a gluon or of a pion
- hybrid meson: states carrying gluonic degrees of freedom

A strong candidate for the tetraquark interpretation is the $X_c(3900)$ as recently observed by BESIII [12] and Belle [13], while the above mentioned X(3872) could be explained through a molecular or tetraquark model.

1.2.1.2 Charmed and Strange Baryons Spectroscopy

Besides meson spectroscopy, the understanding of the excited spectrum of baryon is an important goal of $\bar{P}$ANDA. In fact, thanks to its tracking detectors and particle identification, the experiment aims at giving a strong contribution to the spectroscopy of charmed and strange baryons. In HESR's high luminosity mode, the high production rates of final state baryons is facilitate by the $\bar{p}p$ annihilation allowing a direct production of hyperon pairs avoiding the intermediate step of creating D or K mesons. Moreover, the decays of $\bar{p}p$ into $\Omega\bar{\Omega}$, $\Lambda_c\bar{\Lambda}_c$ or $\Sigma_c\bar{\Sigma}_c$ could be measured for the first time allowing the understanding of their formation cross section [14]. Because of baryons short lifetimes, the reconstruction of their decay patterns is mandatory to detect them. Therefore, an important requirement for such a spectroscopy is a tracking system able to identify displaced secondary vertices.

1.2.2 Hadrons in Nuclei

The properties of hadrons in nuclear matter are affected by the surrounding interactions. When hadrons are produced in a medium, a modification of the chiral symmetry breaking pattern of QCD due to finite density produces two main effects: a mass shift and a splitting of meson-antimeson masses (see figure 1.5) [15,16]. This phenomenon has been widely investigated by many experiments exploiting different kind of colliding particles, but $\bar{P}$ANDA will be the first to use $\bar{p}p$ annihilations allowing the study of this topic also for charmed hadrons through a low momenta nuclear environment where these effects are more relevant.

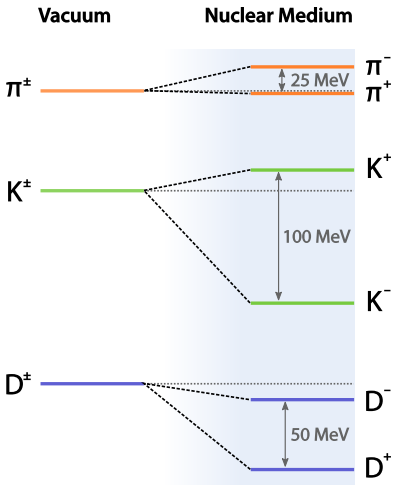


Figure 1.5: Visualization of mass splittings for charge-conjunctive mesons in a nuclear environment compared to their vacuum masses. The splitting of D mesons is not yet measured and based on predictions. Image from [17].

Particularly interesting is the case of the D mesons for which the average mass shift of $D\overline{D}$ is expected to be $50\,\mathrm{MeV/c^2}$ [18] up to $100\,\mathrm{MeV/c^2}$ depending on the used model. The reason why D mesons are a main subject of study is their large constituent mass difference, but this is also source of hard experimental condition to achieve and thus the measurements foreseen by $\bar{P}$ANDA will require further theoretical studies and a better understanding of the experimental capabilities of the detector.

1.2.3 Nucleon structure

The momentum distribution of quarks within a nucleon can be studied with Drell-Yan processes where the annihilation of a quark pair creates a lepton pair. The angular distributions of the final leptons then provide access to the initial quark momentum states.

The electromagnetic form factor of the nucleon has been widely investigated for space-like momentum transfers, but the $\bar{p}p$ annihilation will allow to explore the form factor in the time-like region. The electric G_E and magnetic G_M form factors are accessible by electron positron formation ($\bar{p}p \rightarrow e^+e^-$) and provide insight into both the non-perturbative and regular QCD regime. Especially for high energy transfers Q^2, is common the assumption $|G_\mathrm{E}| = |G_\mathrm{M}|$. $\bar{P}$ANDA will operate with Q^2 up to $20\,\mathrm{GeV}^2$ (which

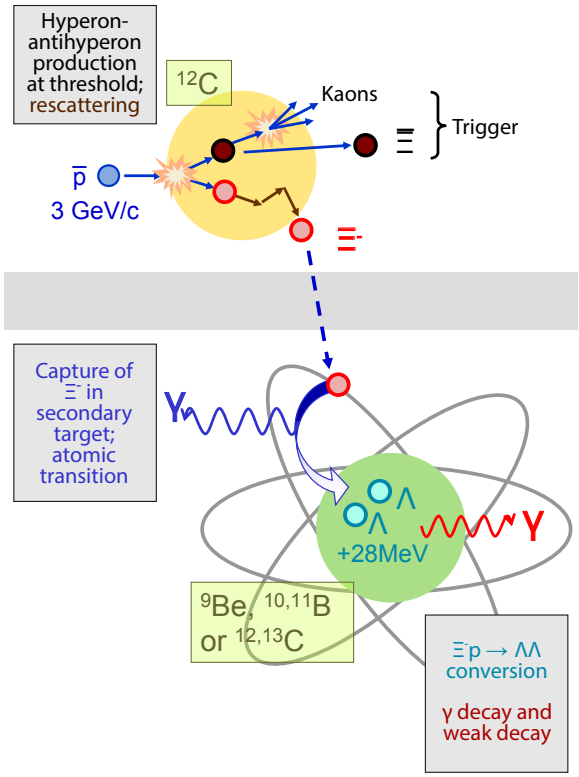


Figure 1.6: The production process of double-Λ hypernuclei with an antiproton beam in PANDA: Slow Ξ from the initial reaction will be stopped in a secondary target (12C) and captured in a nucleus where they will decay into two Λs. Image from [2].

is $5\,\mathrm{GeV}^2$ more than the Fermilab experiments E760 and E835 [19,20]) and will also be able to measure a difference up to around $9\,\mathrm{GeV}$ between the two form factors.

Finally, the General Parton Distributions (GPDs), used to deal with hard exclusive lepton scattering, can be studied through the reactions $\bar{\mathrm{p}}\mathrm{p} \to \gamma\gamma$ and $\bar{\mathrm{p}}\mathrm{p} \to \pi^0\gamma$ [21,22].

1.2.4 Hypernuclei

Nuclei where a nucleon is replaced with an hyperon (i.e., a baryon containing one or more strange quarks) are called hypernuclei. The additional quantum number in such a system increases its degree of freedom, allowing the hyperons to occupy energy states unavailable for protons and neutrons because of the Pauli's principle. For this reason, they can be effectively used to probe the nuclear structure and its modification caused by the presence of hyperons. Therefore, the hypernuclear physics represents a major topic interesting the fields of nuclear, particle, many-body, and astrophysics [23,24].

The existence of hypernuclei is known since the 1950s [25,26] and only six double-Λ hypernuclei have been detected [17]. In $\bar{\mathrm{P}}$ANDA, hypernuclei will be studied using reactions $\mathrm{p} + \bar{\mathrm{p}} \to \Xi^+\Xi^-$ and $\bar{\mathrm{p}} + \mathrm{n} \to \Xi^-\bar{\Xi}^0$ and a dedicated experimental setup [27,28]. Double-Λ hypernuclei will be

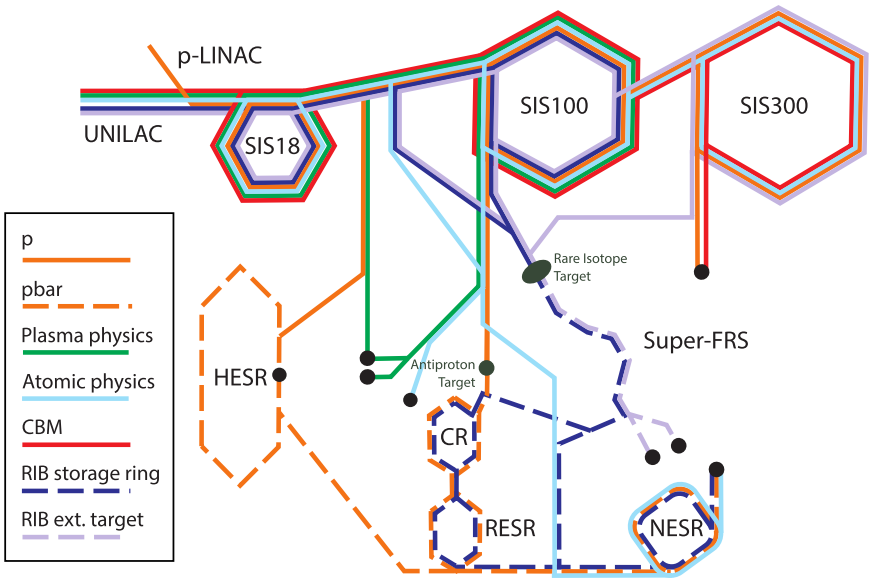


Figure 1.7: The different beam lines of FAIR's accelerator and storage ring complex. Up to four beam lines can be operated in parallel with the orange being the most relevant for $\bar{P}$ANDA. Image from [2].

produced via intermediate $\bar{\Xi}$ production getting decelerated in a secondary target (see figure 1.6). The γ-rays from the de-excitation of the hypernuclei will be detected by an array of high purity germanium detectors.

1.3 The $\bar{P}$ANDA Detector

The $\bar{P}$ANDA detector systems are designed to detect a wide range of charged and neutral particles to reconstruct their trajectories and energies over the almost full solid angle. In the high-luminosity mode of HESR 2×10^7 $\bar{p}p$ annihilations per second happen on average, thus a very high particle rate capability is required alongside a fine vertex and momentum resolution. The vast physics program of $\bar{P}$ANDA does not involve simple event topologies that can be used to trigger the readout, but rather demands a non stop analysis of the data stream and thus a triggerless readout.

To fulfil the above mentioned requirements, the $\bar{P}$ANDA detector foresees two sub-detector systems:

- the Target Spectrometer, oriented around the interaction region in a cylindrical shape covering polar angles greater than 22°;
- the Forward Spectrometer, aiming at reconstructing high-energy, forward-boosted particles at reduced polar angles below 10°.

In the following subsections, a deeper look on the antiproton beam delivered to the $\bar{P}$ANDA detector by the FAIR accelerator facility is essential. Following, an overview on the target system and the main building blocks of the two sub-detectors above mentioned is given, with particular focus on the Micro Vertex Detector.

1.3.1 The antiproton beam

To satisfy the variety of requirements needed by all the experiments at the FAIR facility, a complex of accelerators and storage-cooler rings is foreseen to supply the four research pillars mentioned in section 1.1. Among the many parallel beam lines available, the most relevant for $\bar{\text{P}}$ANDA are the antiproton paths (orange lines in figure 1.7).

The first step of the accelerator complex are two linear accelerators. Alongside the already existing UNILAC, an optimized injection stage will be included for protons, i.e. the Proton Linear Accelerator (p-LINAC). After that, the particles are injected into SIS18 to boost the particles and prepare them for the further acceleration provided by the SIS100 up to the final energy of antiproton production of $29\,\mathrm{GeV}$. The final structure for the antiproton beam is the HESR, a racetrack shaped ring composed of two straight sections $155\,\mathrm{m}$ long and two $180°$ arcs for a total circumference of $575\,\mathrm{m}$ (see figure 1.8).

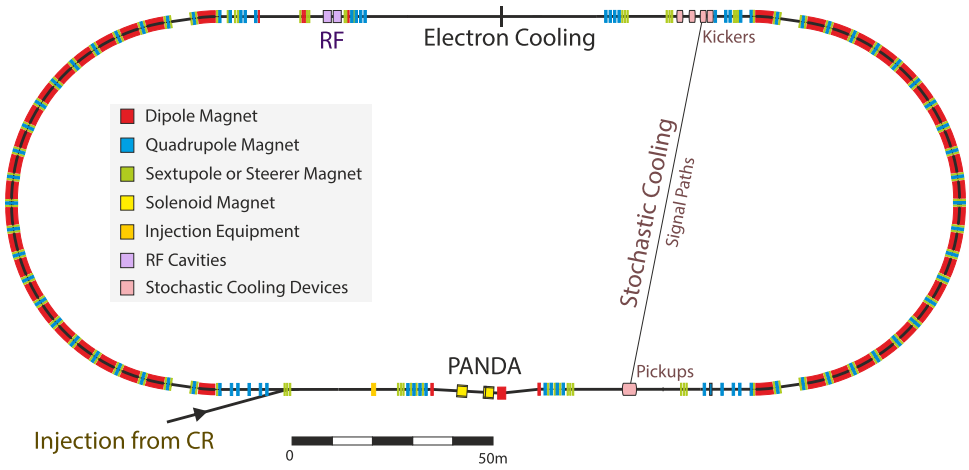


Figure 1.8: Schematic view of the HESR storage ring for antiproton beams with different magnets, acceleration, and cooling components color coded. Image from [2].

The $\bar{\text{P}}$ANDA experiment, acceleration cavities, and cooling equipment are located on the two straight sections of $132\,\mathrm{m}$ each. Two different cooling systems are available: a stochastic cooler with four kickers and the corresponding pickups on the opposite sides of the two straight sections [29]; for antiproton energies up to $8\,\mathrm{GeV}$, an $4.5\,\mathrm{MeV}$ electron cooler is applicable as well, preceded at the beginning by a smaller version with $2\,\mathrm{MeV}$ electrons [30,31].

The accelerator foresees two different mode of operation [32]:

- High precision mode, to achieve a minimal momentum spread of $\Delta p/p = 4 \times 10^{-5}$ with a maximum luminosity of $2 \times 10^{31}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ with $8.9\,\mathrm{GeV/c}$ antiprotons.
- High luminosity mode, to have a maximum luminosity $L = 2 \times 10^{32}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ with $15\,\mathrm{GeV/c}$ antiprotons at the cost of a larger momentum spread of $\Delta p/p = 10^{-4}$.

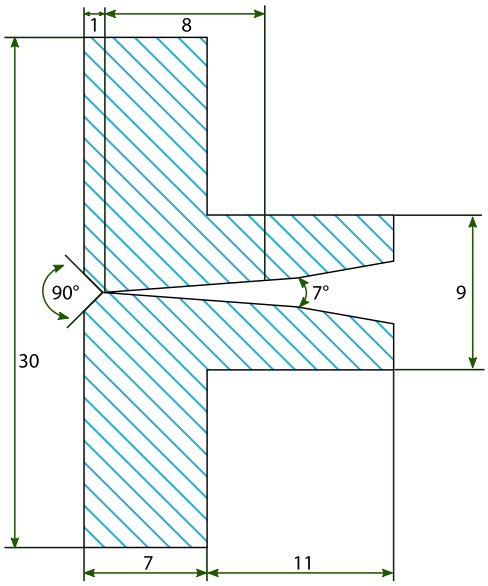


Figure 1.9: An illustration of the cluster-jet target's nozzle. The gas enters from the left through a narrow gap ($\mathcal{O}(10\,\mu\mathrm{m})$) and gets expanded subsequently. Numbers are in mm. Image from [2].

1.3.2 The Target Systems

Two different target systems have been envisaged to provide collision partners for the antiproton beam: the cluster-jet target and the pellet target [33]. The most significant requirement demanded by the desired high luminosity, alongside a low contamination of the beam pipe's vacuum, involve a minimum effective target density of 4×10^{15} hydrogen $\mathrm{atoms/cm^2}$; thus, both systems are being developed to meet this requirement. An overview of their parameters is given in table 1.1.

Table 1.1: Key parameters of the two target systems for $\bar{P}$ANDA [33].

	Cluster-Jet Target	Pellet Target
Effective Target Thickness	$1 \times 10^{15}\,\mathrm{atoms/cm^2}$	$5 \times 10^{15}\,\mathrm{atoms/cm^2}$
Volume Density Distribution	homogeneous	granular
Size Transversal to $\bar{\mathrm{p}}$ Beam	2–3 mm	< 3 mm
Size Longitudinal to $\bar{\mathrm{p}}$ Beam	15 mm	< 3 mm
Target Particle Size	$\mathcal{O}(\mathrm{nm})$	20 µm
Mean Vertical Particle Distance	< 10 µm	2–20 µm
Target Material	H_2, D_2 (heavier gases optional)	H_2, D_2, N_2, Ar (heavier gases optional)

1.3.2.1 Cluster-Jet Target

The working principle of cluster-jet targets is to send pre-cooled gas through a laval-type nozzle (see Figure 1.9). The gas condensate immediately forming a narrow jet of clusters, each with an average of 10^3–10^6 hydrogen

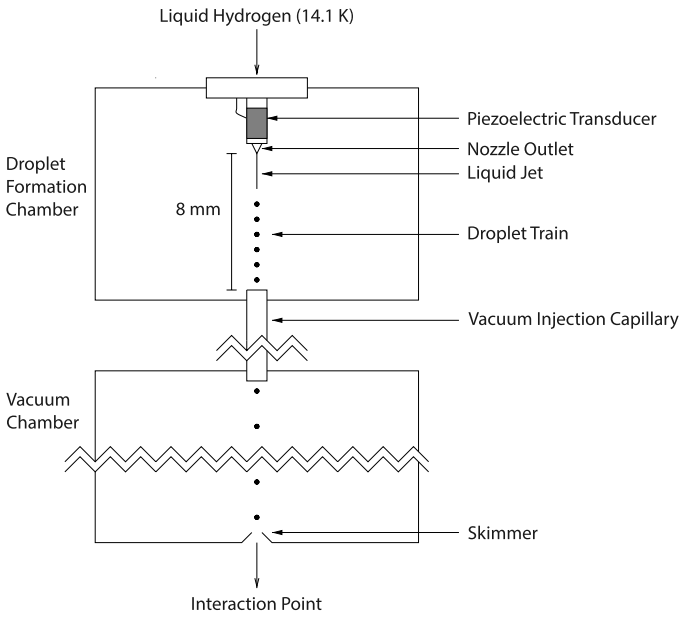


Figure 1.10: A schematic description of the pellet target's working principle. Image from [2].

molecules with sizes of $\mathcal{O}\,(\mathrm{nm})$. The excess gas is extracted by turbomolecular vacuum pumps to minimize contamination in the antiproton beam pipe.

In the directions perpendicular to the beam axis, a good focussing of the antiproton beam allows to define the interaction region very precisely. On the other hand, along the beam direction the uncertainty is considerably higher ($\mathcal{O}\,(\mathrm{mm})$). The main advantage of the cluster-jet is that it provides a very homogeneous and continuous target density that can be varied during operation according to the necessities. Unlike other cluster-jet targets, $\bar{\text{P}}$ANDA's target will operate with incoming material at temperatures of 25–$35\,\mathrm{K}$ and pressures up to $25\,\mathrm{bar}$, resulting in hydrogen fluid. A prototype with the actual $\bar{\text{P}}$ANDA size was built being able to achieve an effective target density of 1.5×10^{15} hydrogen $\mathrm{atoms/cm^2}$ [34].

1.3.2.2 Pellet Target

This kind of target features frozen pellets for high effective target areal densities to achieve the high luminosity. The working principle of this technique is shown in figure 1.10). A cryogenic liquid is injected through a thin nozzle into a gas of the same element close to its triple-point and a piezoelectric transducer, applied on the nozzle, breaks the jet into a series of droplets. The drops pass through a thin capillary into vacuum decreasing their temperature until they freezes into pellets of 25–$40\,\mu\mathrm{m}$ diameter because of surface evaporation. With such a technique, the effective areal density achieved is up to 5 times greater with respect to the cluster-jet approach. Besides, the spatial resolution can be further improved by means of reconstructing the position of individual pellets with an optical tracking system. The size of the pellets plays also an important role on the ratio between the average and the peak luminosity since the latter must be kept below $10^{33}\,\mathrm{cm^{-2}\,s^{-1}}$ to avoid pile-up in the detectors. The design of $\bar{\text{P}}$ANDA's

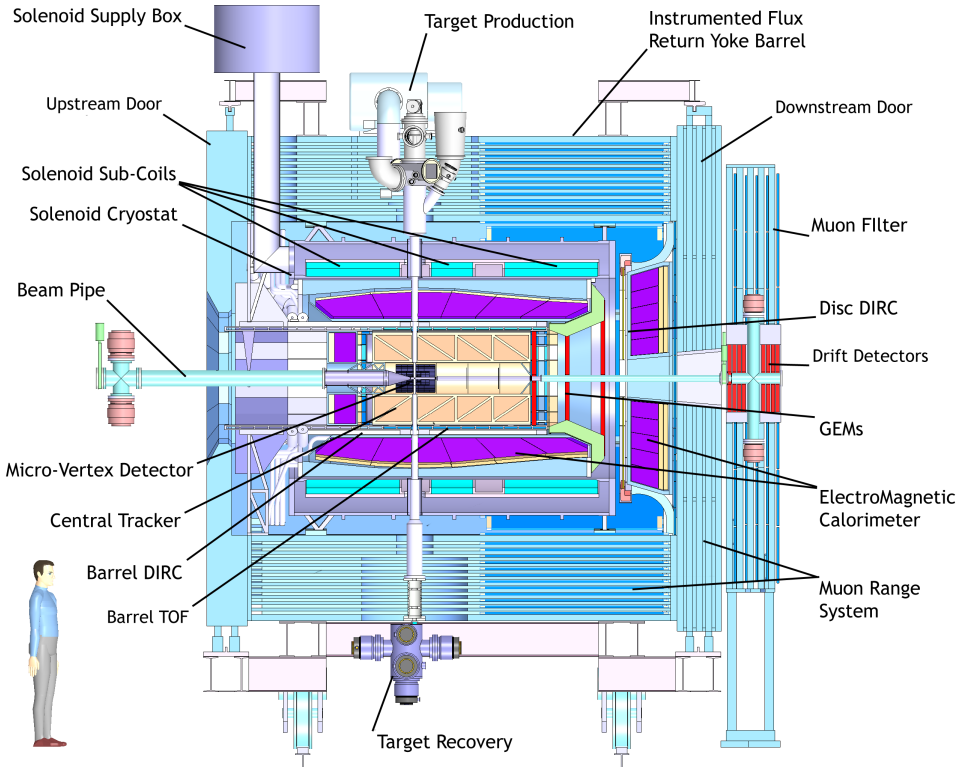


Figure 1.11: Side view of the Target Spectrometer. Image from [36].

pellet target is based on the one currently used at the WASA-at-COSY experiment [35].

1.3.3 The Target Spectrometer

The Target Spectrometer of $\bar{P}$ANDA is built by several detector concentrically placed around the interaction region (see figure 1.21). As mentioned in the introduction of this section, it covers polar angles greater than $22°$ up to $170°$ in the backward region and $5°$–$10°$ in the forward direction. The beam and target pipes are made by beryllium with a diameter of $20\,\mathrm{mm}$ and a wall thickness of $200\,\mu\mathrm{m}$ and the whole spectrometer is merged into a $2\,\mathrm{T}$ field generated by a superconducting solenoid magnet. The detectors building the Target Spectrometer can be divided into six main blocks that will be described in the following subsections.

1.3.3.1 The Tracking Systems

The tracking system of the Target Spectrometer consists of three detectors:

- the Micro Vertex Detector (MVD) surrounding the interaction region;
- the Straw Tube Tracker (STT) enveloping the previous detector;
- the Gas Electron Multiplier (GEM) consisting in three disks in the forward direction.

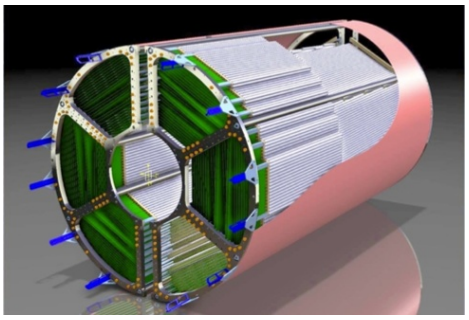


Figure 1.12: A CAD drawing of the STT showing the structure. The MVD is located within the hole in the center. Image from [2].

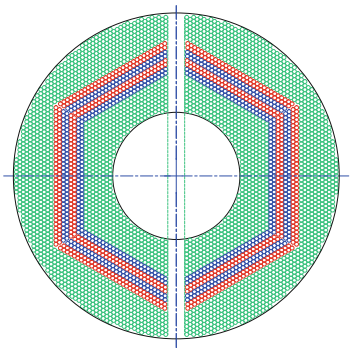


Figure 1.13: A cross section of the straw layers in the x-y projection. Green are parallel to the beam axis, red and blue are skewed by $\pm 2.9°$. Image from [2].

Micro Vertex Detector
The Micro Vertex Detector is the innermost detector designed to provide tracking information with hit points as close as possible to the interaction region, thus its closest sensors are just $2.5\,\mathrm{cm}$ away from the interaction point [37]. The MVD is optimized to measure primary and secondary vertices of charged particles and to contribute to the momentum reconstruction by providing spatial information from their trajectories. The purpose of this thesis is to describe the development work done for the readout electronics of this detector, thus section 1.4 will describe the MVD in more detail.

Straw Tube Tracker
Surrounding the MVD there is the Straw Tube Tracker which is $\bar{P}$ANDA's main tracking detector for charged particles in the Target Spectrometer. It consists of 4636 drift chambers in the shape of long narrow tubes, called straws [38], in a cylindrical arrangement in up to 27 layers (see figure 1.12).

Each straw has a diameter of $10\,\mathrm{mm}$ and a length of $150\,\mathrm{cm}$. The wall of the straw is made of $27\,\mu\mathrm{m}$ thick aluminized Mylar foil acting as the cathode, while a single $20\,\mu\mathrm{m}$ thick gold plated tungsten wire along the axis of the straw represents the anode. The straws are filled with an Ar/CO_2 (90:10 mixture) gas held at an overpressure of $1\,\mathrm{bar}$ making them self supporting. Between the anode and the cathode, an electric field of a few kV ensures a drift of the produced charges with a maximum drift time of $200\,\mathrm{ns}$, providing a resolution in the x and y planes better than $150\,\mu\mathrm{m}$. A z-resolution in the order of $3\,\mathrm{mm}$ is achieved by a peculiar arrangement of the straws (see figure 1.13) foreseeing 8 layers skewed by an angle of $\pm 2.9°$ with respect to the other 19 having a parallel orientation to the z axis. The light construction of such a self-sustaining detector leads to a low material budget of only $X/X_0 = 1.2\,\%$ radiation length in radial direction.

Gas Electron Multiplier
Composed by three disc stations placed $1.1\,\mathrm{m}$, $1.4\,\mathrm{m}$, and $1.9\,\mathrm{m}$ downstream from the interaction point, the GEM detector will measure forward directed particles in an angular range of 3° to 22° (where the coverage of the STT decreases) [17,39]. The GEM disc stations are drift volumes containing micro

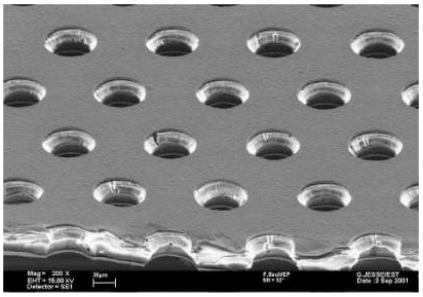


Figure 1.14: A electron microscope picture of a typical GEM electrode with etched holes of $70\,\mu\mathrm{m}$ diameter. Image from [2].

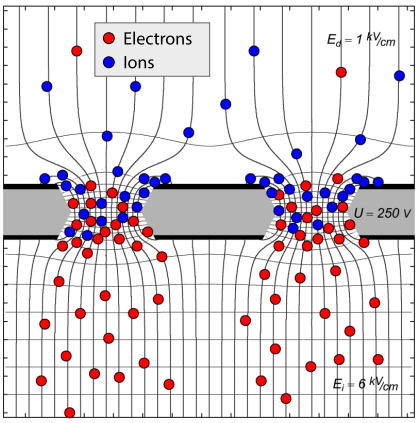


Figure 1.15: A sketch of the GEM's working principle. Strong electric fields lead to gas amplification in the holes. Most ions (blue) are then collected on the back side while electrons (red) continue drifting towards measuring anodes. Image from [2].

perforated thin Kapton foils (around $50\,\mu\mathrm{m}$) with copper coated sides (see figure 1.15). When a high voltage is applied at the two conducting layers, strong electric fields of $\mathcal{O}\,(50\,\mathrm{kV/cm})$ form a dense set of field lines in the holes leading to secondary ionisation and therefore multiplication of the initial charge (see figure 1.14). The advantages of this technique with respect to drift chambers include an easier manufacturing, a more flexible geometry, and a higher rate capability. In particular, this last point is the reason for a double plane of readout pads on each disk since it helps to reduce ambiguities. The outer radius of the disks increases with the distance from the interaction point going from $45\,\mathrm{cm}$ to $74\,\mathrm{cm}$.

1.3.3.2 Particle Identification

The $\bar{P}$ANDA setup foresees several detector to provide an efficient particle identification. A powerful method to extract such an information is to measure the light emitted from particles traversing a material faster than the speed of light in that material. In fact, combining this measurement with the momentum from the tracking system allows to calculate the particle's mass. The light emitted by the particles has a characteristic angle θ_C (depending on the particles velocity) creating a *Cherenkov cone* which is guided towards the readout outside of the central detector where material budget should be minimized. There, the focusing optics and expansion volumes ensure a clean, detectable signal. The $\bar{P}$ANDA particle identification system is built by a barrel part and a forward end cap part plus a Time-of-Flight barrel. The main goal of the system is a separation power of 3σ for π/K up to $4\,\mathrm{GeV/c}$.

Barrel DIRC
The barrel part of the DIRC (Detection of Internally Reflected Cherenkov

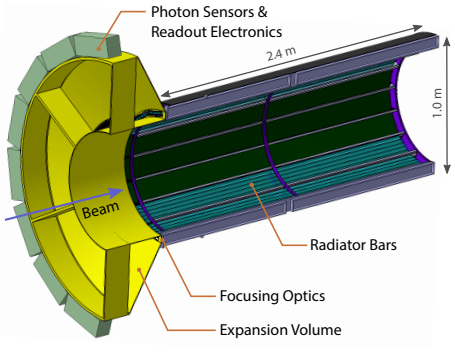


Figure 1.16: The barrel DIRC of the Target Spectrometer with the radiator bars in dark colors and the focusing optics and expansion volume in yellow on the left. Image from [2].

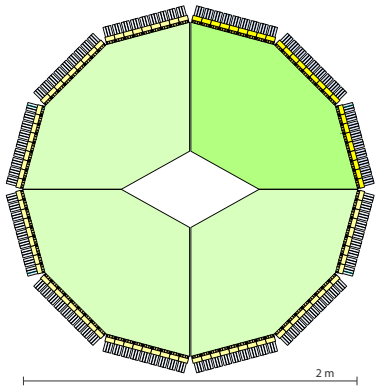


Figure 1.17: The four sectors of the disc DIRC with a hole in the middle for the beam. The focusing optics and readout electronics are placed on the edges. Image from [2].

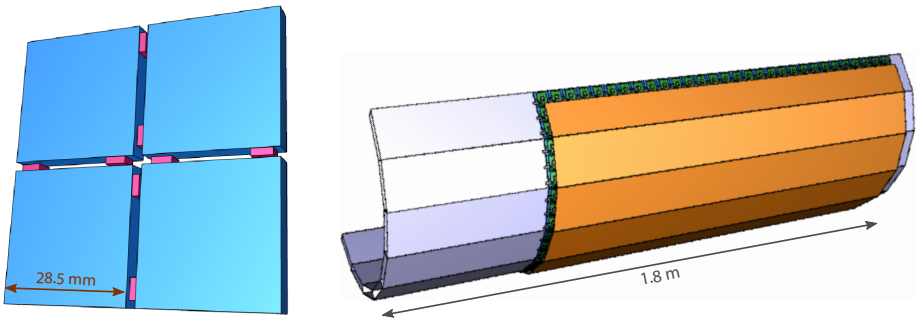
light) detector covers the polar angle from 22° to 140° [40-42]. Its cylindrical shape fits around the STT tracking detector and comprises rectangular radiator bars. The bars have a length of $2.4\,\mathrm{m}$ and are $17\,\mathrm{mm}$ thick. The scintillators are connected to filter optics and expansion volumes, guiding the light to the photon sensors (see figure 1.16). The light is focussed onto micro-channel plate photomultiplier tubes (MCP-PMTs) on the backside of the volume and is converted into an electrical signal with a sum of around $15\,000$ channels. The MCP-PMTs have a pixel size of $6.5\,\mathrm{mm}$ and can work efficiently in the $2\,\mathrm{T}$ field of the Target Spectrometer. The arrival time is measured with a precision of $\mathcal{O}\,(100\,\mathrm{ps})$ and the angular resolution is $8\,\mathrm{mrad}$ to $10\,\mathrm{mrad}$.

Disk DIRC

The disk DIRC shares with the barrel part the same measurement principle but it has a disk-shaped configuration providing π/K separation up to $4\,\mathrm{GeV/c}$ momenta. It is shaped like a regular dodecagon and covers polar angles from 22° down to 10° and 5° for the horizontal and vertical direction respectively. The disk DIRC is made of the same fused silica employed in the barrel part and has a thickness of $2\,\mathrm{cm}$ and a radius of $110\,\mathrm{cm}$. it has four identical but optically separated sub-detectors having their focusing optics and light readout (either MCP-PMTs or SiPMs) placed on the outside (see figure 1.17).

Scintillating Tiles (Time-of-Flight barrel)

The Scintillating Tiles (SciTil) is a Time-of-Flight (TOF) detector providing an accurate timing information for slower particles. TOF detectors are very important since they help disentangling $\bar{P}$ANDA's continuous data stream into single events. The stream has an average time between two events of $50\,\mathrm{ns}$ at its highest luminosity, thus a precise timing information is mandatory. The SciTil is a barrel-shaped scintillator with $<2\,\mathrm{cm}$ radial thickness corresponding to $2\,\%$ radiation length X/X_0 [43] that will be placed just outside the barrel DIRC. About 8000 square plastic scintillator tiles, with a



(a) Four scintillator tiles (blue) and readout (red) forming a module

(b) Half-barrel of SciTil as it will be placed around the barrel DIRC

Figure 1.18: Renderings of the SciTil detector. Images from [2].

side of $20\,\mathrm{mm}$ to $30\,\mathrm{mm}$ and a thickness of $5\,\mathrm{mm}$, are used to form the barrel with the Silicon Photomultiplier (SiPM) and readout electronics facing inside (see figure 1.18).

The SciTil's timing resolution has a foreseen performance of $100\,\mathrm{ps}$ for the full system of scintillator readout [44]. Besides the identification of particles below $1\,\mathrm{GeV/c}$, the detector can also be used to provide track seeds for pattern recognition with the trackers.

1.3.3.3 The Electromagnetic Calorimeter

The Electromagnetic Calorimeter (EMC) of $\bar{P}$ANDA aims at detecting neutral particles (such as π^0 and photons), leptons, and hadrons [45,46]. The EMC is composed by three blocks (see figure 1.19):

- the barrel for tracks above 22°, has an inner radius of $57\,\mathrm{cm}$ and consists of $11\,360$ tapered crystals with a front size of $2.1 \times 2.1\,\mathrm{cm}^2$ placed directly around the TOF detector and read out by Large Area Avalanche Photodiodes (LAAPDs);
- the forward endcap for >5°, built by 3600 tapered crystals in a planar arrangement read out by vacuum photo-triodes [47];
- the backward endcap for >140°, consists of 592 parallelepiped crystals read out by LAAPDs.

The main requirements for the EMC regards an energy resolution in the order of $2\,\%$ at $1\,\mathrm{GeV}$ and a time resolution better than $2\,\mathrm{ns}$. Lead tungstate ($PbWO_4$) fulfil these requirements as scintillating material as proven by the results obtained with the electromagnetic calorimeter of the CMS experiment at CERN [48]. They are $20\,\mathrm{cm}$ long (corresponding to $22\,X_0$ radiation lengths) and operate at $-25\,^{\circ}\mathrm{C}$ in order to increase the light yield by a factor 4 with respect to room temperature.

1.3.3.4 The Solenoid Magnet

The reconstruction of charged particles in $\bar{P}$ANDA is based on the curvature of their trajectories in the magnetic field generated by the superconductive

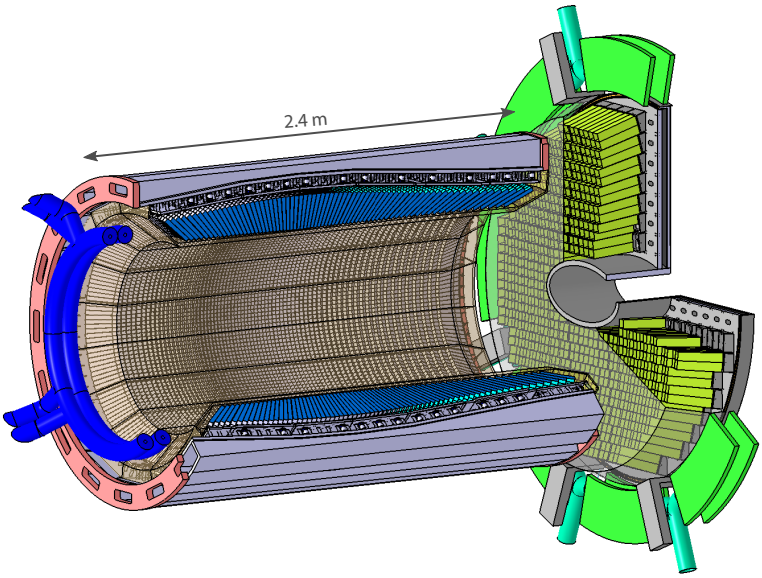


Figure 1.19: The design of the EMC in the Target Spectrometer with cyrstals of the barrel part (blue) and forward endcap (green). Image from [2].

solenoid magnet in the Target Spectrometer [49]. It is designed to provide a homogeneous $2\,\mathrm{T}$ field with fluctuations within $\pm 2\,\%$ in the tracker regions and only small radial field components. All the sub-detectors of the Target Spectrometer except the muon chambers are embedded into the magnet's volume of $4\,\mathrm{m}$ in length and $1.9\,\mathrm{m}$ in diameter. The superconducting coil has a length of $2.8\,\mathrm{m}$ and an inner radius of $90\,\mathrm{cm}$ and two warm bores with a $100\,\mathrm{mm}$ diameter on top and bottom provide the space for the target pipe. The operating current is at $5\,\mathrm{kA}$ and liquid helium is used to maintain superconductivity.

1.3.3.5 The Muon Detector

A proper detection of muons in $\bar{P}$ANDA is crucial for measurements like the identification of J/ψ or investigation of Drell-Yan processes, thus a dedicated muon system is planned as a final detector layer [50]. In the Target Spectrometer, the system is split into two parts (a barrel and an endcap) integrated into the yoke of the solenoid target magnet. A series of aluminium rectangular Mini Drift Tubes (MDTs) is used as a range system to detect muons [50]. MDTs are drift chambers with additional capacitive coupled strips to provide a longitudinal information. For the barrel part, 13 MDT layers, each $3\,\mathrm{cm}$ thick, alternate with $3\,\mathrm{cm}$ thick iron layers. The forward endcap is composed of six detection layers interleaved with five $6\,\mathrm{cm}$ thick iron layers. Downstream of the endcap, an additional muon filter with four iron layers and five MDT layers is placed between the Target and the Forward Spectrometers increasing the muon detection capability and enhancing the magnetic shielding between the two magnetic fields. The muon detection systems are shown in figure 1.20.

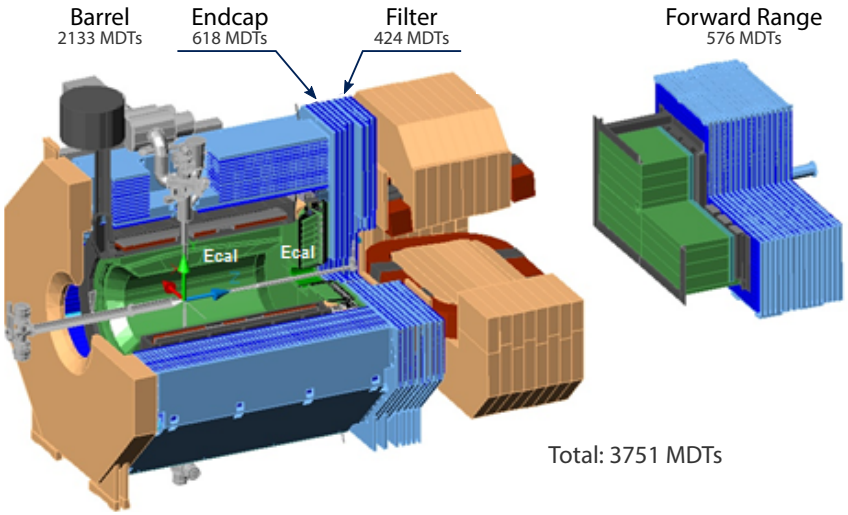


Figure 1.20: The four parts of the muon system of PANDA together with their number of MDTs for the readout. Image from [2].

1.3.4 The Forward Spectrometer

The Forward Spectrometer is designed to measure the particles flying in the forward direction after hitting the fixed target covering polar angles below $\pm 5°$ in vertical and $\pm 10°$ in horizontal direction [51]. It is based on a dipole magnet and composed by trackers, a calorimeter, detectors for particle identification, and a muon detector (see figure 1.21).

The dipole magnet has a maximum rigidity of $2\,\mathrm{T\,m}$ and an opening of about $3\,\mathrm{m}^2$ [49]. Its bending power produces a deflection of the antiproton beam of $2°$ at the maximum momentum of $15\,\mathrm{GeV/c}$. In order to compensate for this deviation, two correcting magnets are placed before and after the $\bar{\text{P}}$ANDA detector, thus the dipole of the Forward Spectrometer is a crucial part of the whole HESR.

1.3.4.1 The Forward Tracking Systems

In the forward region, the tracking is performed by three stations equipped with straw tubes. Each station consists of four sets of straw tubes, with two layers in a set aligned vertically to the beam axis and two skewed by $\pm 5°$ in order to reconstruct the vertical coordinate. Apart form their lengths, the straws are identical to the STT's straws and will also be filled with $\mathrm{Ar/CO_2}$ (90:10 mixture). Another difference with respect to the STT are the lower maximum drift times (130–$150\,\mathrm{ns}$) due to the different magnetic field configuration.

1.3.4.2 The Forward Particle Identification Detectors

The particle identification in the Forward Spectrometer is performed by two detectors: a Ring Imaging Cherenkov detector (RICH) [52] and a TOF wall [53].

The forward RICH design is based on a dual radiator similar to the one used at HERMES [54]. It is located at $6.5\,\mathrm{m}$ downstream of the interaction

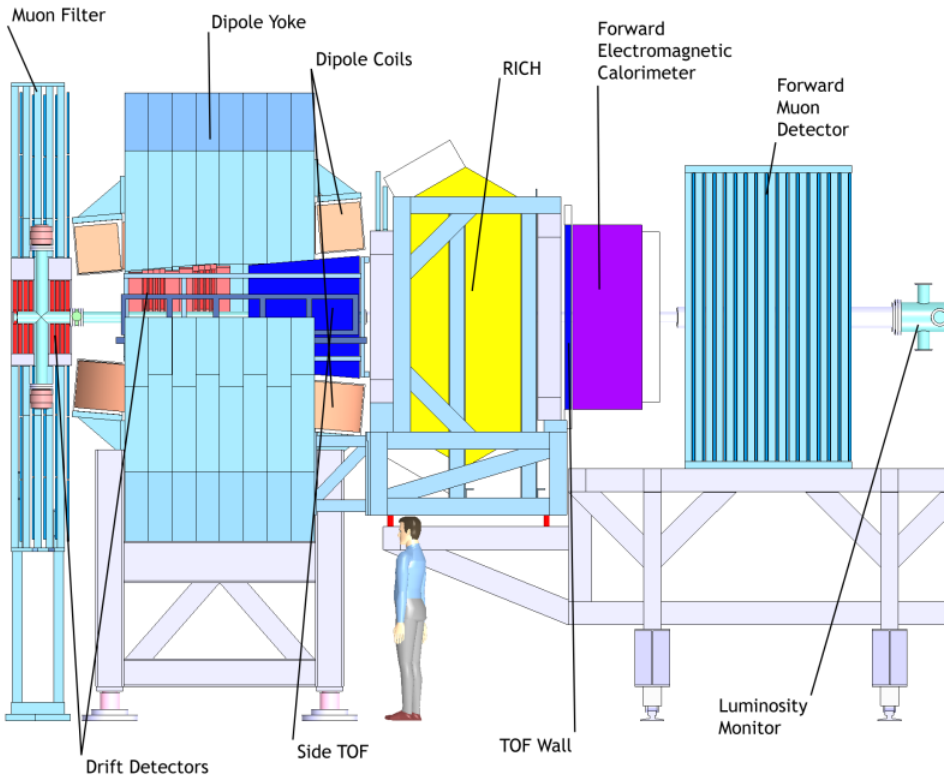


Figure 1.21: Side view of the Forward Spectrometer. Image from [36].

point and covers polar angles $< 10°$ for horizontal and $< 5°$ for vertical directions. The use of silica aerogel (n = 1.0304) and C_4F_10 (n = 1.0014) allows for a π/K and K/p separation in the momentum range 2–15 GeV/c.

The TOF detector in the Forward Spectrometer is arranged as a wall of 140 cm height and 2.5 cm thickness. It consists of three TOF walls made of plastic scintillator slabs read out from both sides with phototubes: one wall is placed perpendicular to the beam at a distance of approximately 7 m from the interaction region, and two smaller walls are placed inside the dipole opening to measure soft particles not escaping the dipole. For this reason, the readout photomultipliers need to be insusceptible to its magnetic field, thus SiPMs are a favourable option. The time resolution of the TOF wall is expected to be between 50–100 ps allowing a π/K and K/p separation momenta of 2.8 GeV/c and 4.7 GeV/c, respectively.

1.3.4.3 The Forward Spectrometer Calorimeter

The Forward Spectrometer Calorimeter provides a $4\,\mathrm{m}^2$ area to measure the energies of the forward boosted particles [55]. The used principle for the calorimeter is called *shashlik calorimeter*. It is realized with alternated plastic scintillator 0.275 mm thick and lead absorber with a thickness of 1.5 mm. The readout is performed with Wavelength Shifting fibres (WLS) coupled to the photomultipliers at the end of the $110 \times 110\,\mathrm{mm}^2$ module [36]. On the bright side, it is a cost-efficient and high-performance solution, but the

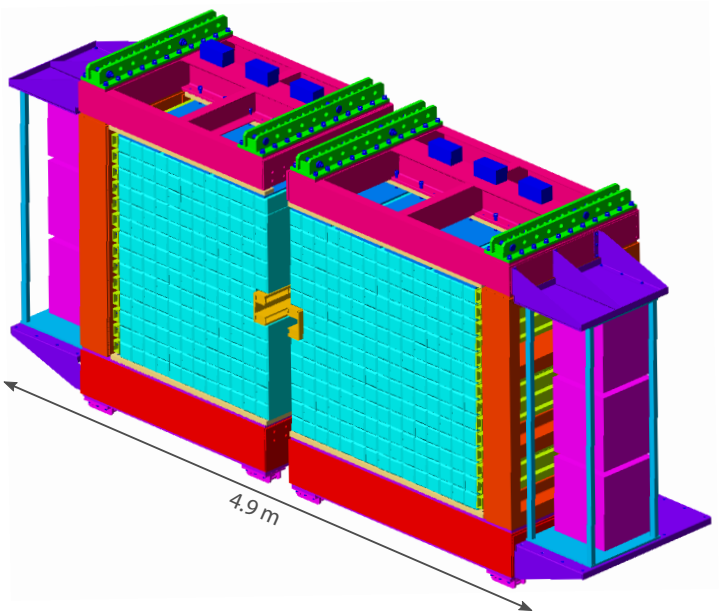


Figure 1.22: A rendering of the Forward Spectrometer Calorimeter detector with scintillator cells in turquoise. Image from [2].

downside is an inhomogeneous light output depending on the angle of entrance. The whole detector, shown in figure 1.22, is composed of 1512 cells each providing a radiation length of $20\,X_0$.

1.3.4.4 The Forward Muon Detector

The muon detector in the forward part is locate about $9\,\mathrm{m}$ downstream from the interaction region. Its design is similar to the system used in the Target Spectrometer where layers of MDTs alternate layers of absorber, each $6\,\mathrm{cm}$ thick, enabling the discrimination between pions and muons. Moreover, the system can measure the energy of neutrons and anti-neutrons with moderate resolution.

1.3.5 The Luminosity Detector

The Luminosity Detector of $\bar{P}$ANDA, shown in figure 1.23, is placed in the most forward part of the experiment [56]. Its purpose is an accurate measurement of the absolute and relative time integrated luminosity with precisions of $5\,\%$ and $1\,\%$, respectively. Elastic scattered antiprotons at very small polar angles (from 3–$25\,\mathrm{mrad}$) with respect to the beam axis are tracked to enable a back-propagation towards the interaction region. Four disks with partially overlapping high-voltage monolithic active-pixel sensors (HV-MAPSs) are used to provide a channel pitch of $80\,\mu\mathrm{m}$ in both directions. To minimize the influence of the beam pipe, the scattered antiprotons enter the detector, merged in a large vacuum box, through a transition cone (see yellow cone in figure 1.23) with walls approximately $10\,\mu\mathrm{m}$ thin.

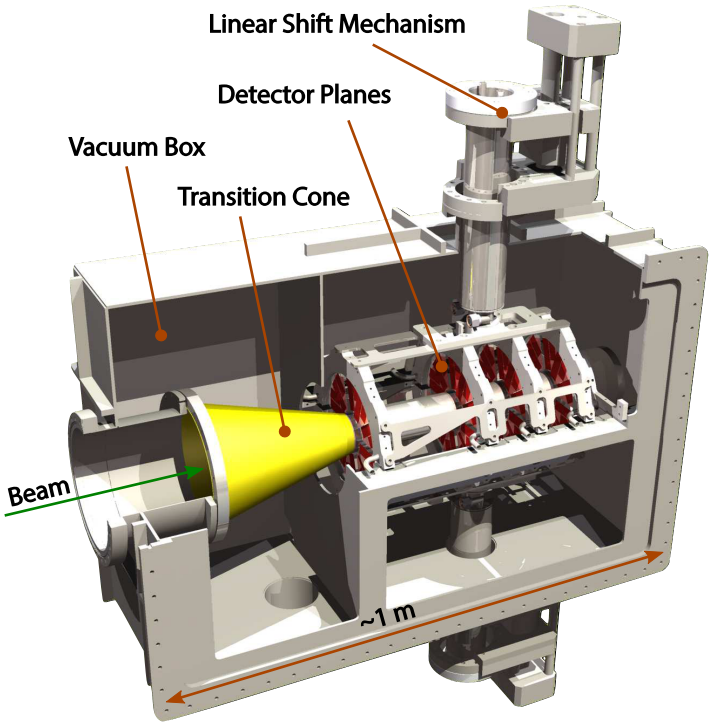


Figure 1.23: A CAD drawing of the Luminosity Detector system. Image from [2].

1.4 The Micro Vertex Detector

As illustrated in section 1.2, $\bar{P}$ANDA's physics program is strongly connected to the measurement of charm and strange hadrons. Therefore, a major task of the detector is to identify those particles through a precise vertex reconstruction. To fulfil these demands, the Micro Vertex Detector (MVD), shown in figure 1.24, provides 3D hit information as close as possible to the interaction region [37]. The detector must be able to determine the primary interaction region and to distinguish it from the secondary vertices from delayed decays of short-lived particles. The performance requirements, the layout, and the detectors building the MVD will be described in the following sections with particular attention to the micro strip sensors directly related to the development work subject of this thesis.

1.4.1 Detector Constraint and Requirements

The MVD is the innermost detector of $\bar{P}$ANDA and this leads to a series of constraints that it has to satisfy. Geometrical constraints regard the size of the detector: the beam pipe outer radius ($1\,\mathrm{cm}$) defines the minimum distance of the innermost layer of the MVD from the beam axis, while the limit of its outermost layer is given by the inner radius of the central tracker ($15\,\mathrm{cm}$). Almost the full solid angle must be covered to maximize the acceptance and, considering the surrounding detectors and structures, the polar angle range is limited to $3°$ to $150°$. To achieve the required resolution in vertex and momentum reconstruction, it is mandatory to have a large

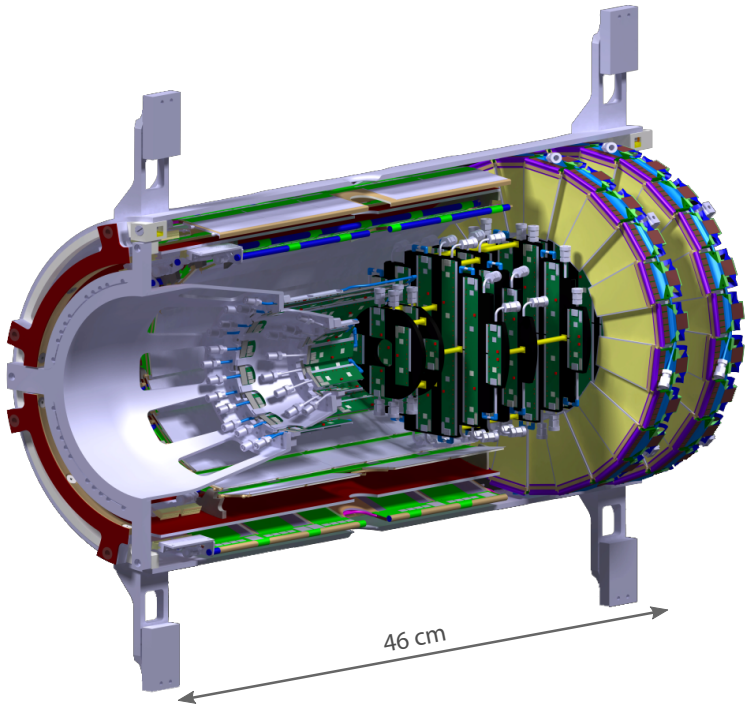


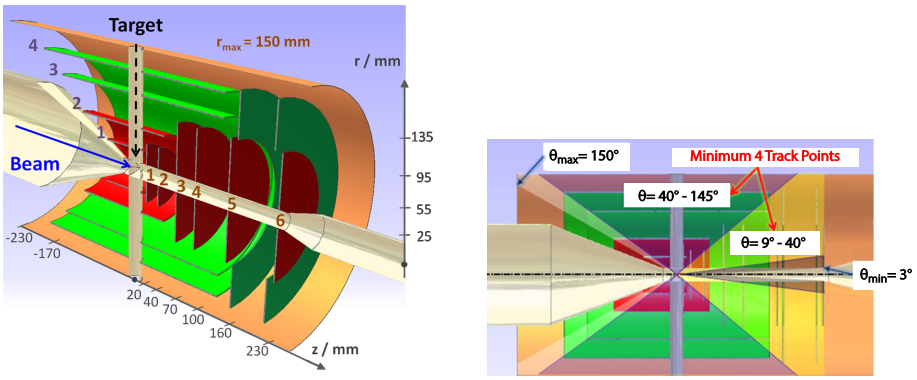
Figure 1.24: A CAD rendering of the MVD with one half of the barrel removed for visibility reasons. The antiproton beam enters from the left. In green on black surfaces are the pixel disk sensor modules, the yellow areas are the trapezoidal strip sensors. Image from [2].

number of hit points as close as possible to the interaction point leading to the need to measure a minimum of 5 hit points per track in the whole acceptance of the detector. The spatial resolution needs to be in the order of $100\,\mu\mathrm{m}$ in the z direction and of a few tens of $\mu\mathrm{m}$ in the xy plane to be able to identify the displaced secondary vertices of open-charm states whose decay lengths measure a few hundred $\mu\mathrm{m}$. Together with the spatial hit information, a time resolution of $\mathcal{O}\left(10\,\mathrm{ns}\right)$ contributes to the task of sorting particles to individual events.

The choice of the technology for the various MVD layers, the granularity of the detector, and the development of the sensors and their readout electronics have been strongly influenced by the expected high interaction rate of 2×10^{17} $\bar{\mathrm{p}}\mathrm{p}$ annihilations per second. Furthermore, the proximity of the first layer of the MVD to the interaction region forces the detector to endure high radiation doses and to provide low material budget. During the expected $\bar{\mathrm{P}}$ANDA operation time of 10 years at $50\,\%$ duty cycle, a predicted $10\,\mathrm{Mrad}$ of total ionizing dose and 10^{13}–$10^{14}\,\mathrm{n/cm^2}$ for $1\,\mathrm{MeV}$ neutron equivalents define the levels the detector components must be able to withstand. Finally, to reduce the impact on the outer detectors and worsening of momentum resolution due to multiple scattering, the limit for the material budget of the MVD is set to $X/X_0 = 10\,\%$ relative radiation length.

1.4.2 Detector Layout

The basic geometry of the MVD, shown in figure 1.25, consists of four concentric barrels and six disks in the forward direction.



(a) The layer orientation and positions, units are in mm.

(b) Side view to visualize the polar angle coverage.

Figure 1.25: The basic layout of the MVD tracking detector. Shown in red are the silicon pixel sensors and in green the silicon strip sensors. Images from [2].

To satisfy the requirements dictated by the high expected rates, the first two barrels and all the six disks of the MVD are instrumented with hybrid pixel detectors [57]. In the outer regions, such a high granularity is not necessary, thus double-sided micro strip silicon sensors cover the last two barrels and the outer rim of the last two disks. This choice meets the demand for low material budget offering at the same time a much lower number of channels to cover a given sensitive area [58].

The four barrels are placed at nominal radii of 25, 50, 92, and 125 mm around the beam axis and have a length of 50, 138, 278, and 312 mm, respectively. The inner diameter of the disks is 22 mm, while the outer diameters are 75 mm and 150 mm, respectively for the first two and the last four disks. Concerning the outer part of the last two forward disks, the inner and outer diameters measure 148 mm and 262 mm, respectively [36].

Due to the geometrical constraints mentioned in the previous section, the outer radius of the MVD is limited to 15 cm by the STT, hence the outermost barrel layer is located at 13.5 mm. In z direction, the detector spreads roughly $\pm$23 cm around the interaction point resulting in at least 4 hit points in a polar angle range of 9°–140°. The operation temperature of the MVD is at around 30 °C, kept stable by a cooling system using low-pressurized water with an inlet temperature of 16 °C. Concerning the material budget requirement, the contribution of the various detector components is shown in table 1.2.

Table 1.2: Contribution of the different components of the MVD to the overall material budget.

	Fraction
Cables for data and supply voltage	37.7 %
Support structures	28.5 %
Active material	15.2 %
Routing of cooling pipes	13.6 %
Readout electronics	5 %

The results of simulations regarding hit multiplicity and material budget are shown in figure 1.26. The design goal of 4 hits per point track is achieved in a large part of the solid angle, though lower values can be seen for polar angles from 40° to 70° (transition area between the disk and the barrel part) and around $\phi = \pm 90°$ (beam pipe location). As of the material budget simulations, the fractional radiation length correlated with the initial θ and ϕ angles of the particle is shown in figure 1.27. The radiation length stays within the design limit of $10\,\% X_0$ in most of the solid angle with $\theta < 140°$, however for greater polar angles it reaches values of several radiation lengths with large deviations along the azimuthal angle because of the routing of all the detector services in the backward direction.

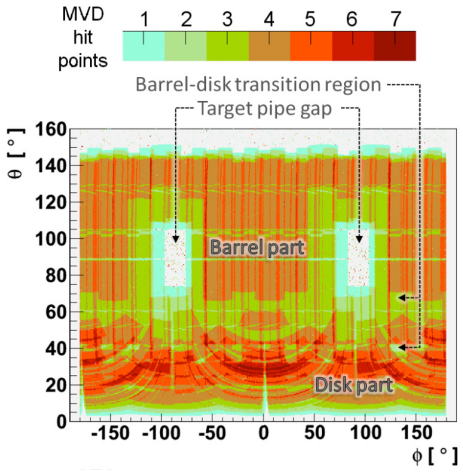


Figure 1.26: Hit multiplicity in the MVD for pions with a momentum of 1 GeV/c from the interaction point. Simulations performed on the layout of the MVD. Images from [2].

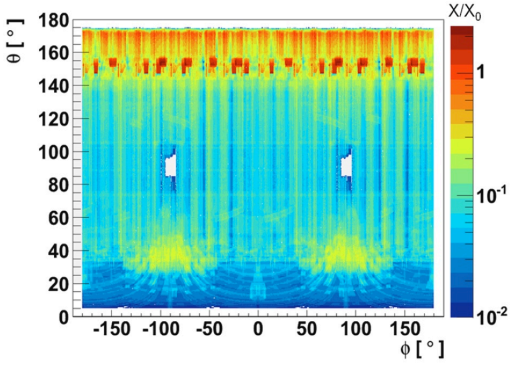


Figure 1.27: The introduced material budget from the MVD in relative radiation lengths. Simulations performed on the layout of the MVD. Images from [2].

1.4.3 MVD Silicon Detectors

1.4.3.1 Signal Generation in Silicon Detectors

An ionizing particle impinging a silicon sensor releases some of its energy generating negatively (electrons) and positively (holes) charged carriers mostly by means of inelastic scattering on shell electrons, i.e. ionization,

excitation. The mean energy loss per passed distance ($\frac{dE}{dx}$), shown in figure 1.28, is described by the Bethe equation 1.1:

$$-\left\langle \frac{dE}{dx} \right\rangle = \frac{4\pi}{m_e c^2} \cdot \frac{nz^2}{\beta^2} \cdot \left(\frac{e^2}{4\pi\epsilon_0} \right) \cdot \left[ln\left(\frac{2m_e c^2 \beta^2}{I \cdot \left(1-\beta^2\right)} \right) - \beta^2 \right] \tag{1.1}$$

where:

- e and m_e are the electron charge and rest mass respectively;
- n is the electron number density;
- $\beta = \frac{v}{c}$ where v is the speed of the particle;
- ϵ_0 is the vacuum permittivity;
- I is the mean excitation potential.

Silicon sensors have a major advantage with respect to gaseous detectors due to the lower energy required to create an electron-hole pair, hence they can be produced thinner without compromising the quality of the extracted signal. In fact, the average energy necessary to liberate one electron-hole pair for silicon is $3.6\,\mathrm{eV}$, while for the gaseous counterpart it ranges from $20\,\mathrm{eV}$ to $30\,\mathrm{eV}$ per pair. However, the charge carrier production is a statistical process, therefore the amount of energy deposited is not constant and especially for thin materials such a probability follows a Landau distribution as shown in figure 1.29.

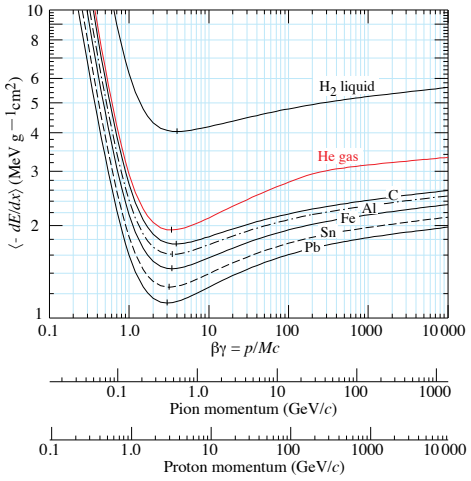


Figure 1.28: The mean specific energy loss in different materials as a function of the particle momentum. Image from [2].

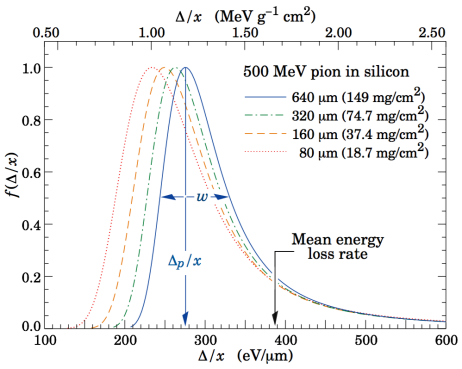


Figure 1.29: The energy loss distribution for $500\,\mathrm{MeV/c}$ pions for different silicon thicknesses. Image from [2].

To detect the charge carriers produced by the just described ionization process, a p-n junction built by two differently doped domains of a semiconductor is completely depleted with a reverse bias. A semiconductor with an excess of electrons is called n-doped, while if the majority carriers

are holes then the part is called p-doped. When no external field is applied, the free electrons in the n-doped volume drift into the p-doped domain to fill the holes there leaving the first positively and the second negatively charged and thus creating an intrinsic electric field. The reverse biasing is a process where an external field counteracting the intrinsic one is applied enlarging the electrically neutral volume (depletion zone). Once the whole volume is depleted, the additional charge carriers created by a charged particle hitting the semiconductor can move relatively freely and be detected. With no segmentation, only the deposited energy can be measured, while the spatial information is obtained segmenting the silicon into strips, pixels, or pads.

1.4.3.2 Hybrid Pixel Detectors

Sensors

The innermost sensors used in the $\bar{\text{P}}$ANDA MVD are based on the technology of hybrid pixels where each sensor is connected individually to the readout chip through a In or Sn-Pb bump. Such a technology has been widely developed for high energy physics, in particular for the LHC experiments. Figure 1.30 shows a cross section of the hybrid pixel sensor. An epitaxial layer of $100\,\mu\text{m}$ is grown on a low resistivity (2–$4\,\text{k}\Omega\,\text{cm}$) substrate with the Czochralski process. The overall thickness of the sensor is in the order of $120\,\mu\text{m}$ thanks to the thinning down of the substrate from hundreds of μm to $20\,\mu\text{m}$ to minimize the material budget.

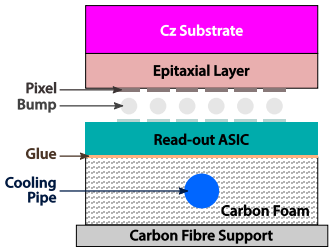


Figure 1.30: A cross-section of the bonding scheme for hybrid-pixel sensors. The Czochralski substrate layer is almost completely removed after bonding. Image from [2].

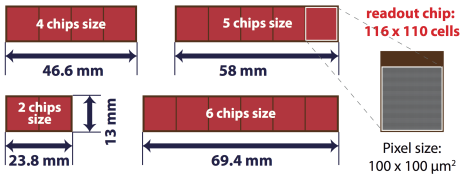


Figure 1.31: Basic sensor geometry in the MVD pixel part: rectangular sensors of four different sizes are used. The elementary unit is the matrix of 116×110 cells in the readout chip, visible on the right. Image from [36].

The detector is built by modules, each consisting of one sensor, the readout chips bump-bonded to it, and a multilayer bus. Depending on the size of the sensor, four different types of modules are foreseen: 2, 4, 5, and 6 (see figure 1.31). The readout ASIC, named ToPix (Torino Pixel ASIC), has been developed in a commercial $130\,\text{nm}$ CMOS technology and its main features will be described in the following paragraph [59]. Finally, the bus, needed to configure the readout chips, transmits the data to the outside of the MVD and provides the power supply to both the chips and the sensor. A full readout matrix contains 116×110 pixel cells for a total area of $1.3\,\text{cm}^2$, thus all pixel sensors taken together make up a total active silicon area of

$0.106\,\mathrm{m}^2$.

Readout
The readout ASIC of the hybrid pixel sensors of the $\bar{\text{P}}$ANDA MVD is called ToPix. The charge information with a $12\,\mathrm{bit}$ resolution is obtained through the Time-over-Threshold (ToT) technique: a channel produces a time stamp for start and length of the input pulses, allowing to reconstruct the deposited energy. The main features of the ToPix chip are summarized in table 1.3.

Table 1.3: Key features of the ToPix chip.

Parameter	Value
Technology	CMOS $130\,\mathrm{nm}$
Input charge dynamic range	up to $50\,\mathrm{fC}$
Power consumption	$120\,\mathrm{mW/chip}$
Front-end noise	$< 200\,\mathrm{e}^-$
Time resolution	$6.8\,\mathrm{ns}$
Charge resolution	$12\,\mathrm{bit}$

A total of 338 readout chips is foreseen for the barrel, 472 for the disk areas. This sums up to 10.3×10^6 readout channels in the pixel part. The connection to the off-detector components is done via optical fibres. Hence, ToPix is directly connected to the CERN-developed radiation hard Gigabit Transceiver ASIC (GBTX) chip [60]. It serializes the data stream onto an optical fibre with a bi-directional transmission speed of up to $4.8\,\mathrm{Gbit/s}$.

1.4.3.3 Double-sided Silicon Strip Detectors

Sensors
The silicon sensors serving the outer region of the $\bar{\text{P}}$ANDA MVD are double-sided micro strips. The detector principle is based on a silicon sensor segmented in narrow strips providing a one-dimensional spatial information with a relatively low number of readout channels. The second coordinate is accessible through a second, tilted array of strips implemented on the same sensor to reduce the material budget. The spatial resolution depends mostly on the strip pitch p according to the following relationship:

$$\sigma_p^2 = \int_{-p/2}^{p/2} \frac{x^2}{p}\, dx = \frac{p^2}{12} \tag{1.2}$$

representing the variance of a uniform distribution with zero average, while the rms is given by:

$$\sigma_p = \frac{p}{\sqrt{12}} \tag{1.3}$$

However, the resolution can be significantly improved if the charge is shared among neighbouring strips [57,61]. The main limitation of the strip detectors with respect to the pixels is the lower particle rate they can sustain, mostly due to ghost hit effect. When two particles hit the detector at the same time, two couples of x and y coordinates are registered, thus the

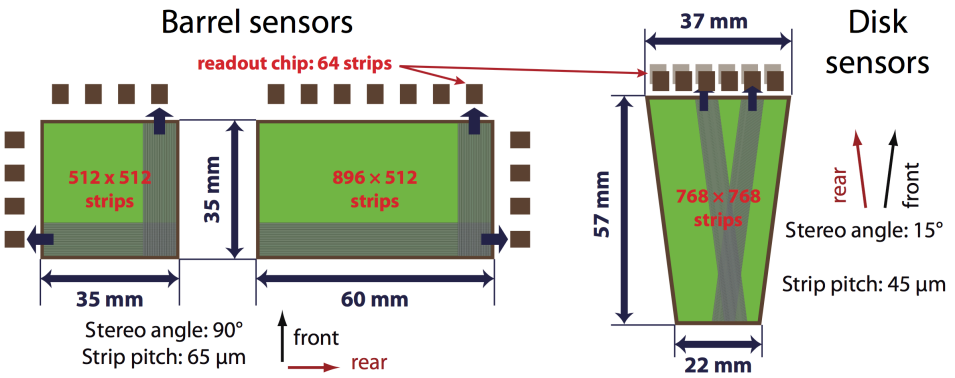


Figure 1.32: Basic sensor geometries in the MVD strip part. Squared and rectangular sensors used for the barrel part (left); trapezoidal sensors employed in the disk part (right). In both cases, every second strip of the sensors is read out. Image from [36].

reconstruction through the analysis of the cross points between the upper and the lower layers is not feasible and requires further assumptions such as on the charge deposition.

The design of the strip detector requires three types of sensors: rectangular and square shaped for the barrel part and trapezoidal for the disk part (see figure 1.32). Hence, the pitch and the stereo angles will be different and with $65\,\mu\mathrm{m}$ and $90°$, and $45\,\mu\mathrm{m}$ and $15°$, respectively [36]. However, the readout pitch will be double with respect to these values. In fact, every second strip will be bonded to the readout electronics exploiting information on the shared charge between neighbouring strips to achieve a better spatial resolution [62].

Readout

The readout of the silicon micro strip sensors of the $\bar{\mathrm{P}}$ANDA MVD is performed by a full custom chip named PASTA ($\bar{\mathrm{P}}$ANDA Strip ASIC). As for ToPix, the charge information is extrapolated using the Time-over-Threshold technique offering several advantages with respect to a more standard amplitude measurement. The ASIC is able to provide accurate time measurements thanks to a Time to Digital Converter (TDC) inherited from a chip developed for medical physics applications named TOFPET [63]. The key features of PASTA are shown in table 1.4 but an extensive description of the ASIC implementation and performance will be the subject of chapters 3 and 4.

Table 1.4: Key features of the PASTA chip.

Parameter	Value
Technology	CMOS 110 nm
Input pitch	63 µm
Rate capability	100 kHz/channel
Power consumption	4 mW/channel
Front-end noise	$< 600\,e^-$
Time bin width	50–400 ps
Charge resolution	8 bit (dynamic range)*
Radiation tolerance	100 kGy*

*: Design goal

The rate capability of 100 kHz/channel meets the requirement of 40 kHz/channel estimated for the micro strip sensors from simulations [37], the overall power consumption fits the cooling system design, and the small time bin width guarantees a better charge resolution through a more precise pulse length reconstruction. The last two entries of table 1.4 are indicated as design goals since they will be verified with the prototype. In particular, radiation hardness will be a very interesting topic to study since the CMOS technology used in the design is quite young in the field of high energy physics, so no information nor reference on this matter is available.

Chapter 2

Front-End Amplifiers

Radiation detectors convert the energy lost by an incident particle into an electrical signal to be processed by the readout electronics. The physics of the process under study, the sensor characteristics, and additional constraint such as the power consumption or the available space, determine the choice of the front-end electronics parameters. Therefore, a customized option is preferred to a commercial solution, thus the need to design an ASIC (Application Specific Integrated Circuit). In this chapter, a theoretical study of the main characteristic of a front-end amplifier will be given to help the understanding of chapter 3 describing the implementation of the PASTA chip. If not stated otherwise, the information presented in this chapter is taken from [64].

2.1 Key Parameters in Front-End Electronics

An ASIC usually consists of an array of identical channels performing in parallel the same functions. Each channel contains an input amplifier followed by several analog and/or digital stages optimizing the signal shape to simplify the processing of the detector signals. The first stage of a front-end amplifier, directly connected to the sensor, is the *preamplifier*, while the following stages are commonly indicated as the *pulse shaper* since they determine the frequency spectrum of the output pulse hence its shape.

A block scheme of a typical front-end amplifier is shown in figure 2.1. The first step to understand the behaviour of such an architecture is to inspect its transfer function. A first, simple approach is particularly useful on this matter, thus the following assumption will be made for a preliminary study:

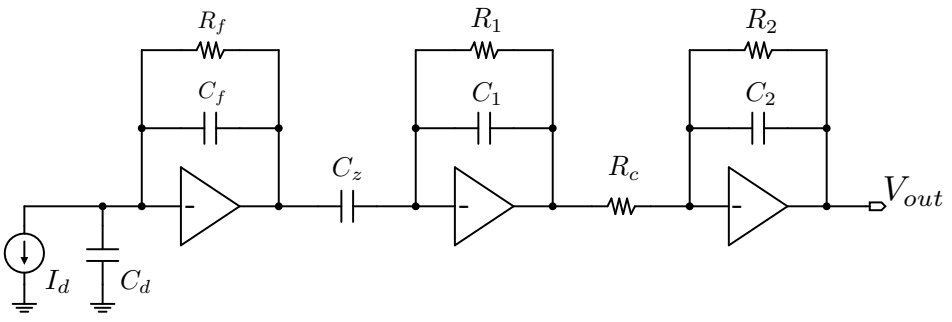


Figure 2.1: Block schematic of the exemplary preamplifier discussed in the text.

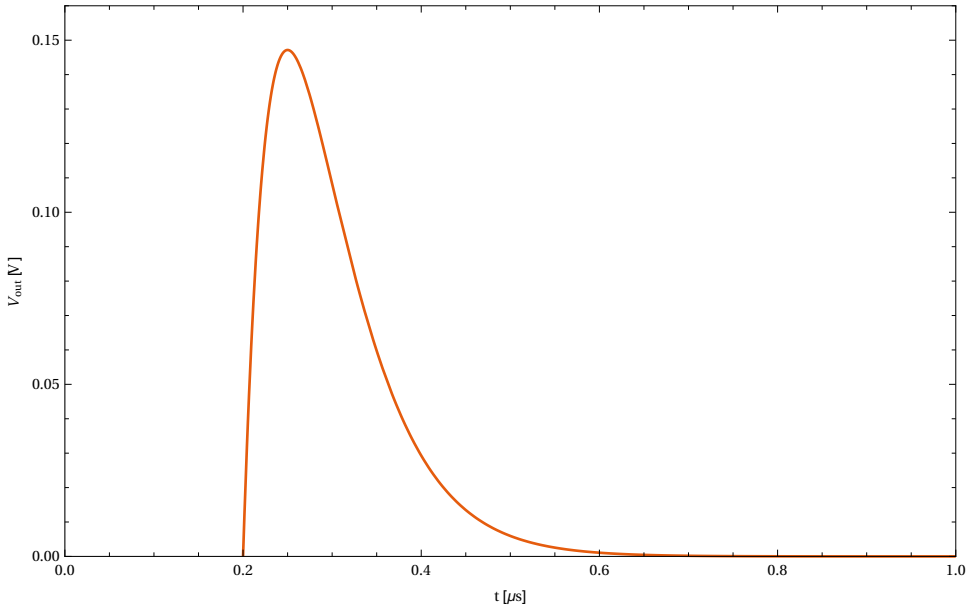


Figure 2.2: Impulse response of the front-end amplifier shown in figure 2.1.

- the detector signal can be approximated with a Dirac delta distribution. The input signal can therefore be written as $I_{in}(t) = Q_{in}\delta(t)$ in the time domain, while in the Laplace domain it simply assumes the constant value Q_{in} representing the total charge contained in the sensor pulse;
- the core amplifiers are ideal voltage amplifiers with infinite gain and bandwidth;
- the preamplifier works as an ideal integrator meaning that its feedback resistance R_f is large enough that its contribution to the signal processing is negligible and it has the only purpose of establishing a DC feedback for a proper biasing of the stage;
- the time constants in the feedback loops of the shaping stages are matched, i.e. $R_1C_1 = R_2C_2 = \tau$.

Under these assumptions, the output signal in the Laplace domain is given by:

$$V_{out}(s) = Q_{in}\,\frac{C_z}{C_f}\,\frac{R_1R_2}{R_c}\,\frac{1}{(1+s\tau)^2} \tag{2.1}$$

Applying the Inverse Laplace Transform to the above equation, the signal representation in the time domain is obtained:

$$V_{out}(t) = Q_{in}\,\frac{C_z}{C_f}\,\frac{R_2}{R_cC_1}\,\frac{t}{\tau}\,\mathrm{e}^{-\frac{t}{\tau}} \tag{2.2}$$

The waveform represented by equation 2.2 is shown in figure 2.2 assigning the following values to the involved parameters:

- $Q_{in} = 1\,\mathrm{fC}$

- $C_z = 50\,\mathrm{pF}$
- $C_f = 500\,\mathrm{fF}$
- $C_1 = C_2 = 500\,\mathrm{fF}$
- $R_1 = R_2 = 100\,\mathrm{k\Omega}$
- $R_c = 50\,\mathrm{k\Omega}$

To make the plot more readable, the input stimulus is applied at $t = 2 \times 10^{-7}\,\mathrm{s}$ and the quiescent point of the output is assumed to be $0\,\mathrm{V}$. In practical cases, the output signal is superimposed on a voltage value called *baseline* needed for a proper biasing of the transistors forming the core amplifiers.

2.1.1 Peaking Time

The time required for a signal to swing from the baseline to its maximum is defined as the peaking time. In the example reported in figure 2.2, the peaking time is $T_p = \tau = 50\,\mathrm{ns}$. This parameter is crucial for the design of a front-end amplifier because it determines the speed and the noise of the system. Typical values range from nanoseconds for fast systems optimized for timing measurements, to several microseconds for high resolution spectroscopy. If the peaking time is shorter than the sensor signal collection time, for the same total charge the output signal exhibits a smaller peak than the one observed with a Dirac delta input. This amplitude loss is called *ballistic deficit*. The ballistic deficit can be neglected if the sensor collection time is constant or if the shape of the detector signal does not vary with the amplitude or with other parameters.

2.1.2 Gain and Signal Polarity

The gain of a front-end amplifier is usually given by the ratio between the peak of the output voltage and the input charge. In the example of figure 2.2, the input charge $Q_{in} = 1\,\mathrm{fC}$ leads to an output signal with amplitude of about $150\,\mathrm{mV}$, hence the gain is $150\,\mathrm{mV/fC}$. In a linear system, the gain should be chosen so that the maximum signal of interest brings the comparator as close as possible to its saturation. To identify the largest input signal that the amplifier can treat without saturating, it is necessary to define the output linear dynamic range (LDR_{out}). This term describe the ratio between the highest output voltage preserving the proportionality between the input and the output signal and the rms output noise. Dividing this ratio by the gain yields the input linear dynamic range LDR_{in}:

$$LDR_{out} = \frac{V_{out,max}}{rmsNoise} \tag{2.3}$$

$$LDR_{in} = \frac{LDR_{out}}{Gain} \tag{2.4}$$

In principle, the gain of the amplifier is chosen considering the expected input range according to the following relationship:

$$Gain = \frac{LDR_{out}}{Q_{in,max}} \tag{2.5}$$

However, as discussed in section 1.4.3.1, the charge generation process in a sensor is affected by statistical fluctuations, so the maximum signal to be treated is not a fixed value. Therefore, when choosing the gain, attention must be paid to the specifications of the detector regarding the expected fluctuations of the input signals.

The polarity of the front-end output depends on how many stages are employed and on their nature (inverting or non-inverting). To maximize the LDR_{out}, the baseline in each stage must thus be appropriately chosen. Consider for example the simple front-end amplifier shown in figure 2.1: it has three inverting stages, hence if the input signal has a positive polarity the baseline of the first and third stage should be close to the ground, while the one of the second stage close to the positive power supply (the opposite is true for an input signal with a positive polarity). The polarity of the input signals depends on the selected detector, thus once it is fixed the ASIC can be designed accordingly. Nevertheless, developing a chip that can handle both polarities can increase the chance of re-using it or be explicitly required. An easy approach to build a system capable able to handle signals of either polarity is to fix the DC bias voltage at the output of each stage half-way between the supply rails, leaving equal margin for signals swinging upwards and downwards. However, this solution halves the possible dynamic range, but since for a given detector the signal polarity does not change during operation, a programmable baseline is the preferable design choice.

2.1.3 Noise

The term noise refers to disturbances generated within the sensor and the front-end amplifier, thus it is intrinsic to the system and cannot be eliminated. Physically, noise stems from the fact that the finite number and speed of the mobile charges in electronic devices. In fact, any fluctuation in the number or in the speed of carriers produces modifications of currents and voltage levels inside the circuit.

To estimate the noise strength, it is necessary to use quantities related to the square of the noisy waveform, such as the sample standard deviation:

$$V_{std} = \sqrt{\frac{1}{N-1}\sum_{k=1}^{N}\left(V_k - V_{av}\right)^2} \tag{2.6}$$

where V_k is the amplitude of the k^{th} pulse and V_{av} is the average value. The quantity obtained is called the *rms output noise* which is usually given as Equivalent Noise Charge (ENC) referred to the amplifier input. In fact, the total charge delivered by the sensor is one of the most relevant information of interest, so using the ENC allows for an immediate comparison between the noise and the signal to be measured. The formula to translate from volts

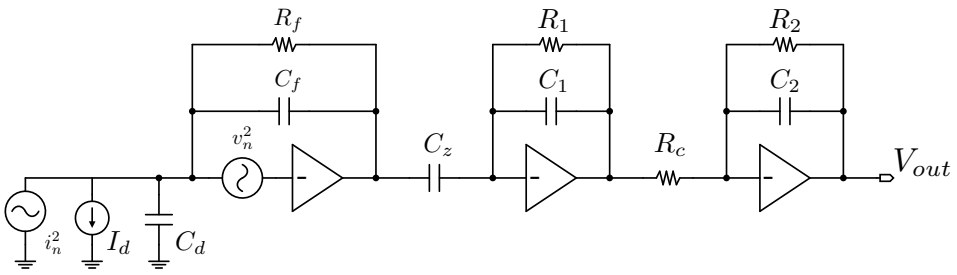


Figure 2.3: Front-end amplifier with input referred parallel and serial noise sources.

(natural unit of measurement) to charge, and thus number of electrons, is the following:

$$ENC = \frac{rmsNoise}{Gain}\,\frac{1}{e} \tag{2.7}$$

where the term containing the electron charge $e = 1.602 \times 10^{-19}\,\mathrm{C}$ converts the ENC into number of electrons. The noise requirements may vary from a few electrons in high resolution spectroscopy to thousands of electrons in readout electronics for high capacitance sensors, such as silicon photomultipliers.

Noise is generated by the sensor leakage current, by the detector bias resistors, and by the devices forming the front-end amplifier. In circuit analysis, the effect of the noise is calculated using the concept of equivalent noise sources modelling the noise as a voltage or as a current contribution. Voltage noise sources are connected in series with the amplifier (series noise), while the current noise sources are connected in parallel (parallel noise), as shown in figure 2.3. The quantity associated to these sources is the *noise spectral density* and represents the power delivered by the noise source into a resistor of $1\,\Omega$ and in a bandwidth of $1\,\mathrm{Hz}$, so that the units are V^2/Hz and A^2/Hz. As a function of frequency, the spectral density may be flat (white noise) or display some dependency (coloured noise). A major example of white (considering the most common range of frequency of interest in front-end electronics) noise is the so called thermal noise due to the fluctuations of the speed of charge carriers produced by thermal agitation. The flicker noise represents instead the most important contribution from coloured noise and its spectral density explains why it is usually indicated as 1/f noise:

$$v_{n,f}^2 = \frac{K_f}{f} \tag{2.8}$$

where K_f is constant for a given device. The noise introduced by the amplifier itself is usually dominated by the series noise with a combination of white and flicker components. Typically, in well designed circuits, the major noise contribution is given by the input transistor and it is in the range of a few $\mathrm{nV}^2/\mathrm{Hz}$.

An easy way to reduce the noise in a front-end amplifier consists in a proper adjustment of the peaking time. Detailed calculations, that will be

discussed in the following sections, show that in a continuous time front-end the equivalent noise charge can be expressed as:

$$ENC = \frac{1}{e}\sqrt{(C_d + C_{in})^2 \left(A_w v_n^2 \frac{1}{T_p} + A_f K_f\right) + A_p i_n^2 T_p} \tag{2.9}$$

In this equation, e is the electron charge, C_d and C_{in} are respectively the detector capacitance and the sum of all the other parallel capacitances seen by the input (including the amplifier input capacitance), A_w, A_f, and A_p are constant coefficients depending on the front-end transfer function, v_n^2 and i_n^2 are respectively the input-referred voltage and current spectral noise densities, and T_p is the peaking time.

A few important points must be noted:

- the effect of series noise (both thermal and flicker) is directly proportional to the input capacitance implying that sensors presenting a small capacitance to the front-end amplifier are preferable;
- the thermal series noise and the parallel noise are weighted in opposite ways by the peaking time, while the flicker noise is not affected by this parameter.

This last observation highlights that an optimal value of peaking time can be found to optimize the noise performance. Figure 2.4 shows an example of this trade-off.

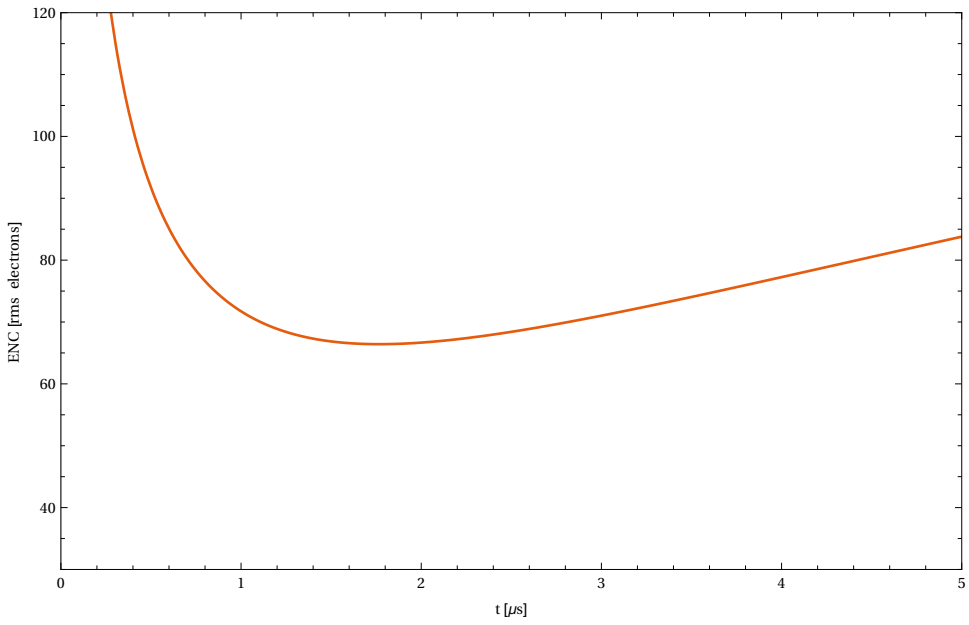


Figure 2.4: ENC versus peaking time for a leakage current of 100 pA.

For the sake of simplicity, the contribution of flicker noise has been neglected, while the values of the other parameters are:

- $C_d + C_{in} = 10\,\mathrm{pF}$
- $A_w = A_p = 1$

- $v_n^2 = 1\,\mathrm{nV}^2/\mathrm{Hz}$
- $i_n^2 = 2eI_L$ where e is the electron charge and $I_L = 100\,\mathrm{pA}$ is the leakage current

This last point derives from calculations showing that in semiconductor sensors the leakage current associated to the reverse bias junctions is often an important noise source that can be modelled by a current source in parallel to the front-end input. The optimum peaking time is about $T_p = 1.8\,\mu\mathrm{s}$ corresponding to $ENC = 60\,\mathrm{electrons}$. Considering the example of figure 2.1, a peaking time of $50\,\mathrm{ps}$ is non-optimal, but since $T_p = \tau = R_1C_1 = R_2C_2$, increasing the value of the passive components improves the noise performance at the cost of a larger silicon area occupied. An interesting analysis regards the change in noise when the leakage current is increased by an order of magnitude. In figure 2.5 can be noticed that the optimal peaking time has changed to about $500\,\mathrm{ns}$ and that the minimum achievable noise has increased by a factor of two. This example shows that even small values of leakage current have a significant impact on the noise performance of a front-end amplifier. Further and more detailed analysis will be discussed in the following sections of this chapter.

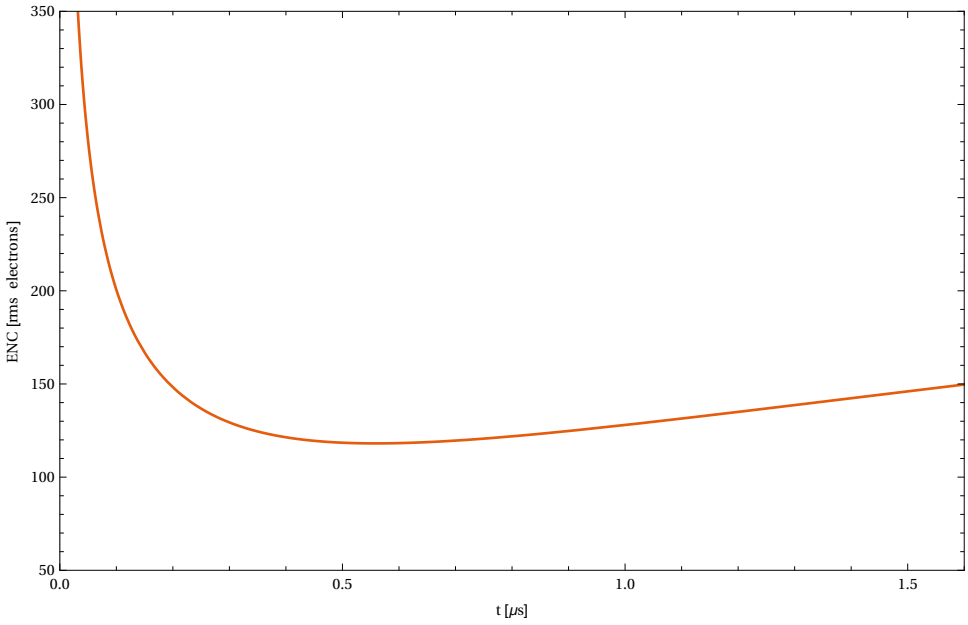


Figure 2.5: ENC versus peaking time for a leakage current of $1\,\mathrm{nA}$.

2.1.4 Time Resolution

The noise optimization discussed so far assumes that the information of interest is the energy, thus the quantity to maximize is the so called Signal-to-Noise Ratio (SNR) i.e. the ratio between the peak of the output signal and the noise floor. Under this assumption, it is advantageous to work with a peaking time as long as permitted by parallel noise. Of course, the peaking time optimization does not apply in case of time-based applications where events must be ordered in time with a certain accuracy. For time measurements, a comparator is usually connected to the output of the

front-end amplifier and when the input signal crosses a predefined threshold, the comparator fires updating the status of a counter counting clock pulses. However, even identical signals have a different transition point because of the *timing jitter*. This phenomenon is due to the uncertainty in the threshold crossing time caused by the noise present at the amplifier output.

From a mathematical point of view, around the nominal transition point t_0, the amplifier output can be approximated with a first order Taylor expression:

$$V_{out} = V_{out}(t_0) + \left.\frac{dV_{out}}{dt}\right|_{t=t_0} (t - t_0) \tag{2.10}$$

Under the licit assumption that the noise standard deviation at the amplifier output is a measure of a typical voltage variation, using 2.10, the relationship between the voltage and time uncertainty can be written as:

$$\sigma_V = \left.\frac{dV}{dt}\right|_{t=t_0} \sigma_t \implies \sigma_t = \frac{\sigma_V}{\left.\frac{dV}{dt}\right|_{t=t_0}} \tag{2.11}$$

where σ_t represents the timing jitter. In other terms, the timing jitter is given by the noise divided by the signal slope around the threshold. In general, the noise of a system is proportional to the square root of the bandwidth (BW), while the signal slope is directly proportional to it, thus:

$$\sigma_t \propto \frac{1}{\sqrt{BW}} \tag{2.12}$$

meaning that faster systems have better timing performance. These results show that there is a trade-off between energy and time measurements. In energy measurements it is important to minimize the amplitude jitter, σ_V calling for peaking time as long as permitted by rate and/or parallel noise considerations. In timing applications instead it is important to minimize the slope-to-noise-ratio demanding for fast peaking times.

Finally, it must be noted that in timing measurement the ultimate limit on the shaping time is given by the speed of the sensor signal. In fact, the total rise time T_{tot} at the amplifier output can be estimated as:

$$T_{tot} = \sqrt{T_p^2 + T_c^2} \tag{2.13}$$

where the term T_c represents the sensor signal collection time. The signal slope is inversely proportional to T_{tot}, so is the amplifier slope to the square root of the peaking time, hence:

$$\sigma_t \propto \sqrt{T_p + \frac{T_c^2}{T_p}} \tag{2.14}$$

The minimum value of σ_t is obtained for $T_p = T_c$, therefore for an optimal time resolution the shaping time should match the charge collection time in the sensor.

2.1.5 Pile-Up

The choice of the peaking time is not only influenced by noise considerations but also by rate requirements. In fact, the amplifier output must return to the baseline before a new pulse can be processed, otherwise the two signals will pile-up. The time of arrival of the events on a radiation detector usually follows a Poisson distribution:

$$P(n) = \mu^n \frac{\mathrm{e}^{-\mu}}{n!} \tag{2.15}$$

where $P(n)$ is the probability of observing n events in a process with a mean value of μ. The following example will help to understand the meaning of this relationship. Consider a maximum front-end amplifier output pulse length of $1\,\mu\mathrm{s}$ and an event rate of $200\,\mathrm{kHz}$ (i.e. average interval between two events of $5\,\mu\mathrm{s}$). To avoid pile-up, the requirement is to have no event on the occupied channel during the busy time. The probability for this to happen is obtained by 2.15 putting $n = 0$ (no event arrives in the considered time) and $\mu = 0.2\,\mathrm{events}$ (average events in the $1\,\mu\mathrm{s}$ interval). The result is thus given by $\mathrm{e}^{-0.2} \approx 82\,\%$ meaning that about $18\,\%$ of the events of interest will overlap. The amount of tolerable pile-up depends on the particular application, but in general it can be handled using a front-end with fast return to baseline and/or increasing the sensor granularity to reduce the event rate per channel. In case none of the mentioned options is possible, a logic circuit called Pile-Up Rejector (PUR) can be introduced to detect the occurrence of a pile-up condition and discard overlapping pulses that would result in incorrect amplitude measurement.

2.1.6 Detector Efficiency and Derandomization

In case a very fast front-end is used, the channel dead-time is dominated by the time necessary to read the data out. Considering input events following a Poisson distribution with an average event rate of $100\,\mathrm{kHz}$ and a busy time of $10\,\mu\mathrm{s}$, the probability that an event arrives and has to be rejected because the channel is already occupied can be calculated using (2.15) with $\mu = 1$:

$$P_{loss} = 1 - P(0) = 1 - \mathrm{e}^{-1} \approx 63\,\% \tag{2.16}$$

The straightforward approach to reduce the event loss is to speed-up the system, so to achieve an inefficiency below $1\,\%$ the required average events must be:

$$P_{loss} = 1 - P(0) = 1 - \mathrm{e}^{-\mu} = 1\,\% \implies \mu \approx 0.01 \tag{2.17}$$

corresponding to a maximum allowed dead-time of $100\,\mathrm{ns}$. However, faster systems demand higher power consumption, therefore other solutions are preferable. For instance, adding a memory block to store locally the data while waiting for read-out reduces significantly the channel dead-time. In fact, it is necessary that at least two events arrive in the considered time window of $10\,\mu\mathrm{s}$ for one to be lost, thus the loss probability becomes:

$$P_{loss} = 1 - P(0) - P(1) \approx 26\,\% \tag{2.18}$$

In general, with a memory block able to store N events in the channel, the probability of losing one hit becomes:

$$P_{loss} = 1 - \sum_{n=0}^{N} \mu^n \frac{\mathrm{e}^{-\mu}}{n!} \tag{2.19}$$

showing that in a system allowing the storage of $N = 4\,\mathrm{events}$ the probability of missing ones is $\approx 0.4\,\%$. This means that, after the buffers, the speed of the system can be tuned on the average arrival rate rather than on the maximum one. The random input data stream has thus been regularized or, in jargon, *derandomized*. So far, the hypothesis was that the busy time of the channel was the dominant source of inefficiency, but it can actually be any of the blocks building the front-end. On the other hand, the derandomization technique can be in principle applied to all of them using more elements in a time-interleaved configuration, so that when a unit is busy there is statistically at least another identical one free that can be used. However, in analog circuits with high gain, such as the input amplifier, the noise associated with the switching procedure can degrade the system performance, hence it is preferable to apply the derandomization to already amplified signals (i.e. after the preamplifier and the pulse shaper).

2.2 Time Invariant Shapers

As discussed in the previous section, the preamplifier and the shaper set the ultimate limits to the measurement quality, thus the factors affecting their performance must be properly understood. The easiest approach is to consider systems employing only linear, time invariant networks that can be comfortably studied with Laplace transforms.

In the first part of this section the subject will be the methods to achieve a given signal shape, the second part will be dedicated to noise calculations, and the last part will focus on the effects of non-idealities occurring in the building blocks of a front-end amplifier.

2.2.1 Ideal Charge Sensitive Amplifier

As described in section 2.1, most radiation sensors can be modelled as a current source with a capacitor in parallel (see I_d and C_d in figure 2.1). The input stage of the front-end must read the sensor current transforming it into a signal strong enough to drive the following circuitry. The first element of the processing chain must therefore be a transimpedance (current input, voltage output) or current (current input, current output) amplifier. A transimpedance amplifier can be realized by connecting an appropriate network in the feedback path of a high gain voltage amplifier. A multi-stage front-end often employs as the input stage the Charge Sensitive Amplifier (CSA) shown schematically in figure 2.6.

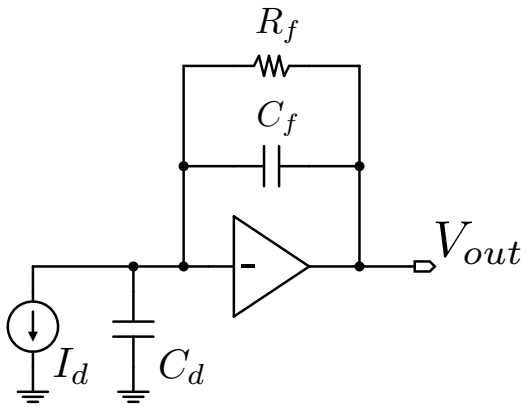


Figure 2.6: Charge sensitive amplifier (CSA).

A CSA is a form of transimpedance amplifier in which the feedback resistor, necessary to define the amplifier DC operating point, is big enough to give a minor and ideally negligible contribution to the signal processing. For the sake of simplicity, the transfer function of the circuit will be first studied under the assumptions presented in section 2.1. The CSA thus behaves as an ideal integrator and its output voltage is given by:

$$V_{out}(t) = \frac{1}{C_f} \int i(t)\, dt \tag{2.20}$$

which under the assumption of a δ-like stimulus becomes:

$$V_{out}(t) = \frac{Q_{in}}{C_f}\, u(t) \tag{2.21}$$

where $u(t)$ is the unit step function defined as:

$$\begin{cases} u(t) = 1 \ \text{ for } \ t \geq 0 \\ u(t) = 0 \ \text{ for } \ t < 0 \end{cases} \tag{2.22}$$

It is important to remember that since the idealized input signal for the front-end chain is a Dirac current pulse, the idealized input stimulus for the shaper is a voltage step with zero rise time.

2.2.2 The CR-RC Shaper

The simplest type of pulse shaper (shown in the dashed box of figure 2.7) consists of a cascade of an high and a low pass filter. The filters are isolated by a voltage buffer decoupling the two time constants, while the output buffer drives the load presented by the following stages to the front-end amplifier. Calling V_{CSA} the amplitude of the step delivered by the CSA, in the Laplace domain the signal at the output of the high pass filter can be written as:

$$V_{R_z}(s) = \frac{Q_{in}}{C_f}\, \frac{\tau_z}{(1 + s\tau_z)} \tag{2.23}$$

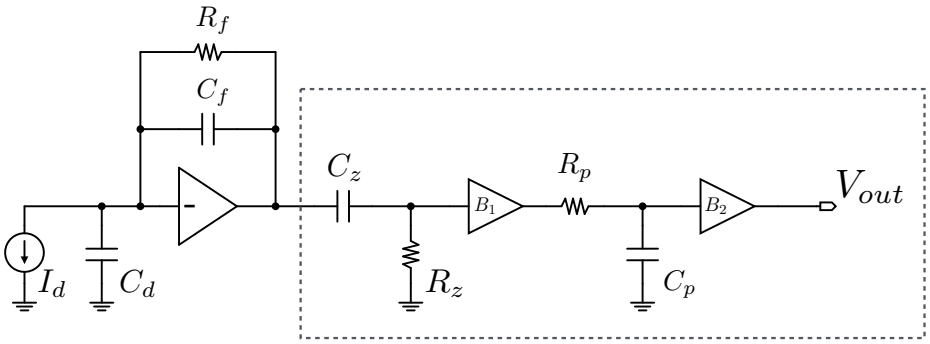


Figure 2.7: CSA followed by a CR-RC shaper. The shaper is the circuit included in the dashed box. The blocks indicated with "B" are voltage buffers.

where $\tau_z = R_z C_z$. Taking the inverse Laplace transform, the equation 2.23 in the time domain has the expression:

$$V_{R_z}(t) = \frac{Q_{in}}{C_f} \, \mathrm{e}^{-\frac{t}{\tau_z}} \tag{2.24}$$

The primary role of the high pass filter is to cut off the constant or slowly varying components of the CSA output, creating a signal that goes back to the baseline before the next pulse arrives. In many applications, the charge released in the sensor is extracted by capturing the peak height. However, the signal at the output of the high pass filter shown in figure 2.8 starts fading away immediately after its maximum value has been reached making it hard to sample. It is therefore preferable to treat signals having slower variations around the peak which can be obtained using a low pass filter. The second, and even more important, role is to optimize the signal-to-noise ratio, but this will be discussed in the following sections.

The complete transfer function of the circuit in figure 2.7 is:

$$V_{out}(s) = \frac{Q_{in}}{C_f} \, \frac{\tau_z}{(1 + s\tau_z)\left(1 + s\tau_p\right)} \tag{2.25}$$

Calculating the inverse Laplace transform, the signal representation in the time domain is:

$$V_{out}(t) = \frac{Q_{in}}{C_f} \, \frac{\tau_z}{\tau_z - \tau_p} \left(\mathrm{e}^{-\frac{t}{\tau_z}} - \mathrm{e}^{-\frac{t}{\tau_p}} \right) \tag{2.26}$$

which, of course, is valid only for $\tau_z \neq \tau_p$. For the particular case in which the two time constants are equal, the expression of the output signal in the Laplace domain becomes:

$$V_{out}(s) = \frac{Q_{in}}{C_f} \, \frac{\tau}{(1 + s\tau_z)^2} \tag{2.27}$$

while in the time domain it is:

$$V_{out}(t) = \frac{Q_{in}}{C_f} \, \frac{t}{\tau} \, \mathrm{e}^{-\frac{t}{\tau}} \tag{2.28}$$

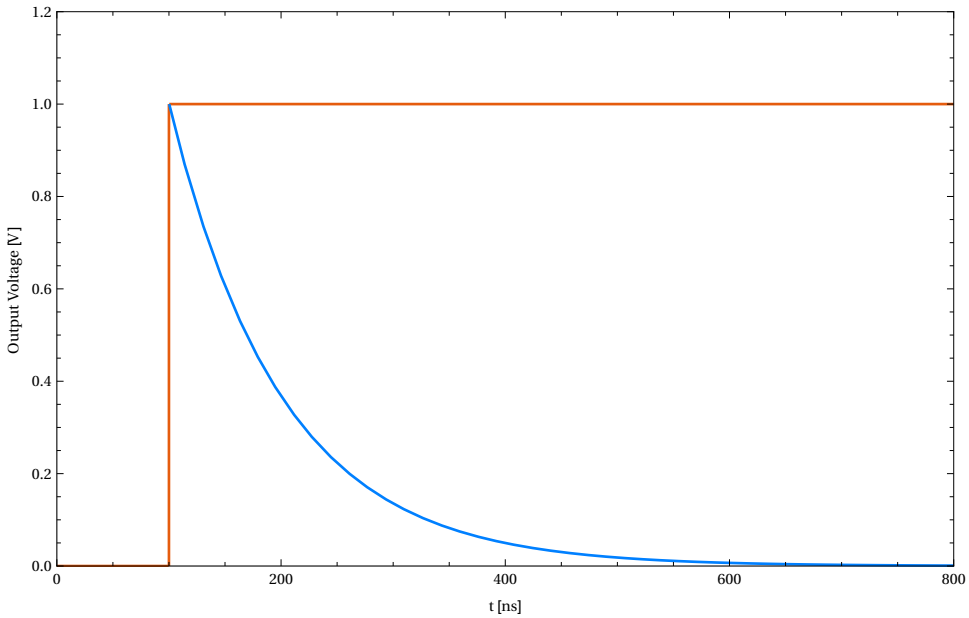


Figure 2.8: CSA (orange) and high pass filter (blue) output.

In the last two equations $\tau_z = \tau_p = \tau$. Equations 2.25-2.28 are valid assuming that the buffers have unity gain, otherwise a constant term $G = B_1 B_2$, multiplying the above mentioned expressions, should be added.

To understand the optimal choice of the two time constants, it is mandatory to study their effects on the shape of the output signal (see figure 2.9).

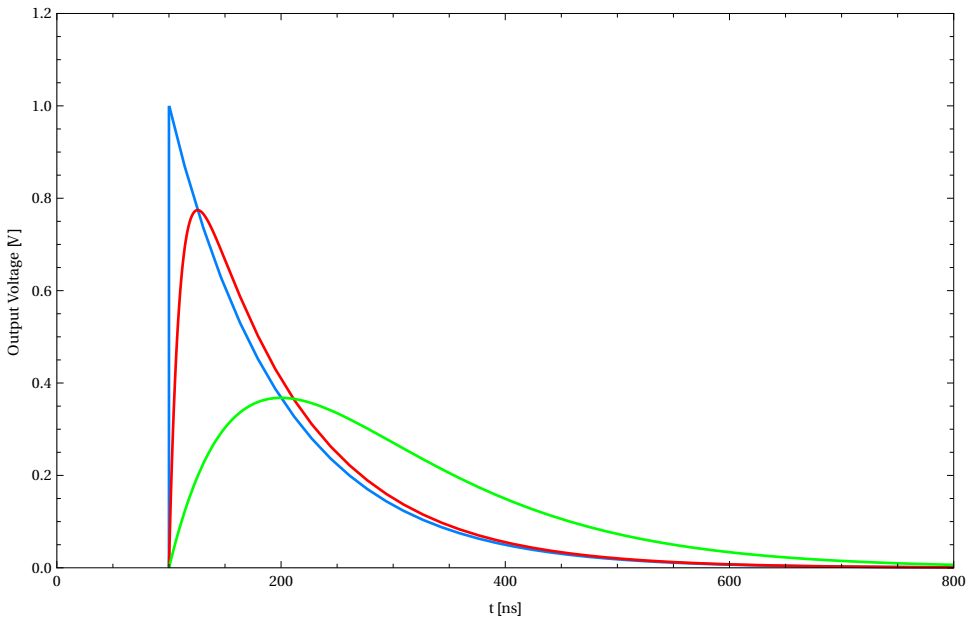


Figure 2.9: Effects of the integration time constant on the response of a CR-RC shaper. The derivation time constant is fixed $\tau_z = 100\,\mathrm{ns}$. The integration time constant τ_p assumes the values $0\,\mathrm{ns}$ (blue), $10\,\mathrm{ns}$ (red), and $100\,\mathrm{ns}$ (green), respectively.

In the plot, the derivation time constant τ_z is fixed, thus the increase of

τ_p produces a smoother signal with a smaller amplitude. Moreover, it can be observed that when τ_p becomes greater than τ_z it starts dominating the signal duration and for $\tau_p \gg \tau_z$, equation 2.26 can be approximated as:

$$V_{out}(t) \approx \frac{Q_{in}}{C_f} \frac{\tau_z}{\tau_p} \mathrm{e}^{-\frac{t}{\tau_p}} \tag{2.29}$$

and τ_p dominates the signal decay. In the plot of figure 2.10, the integration time constant is fixed while τ_z is varied.

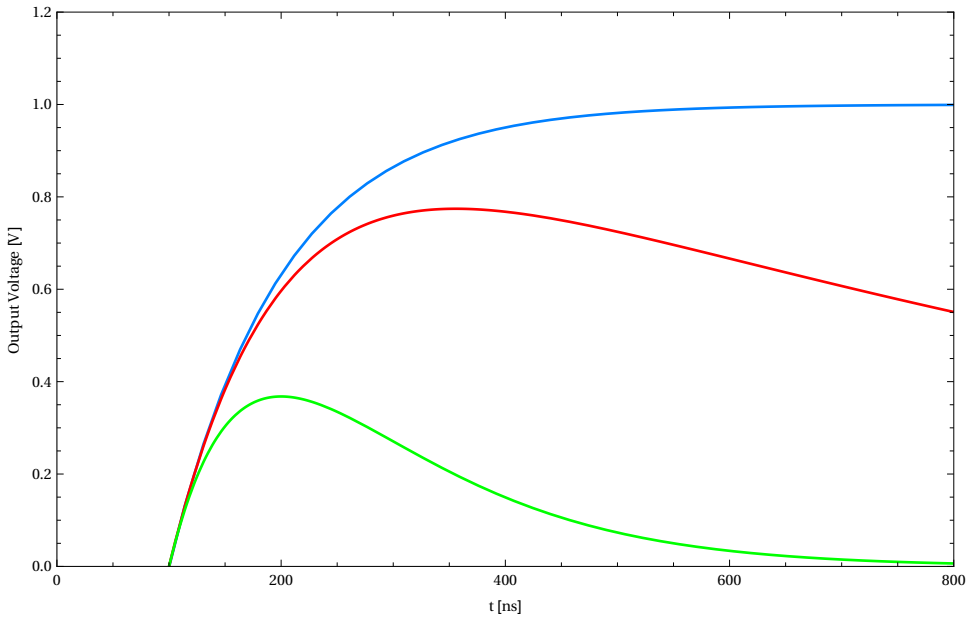


Figure 2.10: Effects of the derivation time constant on the response of a CR-RC shaper. The integration time constant is fixed $\tau_z = 100\,\mathrm{ns}$. The derivation time constant τ_z assumes the values ∞ (blue), $1\,\mu\mathrm{s}$ (red), and $100\,\mathrm{ns}$ (green), respectively.

An interesting case is when $\tau_z \to \infty$ and equation 2.26 can be approximated as:

$$V_{out}(t) \approx \frac{Q_{in}}{C_f} \left(1 - \mathrm{e}^{-\frac{t}{\tau_p}}\right) \tag{2.30}$$

In this scenario, there is no derivation time constant and the step at the preamplifier output is just low pass filtered by the integrator resulting in a smoother output signal with a $10\,\%$ to $90\,\%$ rise time of $2.2\tau_p$. When τ_z becomes smaller than τ_p, the amplitude of the signal is reduced because the slower time constant dominates the return to the baseline.

These considerations suggest that the best compromised is achieved with equal time constants as they maximize the signal amplitude for a given pulse duration. It is therefore interesting to study in more detail the case $\tau_z = \tau_p = \tau$. The peaking time of the output signal (equation 2.28) can be calculated as:

$$\frac{dV_{out}}{dt} = \frac{1}{\tau} \mathrm{e}^{-\frac{t}{\tau}} - \frac{t}{\tau^2} \mathrm{e}^{-\frac{t}{\tau}} = 0 \implies t_{max} \equiv T_p = \tau \tag{2.31}$$

and the magnitude of the peak is:

$$V(T_p) \equiv V_{out,max} = \frac{Q_{in}}{C_f}\frac{1}{\mathrm{e}} \tag{2.32}$$

A practical design of a CR-RC shaper is the one previously presented in figure 2.1 (transfer function presented in equation 2.2). The input signal undergoes several conversions between the current and the voltage domains propagating throughout the whole chain. A couple of differences can be noticed: no buffer is explicitly inserted to decouple the stages (the low output impedance of the core voltage amplifiers is rather exploited for this purpose); the high pass filtering capacitor C_z is not terminated over a resistor, but it is instead connected between the output of the CSA and the input of the second stage (which can be considered a virtual ground).

2.2.3 CR-RC^n Shapers

As discussed in section 2.1.3, to improve the noise performance it is advisable to have long peaking times (as long as permitted by the parallel noise). The effect of adding further integration stages is to increase the peaking time maintaining a restrained signal duration, thus it is of primary interest to study high order shapers. The number of integrators defines the order of the shaper. For the sake of simplicity, the following considerations are referred to integrators implemented with buffered low pass filters with unity gain (as in figure 2.7) and that the derivation and integration time constants have the same value. The transfer function of a generic CR-RC^n shaper contains $n+1$ poles, n introduced by the integrators and one by the differentiator, and in the Laplace domain can be written as:

$$V_{out}(s) = \frac{Q_{in}}{C_f}\frac{\tau}{(1+s\tau)^{n+1}} \tag{2.33}$$

which in the time domain becomes:

$$V_{out}(t) = \frac{Q_{in}}{C_f}\frac{1}{n!}\left(\frac{t}{\tau}\right)^n \mathrm{e}^{-\frac{t}{\tau}} \tag{2.34}$$

The peaking time can be calculated as:

$$\frac{dV_{out}}{dt} = \frac{Q_{in}}{C_f}\frac{1}{n!}\left[\frac{n}{\tau}\left(\frac{t}{\tau}\right)^{n-1}\mathrm{e}^{-\frac{t}{\tau}} - \left(\frac{t}{\tau}\right)^n \frac{1}{\tau}\mathrm{e}^{-\frac{t}{\tau}}\right] = 0 \implies T_p = n\tau \tag{2.35}$$

showing that in a CR-RC^n shaper the peaking time is given by the integration time constant multiplied by the number of integrators. The peak amplitude is:

$$V_{out,max} = \frac{Q_{in}}{C_f}\frac{n^n}{n!}\mathrm{e}^{-n} \tag{2.36}$$

Two interesting cases can be studied. The first one is to increase the number of integration stages without modifying the integration and derivation time constants and the result is shown in figure 2.11. The first important observation is that increasing the filter order leads to more symmetric

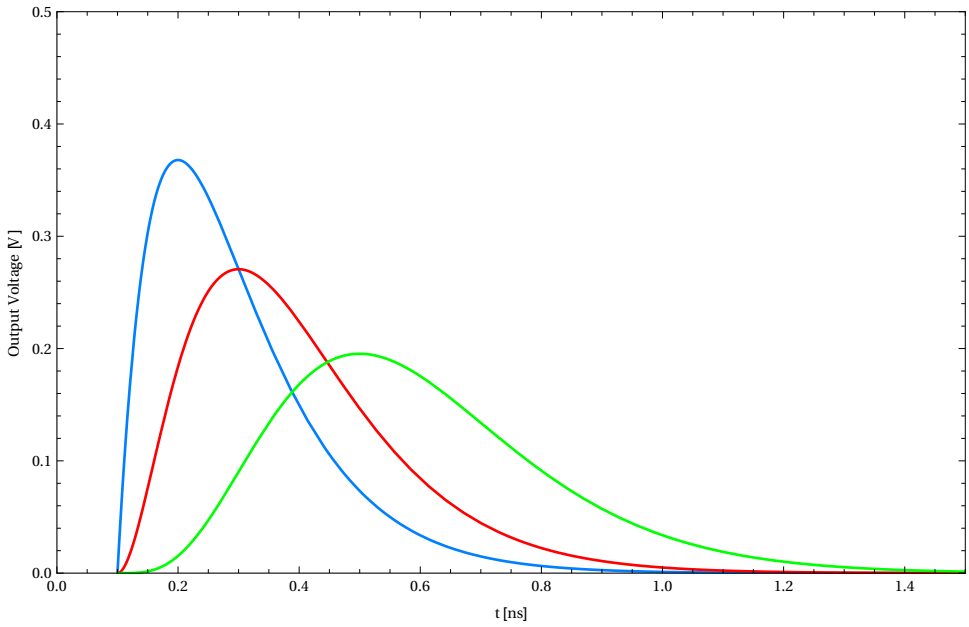


Figure 2.11: Outputs of CR-RC^n shapers of different orders with the same derivation and integration time constants fixed to $\tau = 100\,\mathrm{ns}$. The peaking times of the signals are: $T_p(1) = 100\,\mathrm{ns}$ (blue), $T_p(2) = 200\,\mathrm{ns}$ (red), and $T_p(4) = 400\,\mathrm{ns}$ (green).

signals. In fact, due to the similarity between their impulse response and a Gaussian waveform, CR-RC^n filters are commonly known as *Semi-Gaussian* shapers. It is important to highlight that the amplitude of the signal is more and more reduced as the order of the shaper is increased, but the amount of attenuation is less pronounced moving from a given order to the next. In fact, the relationship between the peak amplitudes of two shapers of generic order n and $n+1$ is:

$$\frac{V_{peak,n+1}}{V_{peak,n}} = \left(1 + \frac{1}{n}\right)^n \frac{1}{\mathrm{e}} \tag{2.37}$$

The limit for $n \to \infty$ is:

$$\lim_{n\to\infty} \left(1 + \frac{1}{n}\right)^n = \mathrm{e} \tag{2.38}$$

therefore the ratio defined in equation 2.37 is unitary for shapers of arbitrary high orders.

The second case of interest is to increase n without changing the peaking time. This means that as the number of integrators is increased, the value of the integration and derivation time constants must be reduced according to 2.35. To allow a better comparison between different pulse shapes, the amplitudes in figure 2.12 have been normalized to $1\,\mathrm{V}$. It is possible to observe that increasing the shaper order for the same peaking time leads to a faster return to the baseline making high order shapers a better choice for high rate applications.

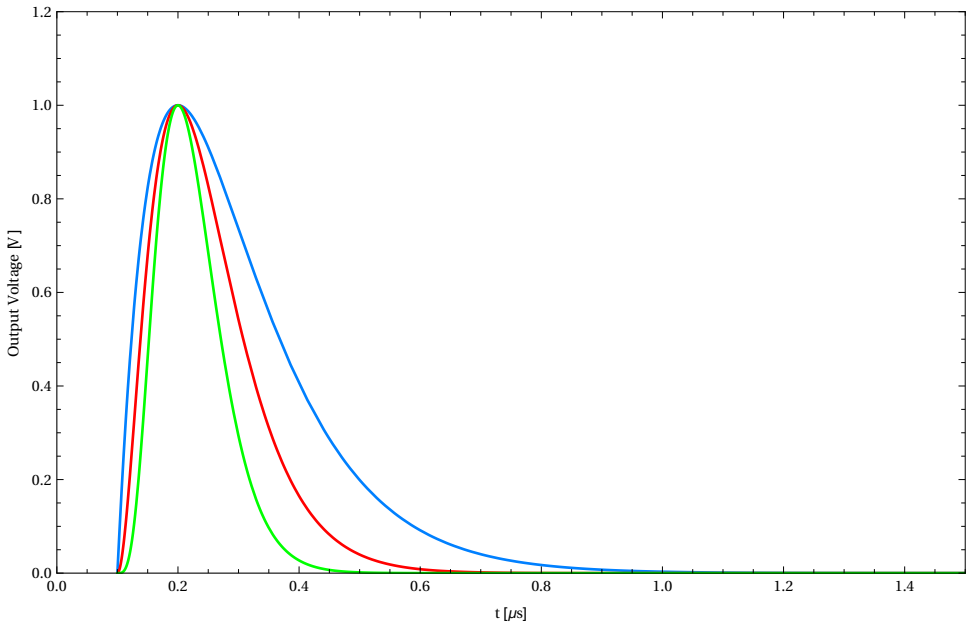


Figure 2.12: Outputs of CR-RC^n shapers of different orders with the same peaking time $T_p = 100\,\text{ns}$. The time constants of the shapers are: $\tau(1) = 100\,\text{ns}$ (blue), $\tau(2) = 200\,\text{ns}$ (red), and $\tau(4) = 400\,\text{ns}$ (green).

2.2.4 Pole-Zero Cancellation and Baseline Control

The assumption that the feedback resistor of the charge sensitive amplifier does not give any contribution to the signal shape is an over-simplification. In the following section, the effects of a finite feedback resistance R_f will be studied for CR-RC shapers, but the conclusions derived are qualitatively valid for shapers of any order. The introduction of the resistor yields to a feedback impedance of the CSA given by the parallel between R_F and $1/sC_f$:

$$Z_f = \frac{R_f}{1 + sR_fC_f} \tag{2.39}$$

and therefore the full transfer function of the front-end amplifier in the Laplace domain becomes:

$$V_{out}(s) = I_{in}(s)\,\frac{R_2}{R_c}\,\frac{R_f}{1 + s\tau_f}\,\frac{sR_1C_z}{(1 + s\tau_{sh})^2} \tag{2.40}$$

where $\tau_f = R_fC_f$ is the time constant associated to the feedback network of the CSA and $\tau_sh = R_1C_1 = R_2C_2$ is the shaping time constant. The above equation shows that the finite value of R_f has moved the pole in the CSA transfer function from the origin to a new value of s given by:

$$s_{CSA} = -\frac{1}{\tau_f} \tag{2.41}$$

An important consequence of this shift is that the pole of the CSA and the one of the differentiator do not cancel each other out any longer. Both effects can be easily seen considering the Bode plots of the CSA and of the full amplifier. In the plot in figure 2.13, it can be observed that the CSA

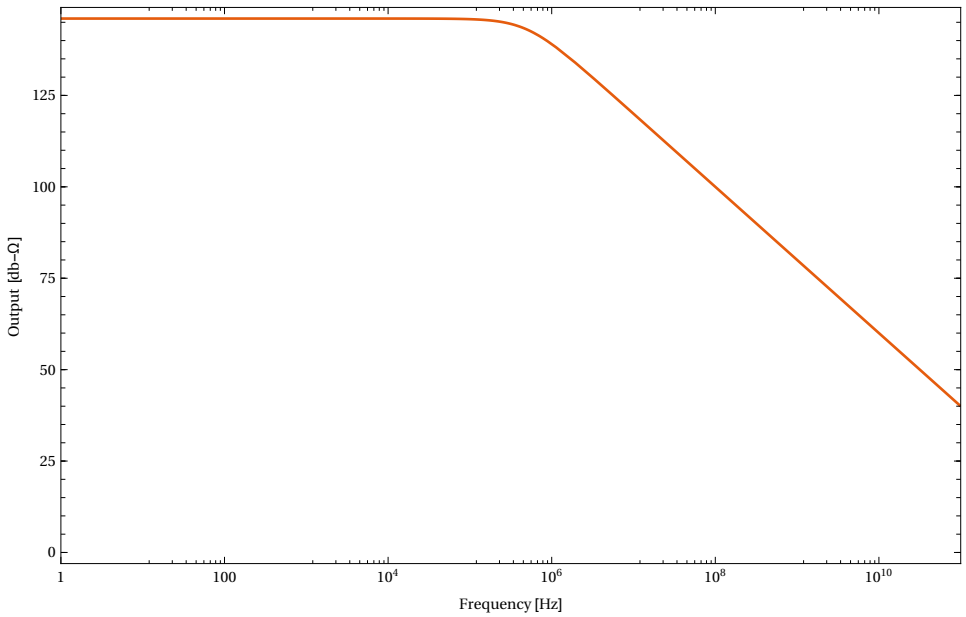


Figure 2.13: Bode plot of a CSA with finite feedback resistor.

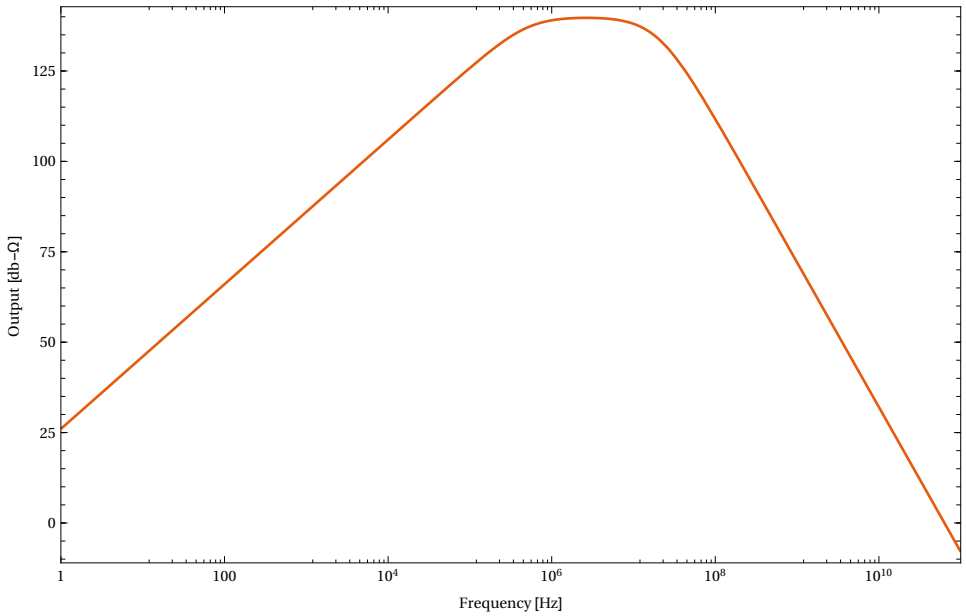


Figure 2.14: Bode plot of a CR-RC shaper with finite feedback resistor in the CSA.

has a first order low pass filter behaviour with a cut-off frequency $f_{CSA} = 1/2\pi\tau_f \approx 80\,\mathrm{kHz}$ after which the gain drops with a slope of $20\,\mathrm{dB/decade}$. In the plot in figure 2.14, without the pole-zero cancellation due to the finite value of the feedback resistor R_f, a zero is left in the origin and the gain of the full amplifier rises with a slope of $20\,\mathrm{dB/decade}$. When the CSA pole is found, the effect of the zero is cancelled and the gain remains constant until the roll-off of $40\,\mathrm{dB/decade}$ introduced by the double pole at the frequency $f_{sh} = 1/2\pi\tau_{sh} \approx 3.2\,\mathrm{MHz}$. In other words, the front-end amplifier becomes a band-pass filter. The cut-off of the lower portion of the frequency spectrum has several advantages as the impact of the DC and slow variations occurring in the CSA are suppressed, but it has also potential undesired consequences on the signal shape. To understand this point, it is helpful to study the inverse Laplace transform of equation 2.40 under the hypothesis of a δ-like input pulse:

$$V_{out}(t) = Q_{in}\left[\frac{R_1R_2R_fC_z}{R_c\tau_{sh}\left(\tau_f-\tau_{sh}\right)}\left(\frac{t}{\tau_{sh}}\right)\mathrm{e}^{-\frac{t}{\tau_{sh}}} + \frac{R_1R_2R_fC_z}{R_c\left(\tau_f-\tau_{sh}\right)^2}\left(\mathrm{e}^{-\frac{t}{\tau_{sh}}}-\mathrm{e}^{-\frac{t}{\tau_f}}\right)\right] \tag{2.42}$$

Isolating the terms multiplying the exponentials in the above equation, the result is:

$$V_{out}(t) = A\,\mathrm{e}^{-\frac{t}{\tau_{sh}}} + B\,\mathrm{e}^{-\frac{t}{\tau_f}} \tag{2.43}$$

where the term A is given by:

$$A = Q_{in}\,\frac{R_1R_2R_fC_z}{R_c}\,\frac{1}{\left(\tau_f-\tau_{sh}\right)^2}\left[\left(\frac{\tau_f}{\tau_{sh}}-1\right)\,\frac{t}{\tau_{sh}}+1\right] \tag{2.44}$$

Since $\tau_f \gg \tau_{sh}$, some approximations yield to:

$$A \approx Q_{in}\,\frac{R_1R_2R_fC_z}{R_c}\,\frac{1}{\tau_f\tau_{sh}}\left(\frac{t}{\tau_{sh}}\right) \tag{2.45}$$

and substituting the time constants with the respective resistors and capacitances, the final result is:

$$A \approx Q_{in}\,\frac{C_z}{C_f}\,\frac{R_2}{R_cC_1}\,\frac{t}{\tau_{sh}} \tag{2.46}$$

which is the term multiplying the exponential $\mathrm{e}^{-\frac{t}{\tau_{sh}}}$ on equation 2.2, meaning that the signal component $B\,\mathrm{e}^{-\frac{t}{\tau_f}}$ of equation 2.42 is subtracted to the "main" signal shown in figure 2.2. The resulting impulse response is represented in figure 2.15. The waveform goes below the baseline before returning to the quiescent point in a time scale defined by the CSA time constant τ_f. This negative tail, called *undershoot*, extends significantly the signal duration, reducing the rate capability of the system. The presence of the undershoot stems from the fact that an unipolar pulse (the output of the CSA) is fed to a network (the shaper) containing a capacitor in series. This capacitor blocks any DC component coming from the first stage, so the CSA signal cannot modify the DC level at the output of the shaper. As

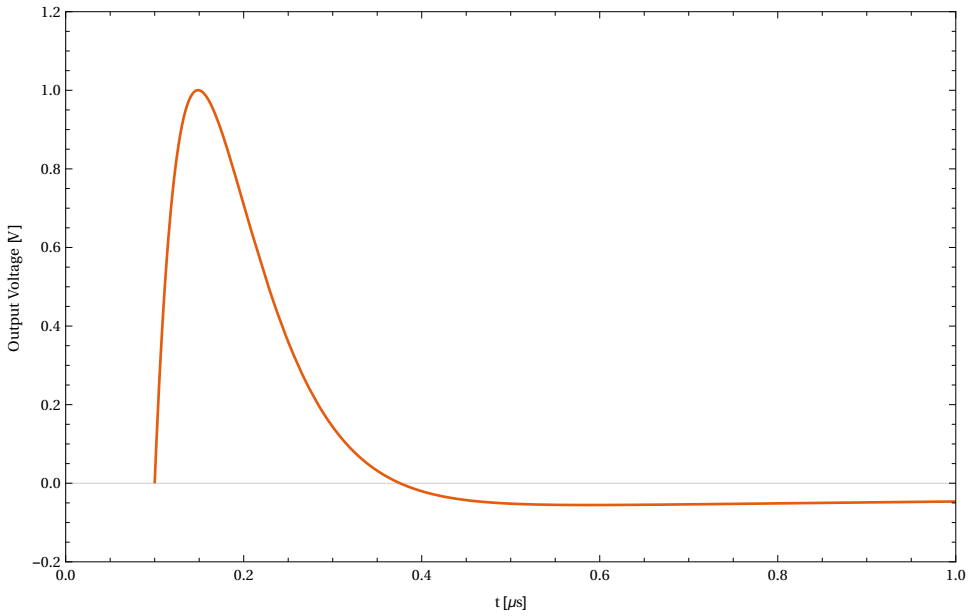


Figure 2.15: CR-RC impulse response with finite CSA feedback resistance.

a consequence, the shaper response can not be purely unipolar, but must have a bipolar nature, so that the net signal contribution to the output DC value is zero. The most important effect of the undershoot is the baseline drift at high rates: the quiescent point drifts downwards till the new level that yields a zero average value of the output is reached. When the interval between pulses is not uniform (such as for radiation sensors), the baseline fluctuates up and down rather than reaching a stable value leading to a significant performance degradation. Before studying the solutions to this problem, it is interesting to observe that there is a trade-off between the undershoot duration and its amplitude. In fact, the term B of equation 2.43, under the same hypothesis made to obtain A, can be written as:

$$B = -Q_{in}\frac{R_1R_2R_fC_z}{R_c}\frac{1}{\left(\tau_f-\tau_{sh}\right)^2} \approx -Q_{in}\frac{C_z}{C_f}\frac{R_2}{R_cC_1}\frac{\tau_{sh}}{\tau_f} \tag{2.47}$$

Therefore, the undershoot tail can be written as:

$$V_u(t) = -Q_{in}\frac{C_z}{C_f}\frac{R_2}{R_cC_1}\frac{\tau_{sh}}{\tau_f}\,\mathrm{e}^{-\frac{t}{\tau_f}} \tag{2.48}$$

showing that increasing the time constant in the CSA feedback reduces the undershoot amplitude, but extends its duration.

2.2.4.1 Pole-Zero Cancellation

To address the baseline drift issue, a very common approach is to shift the position of the zero introduced by C_z so that its frequency matches again exactly the one of the CSA pole. This is achieved with the introduction of

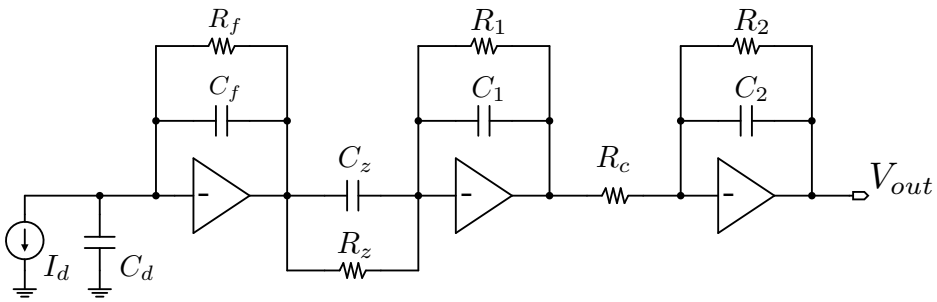


Figure 2.16: Front-end with pole-zero cancellation.

an extra resistor R_z in parallel to C_z. The transfer function of the resulting circuit (see figure 2.16) is the following:

$$V_{out}(s) = I_{in}(s)\,\frac{R_f}{1+s\tau_f}\,\frac{1+s\tau_z}{R_z}\,\frac{R_1R_2}{R_c\,(1+s\tau_{sh})^2} \tag{2.49}$$

where $\tau_z = R_zC_z$. If R_Z is chosen so that $\tau_z = \tau_f$, the transfer function can be simplified as:

$$V_{out}(s) = I_{in}(s)\,\frac{R_f}{R_z}\,\frac{R_1R_2}{R_c\,(1+s\tau_{sh})^2} = I_{in}(s)\,\frac{C_z}{C_f}\,\frac{R_1R_2}{R_c\,(1+s\tau_{sh})^2} \tag{2.50}$$

which is the same obtained in the case of infinite CSA feedback resistor. The Bode plot obtained from such a system is shown in figure 2.17. The circuit has a strict low pass filter behaviour, so it amplifies any signal starting from DC. The impulse response in the time domain is given by:

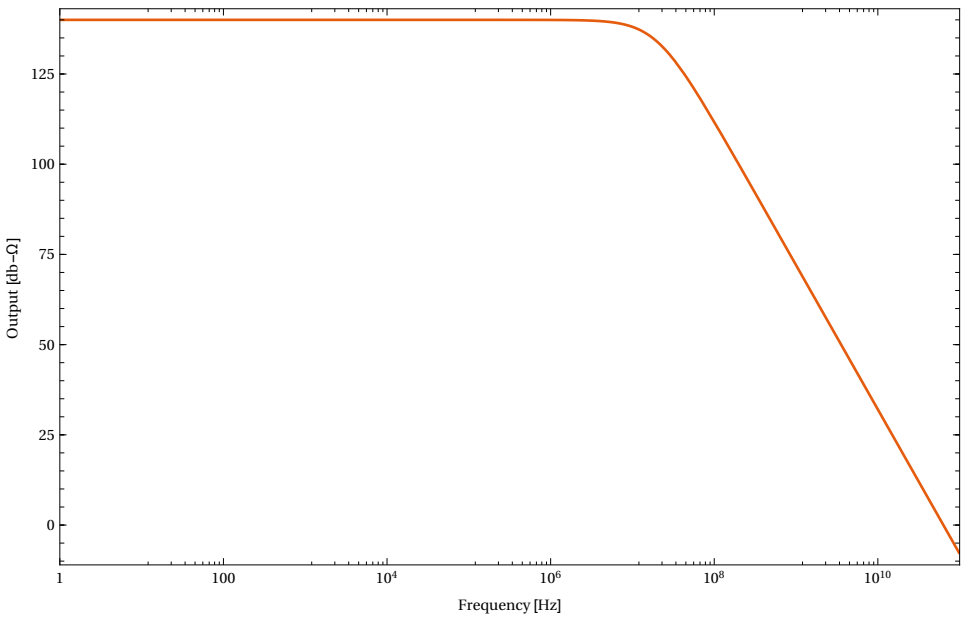


Figure 2.17: Bode plot of a front-end with pole-zero cancellation.

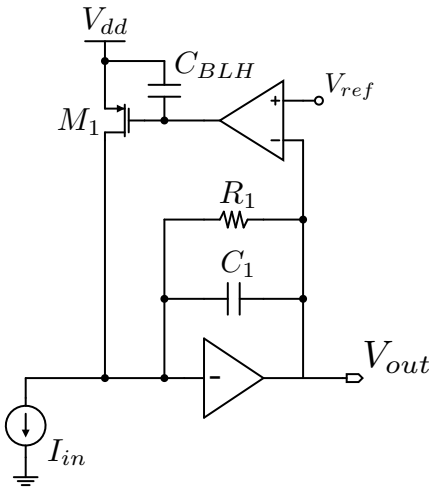


Figure 2.18: Baseline holder principle.

$$V_{out}(t) = Q_{in}\,\frac{R_f}{R_z}\,\frac{R_1 R_2}{R_c \tau_{sh}}\mathrm{e}^{-\frac{t}{\tau_{sh}}} = Q_{in}\,\frac{C_z}{C_f}\,\frac{R_2}{R_c C_1}\,\frac{\tau_f}{\tau_z}\mathrm{e}^{-\frac{t}{\tau_{sh}}} \tag{2.51}$$

and, again, since $\tau_z = \tau_f$, the expression of the signal in the time domain is the same as in equation 2.2. The above expression confirms that there is no undershoot in the output signal, hence no baseline drift should be expected.

2.2.4.2 Baseline Holders

The drawback of the pole-zero cancellation described so far is that it makes the circuit sensitive to DC or low frequency variations. Therefore, techniques more elaborate than a single blocking capacitor are required. One possible approach is the baseline holder shown in figure 2.18 (an alternative architecture to compensate a current entering the input node foresees an NMOS transistor instead of a PMOS). In absence of the additional feedback network formed by the differential amplifier A_2 and transistor M_1, a current sunk from the input node would flow through R_1 increasing the output voltage. The quantity $V_{ref} - V_{out}$ is however sensed and amplified by A_2 decreasing the voltage at the gate of M_1. The transistor pumps current into the input node locking the DC level of the output voltage to the reference voltage fed to the differential amplifier, provided that the loop gain is high enough. The differential amplifier and the transistor can be considered as a single transconductance amplifier, with $G_m = g_{m1} A_{d2}$ where g_{m1} is the transconductance of M_1 and A_{d2} is the differential voltage gain of A_2. For a better comprehension of the process described, the assumption that A_2 has a single pole transfer function is made:

$$A_{d2} = \frac{A_{d2_0}}{1 + s\tau_L} \tag{2.52}$$

The capacitor C_{BLH} has the purpose of keeping the bandwidth of the differential stage small enough so that the additional feedback loop processes only low-frequency signals. The transconductance G_m can be written as:

$$G_m = \frac{A_{d2_0} g_{m1}}{1 + s\tau_L} = \frac{G_{m0}}{1 + s\tau_L} \tag{2.53}$$

where G_{m0} is the low-frequency overall transconductance. The hypothesis that $\tau_L \gg \tau_1 = R_1 C_1$ allows to consider only the resistive part of the feedback impedance of the main amplifier A_1. Writing the equation for the input node the result is:

$$I_{in} + \frac{V_{in} - V_{out}}{R_1} - I(M_1) = 0 \implies I_{in} = I(M_1) - \frac{V_{in} - V_{out}}{R_1} \tag{2.54}$$

where the contribution of the feedback capacitance C_1 has been neglected. If the input node of A_1 is treated as a virtual ground (i.e. assuming that $V_{in} = 0$), the small signal current flowing in M_1 can be written as:

$$I(M_1) = G_m V_{out} \tag{2.55}$$

and thus the expression of the gain is:

$$\frac{V_{out}}{I_{in}} = \frac{R_1}{1 + G_m R_1} = \frac{R_1}{1 + G_{m0} R_1} \frac{1 + s\tau_L}{1 + s\frac{\tau_L}{1 + G_{m0} R_1}} \tag{2.56}$$

At low frequency ($s = 0$), the transimpedance gain becomes:

$$\frac{V_{out}}{I_{in}} = \frac{R_1}{1 + G_{m0} R_1} \tag{2.57}$$

As the frequency rises, the zero is found at $f_L = 1/2\pi\tau_L$ and the gain rises with a $20\,\mathrm{dB/decade}$ slope till the pole is met at the frequency $1 + G_{m0}R_1$. Above the pole frequency, the gain can be approximated as:

$$\frac{V_{out}}{I_{in}} \approx \frac{R_1}{G_{m0} R_1} \frac{s\tau_L}{\frac{s\tau_L}{G_{m0} R_1}} = R_1 \tag{2.58}$$

where the condition $G_{m0}R_1 \gg 1$ has also been used. This separation in frequency is important because the G_m feedback must only compensate undesired DC or close to DC components.

In the more realistic case in which the feedback capacitance C_1 is taken into account, the baseline holder transfer function can be rewritten as:

$$\frac{V_{out}}{I_{in}} = \frac{R_1 \left(1 + s\tau_L\right)}{\tau_1 \tau_L s^2 + \left(\tau_1 + \tau_L\right) s + 1 + G_{m0} R_1} \tag{2.59}$$

Thus, considering C_1 a second order transfer function, potentially containing complex conjugate poles, is obtained. To avoid complex conjugate roots, the requirement is that:

$$\left(\tau_L + \tau_1\right)^2 > 4\tau_1 \tau_L \left(1 + G_{m0} R_1\right) \tag{2.60}$$

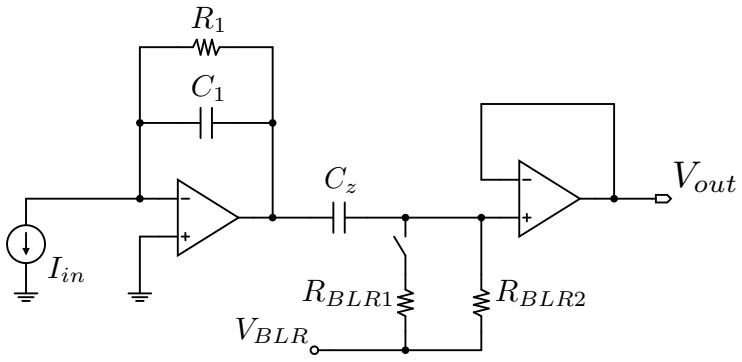


Figure 2.19: Conceptual scheme of a baseline restorer.

which, supposing that $\tau_L \gg \tau_1$ and $G_{m0}R_1 \gg 1$, can be approximated as:

$$\tau_L > 4\tau_1 G_{m0} R_1 \tag{2.61}$$

showing the connection between the low frequency time constant, the shaping time constant, and the loop gain. The above equation reveals that an excessive loop gain may lead to instability. If the current in M_1 increases so does its transconductance and thus the loop gain, hence the stability of a baseline holder must be checked for the maximum current that it is expected to compensate.

2.2.4.3 Baseline Restorers

An alternative method to the baseline holder is the baseline restorer, which is a time variant circuit. The concept is shown in figure 2.19. The first stage represents a generic chain delivering unipolar pulses. Resistor R_{BLR1} establishes a DC path from the reference voltage V_{BLR} to the input of the buffer. The switch must be open when the signal arrives. If the time constant $R_{BLR1}C_z$ is much bigger than the pulse peaking time, a single pulse is passed over the capacitor with a minimal undershoot. However, without the switch and the resistor R_{BLR2}, the circuit is a simple high pass filter and the baseline drift would occur at high rates, therefore, after the pulse, the switch is closed to avoid the problem. The condition $R_{BLR2} \ll R_{BLR1}$ is necessary to allow a quick recovery, controlled by the time constant $R_{BLR2}C_z$, of the baseline to the reference level V_{BLR}. The switch is then open again before the next pulse arrives. The baseline restorer described can therefore be seen as the combination of two high pass filters: one with long time constant, which gives a small undershoot but a long recovery time; and another with a short time constant, which offers short recovery time but bigger undershoot and visible differentiation of the signal. The baseline restoration circuit is made active only at selected times by switches, hence the name of *gated baseline restorer*. Alternatively, the switch can be replaced by a non-linear component allowing unidirectional current flow, so that it becomes active only when the buffer input goes below the reference voltage.

2.2.5 Gain and Bandwidth Limitations in CSAs

The gain and bandwidth limitations of the core stages used in the implementation of the front-end described so far must be considered. In particular, they are extremely important for the charge sensitive amplifier since it is the stage providing the direct interface to the sensor.

2.2.5.1 Effects of Finite Gain in the CSA

The first step to study the properties of a non-ideal CSA is to use a core amplifier with finite gain A_0 but still infinite bandwidth. The nodal equation for the input of the circuit shown in figure 2.6 is the following:

$$I_{in}(s) + V_{in} s C_T + (V_{in} - V_{out})\, s C_f = 0 \tag{2.62}$$

Writing $V_{in} = -V_{out}/A_0$ and solving for V_{out}/I_{in} the result is:

$$\frac{V_{out}}{I_{in}} = -\frac{A_0}{s\left[C_T + (1 + A_0)\, C_f\right]} \tag{2.63}$$

To find again the result obtained in the ideal case ($V_{out}/I_{in} = 1/sC_f$), the gain of the amplifier should not only be much above unity (i.e. $A_0 \gg 1$), but the feedback capacitance multiplied by the open-loop gain must be much greater than the total capacitance seen between the amplifier input and ground (i.e. $(1 + A_0)\, C_f \gg C_T$). This can be understood using the Miller theorem, which represents the term $(1 + A_0)\, C_f$ as a capacitance in parallel to C_T. The sum of the charges accumulated by the two capacitances must be equal to the one contained in the input signal (i.e. $Q_{in} = Q_T + Q_f = V_{in} C_T + V_{in}\,(1 + A_0)\, C_f$). However, only Q_f, being physically stored in C_f, contributes to the output signal, while the rest is lost to further processing. The problem is even more serious because in multichannel sensors, at least a fraction of the sensor capacitance stems from the coupling between neighbouring channels. The lower the amplifier gain, the higher the swing of the input voltage will be, coupling part of the signal to the adjacent channels as cross-talk. This shows that it is mandatory to prevent the CSA from saturating, because in this case the gain drops and the charge is directly integrated on the input node, rising significantly the input voltage and exacerbating the cross-talk.

2.2.5.2 Effects of Bandwidth Limitation

To understand the effects of bandwidth limitation in CSAs, a simple transistor can be considered as core amplifier. The small signal equivalent model of such a CSA is shown in figure 2.20. The transfer function is obtained solving the following system neglecting, in a first order approximation, the feedback resistor R_f:

$$\begin{cases} I_{in}(s) + V_{in} s C_T + (V_{in} - V_{out})\, s C_f = 0 \\ g_m V_{in} + (V_{out} - V_{in})\, s C_f + V_{out}\left(\frac{1}{R_L} + s C_L\right) = 0 \end{cases} \tag{2.64}$$

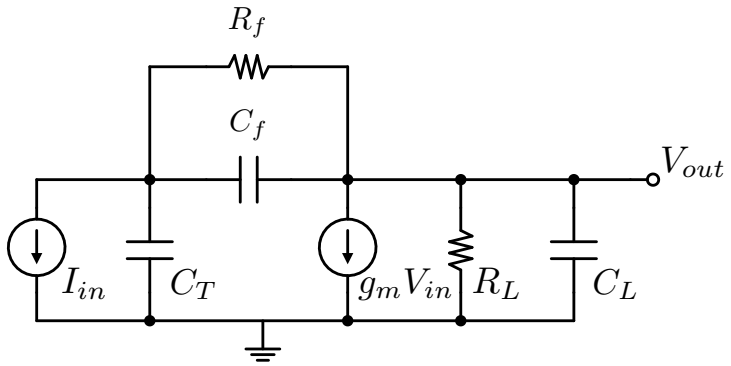


Figure 2.20: Small signal equivalent circuit of a CSA.

where R_L and C_L are the equivalent load resistor and capacitor, respectively. Considering the case with $R_L \to \infty$, the resulting transfer function is:

$$V_{out}(s) = -\frac{I_{in}(s)\left(1 - s\frac{C_f}{g_m}\right)}{(1 + sT_r)\, sC_f} \tag{2.65}$$

where

$$T_r = \frac{C_L C_T + (C_L + C_T)\, C_f}{g_m C_f} \tag{2.66}$$

is the rise time constant. The response to a δ-like input current in the time domain is given by:

$$V_{out}(t) = -\frac{Q_{in}}{C_f}\left(1 - \mathrm{e}^{-\frac{t}{T_r}}\right) \tag{2.67}$$

The effects of bandwidth limitation can be better understood studying two different cases:

1. $C_f \gg C_L$
   The rise time can be approximated as:

   $$T_r \approx \frac{C_L + C_T}{g_m} \tag{2.68}$$

   which can be further simplified under the hypothesis of $C_T \gg C_L$:

   $$T_r \approx \frac{C_T}{g_m} \tag{2.69}$$

   The speed of the signal depends weakly from the value of the feedback capacitance C_f and mainly depends on the input capacitance C_T.

2. $C_f \ll C_L$
   In this case, the rise time is:

$$T_r \approx \frac{C_L C_T}{g_m C_f} \tag{2.70}$$

   hence the speed of the signal is limited by the ratio C_T/C_f.

For both cases it can be observed that limiting the CSA bandwidth leads to an output signal different from the ideal voltage step reaching the value Q_{in}/C_f in a null time, but it gets instead a time T_r to get to that level. In a more realistic case, the feedback resistor R_f must be considered and the resulting transfer function is:

$$V_{out}(s) = \frac{I_{in}(s) R_f}{(1 + s\tau_f)(1 + sT_r)} \tag{2.71}$$

valid under the assumption that

$$\tau_f = R_f C_f \gg \frac{C_L + C_T}{g_m} \tag{2.72}$$

The pulse response in the time domain is then:

$$V_{out}(t) = \frac{Q_{in}}{C_f} \frac{\tau_f}{T_r - \tau_f} \left(\mathrm{e}^{-\frac{t}{T_r}} - \mathrm{e}^{-\frac{t}{\tau_f}} \right) \tag{2.73}$$

The peaking time is given by:

$$T_p = \frac{T_r \tau_f}{T_r - \tau_f} ln \left(\frac{T_r}{\tau_f} \right) \tag{2.74}$$

and the resulting amplitude is therefore:

$$V_{out,max} = \frac{Q_{in}}{C_f} \left(\frac{T_r}{\tau_f} \right)^{\frac{T_r}{T_r - \tau_f}} \tag{2.75}$$

So the step amplitude is modulated by a term depending on the ratio between the feedback time constant τ_f and the signal rise time T_r. This amplitude loss is another example of ballistic deficit, but in this case it is the finite bandwidth of the CSA that limits the signal formation time rather than the detector.

2.3 Noise Calculations

The purpose of this section is to show how to calculate the equivalent noise charge of a front-end amplifier. As discussed in section 2.1.3, the first step is to identify the relevant noise generators and represent them as current (parallel noise) or voltage (series noise) sources properly connected to the input (see figure 2.21). The capacitor C_T is given by the sum of any capacitance seen between the amplifier input and ground, including the sensor capacitance and the gate capacitance of the input device. In the frequency domain, a power spectral density, S_n, is associated to each noise source and its effect on the amplifier is calculated by integrating over the whole frequency spectrum its product with the modulus square of the appropriate

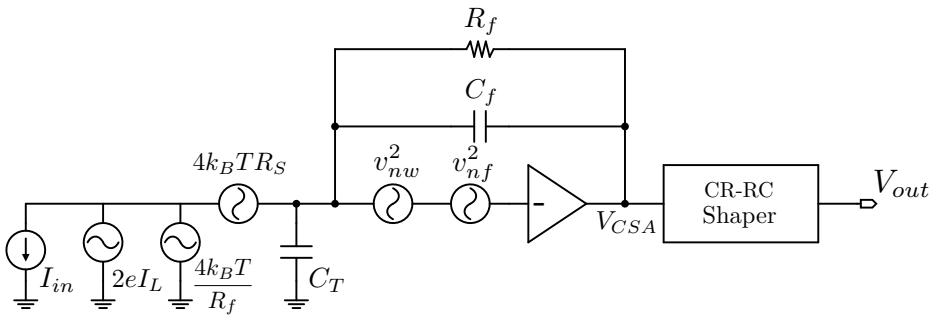


Figure 2.21: Noise sources in a front-end amplifier.

transfer function. The quantity thus obtained is the power of the output waveform generated by the considered noise source and, in the case of interest, it coincides with the variance of the output signal corrupted by noise:

$$\langle v_{out}^2 \rangle = \frac{1}{2\pi} \int_0^\infty S_n^2 \left| T_n(j\omega) \right|^2 d\omega \tag{2.76}$$

where $\omega = 2\pi f$ is the angular frequency. It is important to underline that $T_n(j\omega)$ is the transfer function from the particular noise source to the output and it might or might not coincide with the signal transfer function. If more uncorrelated noise source are involved, all the square contributions are assumed at the output:

$$\langle v_{out,tot} \rangle = \langle v_{out1}^2 \rangle + \langle v_{out2}^2 \rangle + \cdots + \langle v_{outn}^2 \rangle \tag{2.77}$$

The square root of the above expression gives the output rms noise:

$$v_{out,tot}^2 = \sqrt{\langle v_{out1}^2 \rangle + \langle v_{out2}^2 \rangle + \cdots + \langle v_{outn}^2 \rangle} \tag{2.78}$$

The ENC is obtained dividing the rms output noise by the peak amplitude of the signal generated by a Dirac delta pulse containing a single electron:

$$ENC = \frac{\langle v_{out} \rangle}{V_{out,peak}(Q_{in} = e)} \tag{2.79}$$

In a well designed amplifier, the noise should be dominated by the one of the input stage, which operates on weak signals. However, this does not mean that the noise introduced by the shaper itself can be neglected a priori.

2.3.1 Noise in CR-RC Shapers

The first step is to evaluate the effects of the white series noise, represented by the voltage source v_{nw}^2. The noise voltage is converted into a current by the capacitance C_T and it is then integrated on C_f, so it can be expressed as:

$$v_{nw,CSA}^2 = v_{nw}^2 \left| \frac{C_T}{C_f} \right|^2 \tag{2.80}$$

The output noise of the CSA is then processed by the transfer function of the pulse shaper, which, for a CR-RC shaper, is:

$$T(s) = \frac{s\tau}{(1+s\tau)^2} \tag{2.81}$$

The aim is to calculate the ENC and any gain would affect equally both the signal and the noise, therefore the assumption that the shaper does not introduce gain is made. As shown in equation 2.76, an integration in the frequency domain is needed, thus the transfer function of the shaper can be rewritten as:

$$T(j\omega) = \frac{j\frac{\omega}{\omega_0}}{1+j\frac{\omega}{\omega_0}} \tag{2.82}$$

where ω_0 is the pole angular frequency, i.e. $\omega_0 = 1/\tau$. The noise output voltage is given by:

$$\langle v_{out}^2 \rangle_{nw} = \frac{v_{nw}^2}{2\pi} \int_0^\infty \left|\frac{C_T}{C_f}\right|^2 |T(j\omega)|^2 \, d\omega \tag{2.83}$$

Introducing the expression of the modulus squared of the transfer function, the result is:

$$\langle v_{out}^2 \rangle_{nw} = \frac{v_{nw}^2}{2\pi} \left(\frac{C_T}{C_f}\right)^2 \int_0^\infty \frac{\omega^2}{\left(\omega_0 - \frac{\omega^2}{\omega_0}\right)^2 + 4\omega^2} d\omega = v_{nw}^2 \left(\frac{C_T}{C_f}\right)^2 \frac{\omega_0}{8} \tag{2.84}$$

The above quantity can also be rewritten as:

$$\langle v_{out}^2 \rangle_{nw} = v_{nw}^2 \left(\frac{C_T}{C_f}\right)^2 \frac{1}{8T_p} \tag{2.85}$$

where it has been used the relationship $\tau = T_p$. Using equation 2.28, the peak output voltage for an input signal of one electron is:

$$V_{out,peak} = \frac{e}{C_f} \frac{1}{\mathrm{e}} \tag{2.86}$$

Finally, using the equation 2.79, the result is:

$$ENC_w = \frac{\mathrm{e}}{e} C_T \sqrt{\frac{v_{nw}^2}{8T_p}} \tag{2.87}$$

The above relationship shows that the ENC due to series white noise increases linearly with the total capacitance shunting the amplifier input and decreases with the square root of the peaking time.

The contribution of the flicker noise can be written as:

$$v_{nf}^2 = \frac{K_f}{C_{ox}WL} \frac{1}{f} = \frac{A_f}{f} \tag{2.88}$$

Thus, the voltage produced at the CSA output becomes:

$$v_{nf,CSA}^2 = \frac{A_f}{f}\left|\frac{C_T}{C_f}\right|^2 \tag{2.89}$$

Following the same procedures done for the white series noise, the final result is:

$$ENC_f = \frac{\mathrm{e}}{e} C_T \sqrt{\frac{A_f}{2}} \tag{2.90}$$

Therefore, the equivalent noise charge due to flicker noise is proportional to the total input capacitance (as for the white series noise), but it is independent of the peaking time.

The last evaluation regards the parallel noise. At the output of the CSA, the noise due to the current generator i_n^2 is given by:

$$v_{ni,CSA}^2 = i_n^2\left|\frac{1}{j\omega C_f}\right|^2 = \left(\frac{i_n}{\omega C_f}\right)^2 \tag{2.91}$$

Processing the noise with the shaper transfer function, the result leads to:

$$ENC_i = \frac{\mathrm{e}}{e}\sqrt{\frac{i_n^2}{8}T_p} \tag{2.92}$$

The above equation reveals that the effect of the parallel noise is independent of the input capacitance and is proportional to the square root of the peaking time. Finally, the total output noise introduced with equation 2.9 is obtained by summing up the squares of all contributions:

$$ENC = \sqrt{ENC_w^2 + ENC_f^2 + ENC_i^2} = \frac{\mathrm{e}}{e}\sqrt{C_T^2\left(\frac{v_{nw}^2}{8T_p} + \frac{A_f}{2}\right) + \frac{i_n^2}{8}T_p} \tag{2.93}$$

Considering that the peaking time weights in opposite ways white series and parallel noise, an optimal T_p can be found solving the following equation:

$$\frac{\partial ENC^2}{\partial T_p} = \frac{\mathrm{e}^2}{8e^2}\left(-v_{nw}^2\frac{C_T^2}{T_p^2} + i_n^2\right) = 0 \implies T_{p.opt} = \frac{v_{nw}}{i_n}C_T \tag{2.94}$$

Figure 2.22 reports the ENC versus peaking time for a system with the following parameters:

- $C_T = 1\,\mathrm{pF}$
- $v_{nw}^2 = 10^{-17}\,\mathrm{V}^2/\mathrm{Hz}$
- $A_f = 10^{-12}\,\mathrm{V}^2$
- $i_n^2 = 10^{-24}\,\mathrm{A}^2/\mathrm{Hz}$

It can be seen that the minimum noise is actually achieved at the intersection between the series and parallel noise curves.

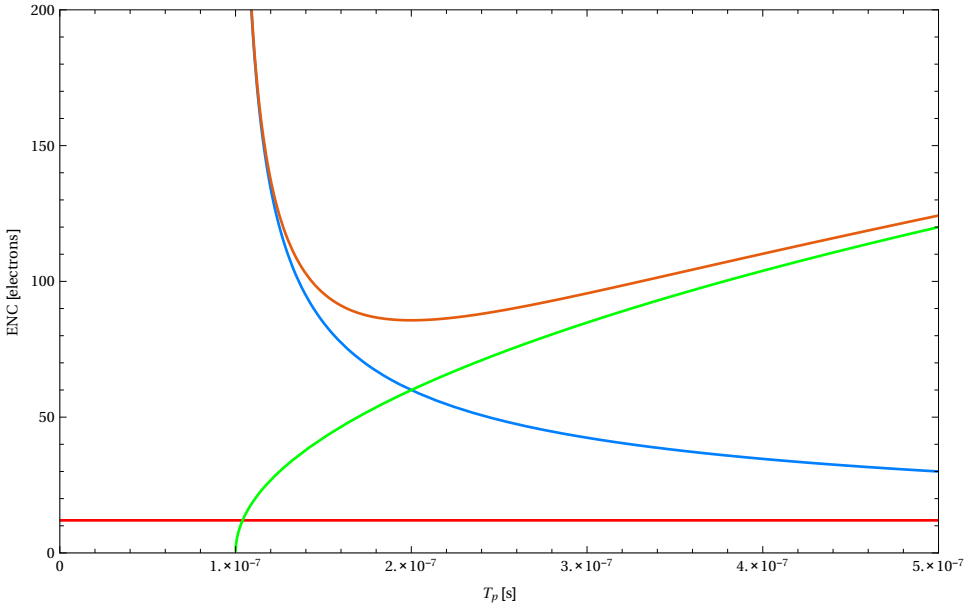


Figure 2.22: ENC versus peaking time T_p.

Chapter 3

$\bar{\text{P}}$ANDA Strip ASIC

As introduced in section 1.4, the readout ASIC designed to serve the double-sided micro strip silicon sensors of the $\bar{\text{P}}$ANDA Micro Vertex Detector is named PASTA ($\bar{\text{P}}$ANDA Strip ASIC). Among the many challenges in developing PASTA, one of the most important and characteristic for the $\bar{\text{P}}$ANDA experiment is the demand for a triggerless data acquisition system [65]. In order to provide accurate measurements of both time stamp and charge, a time-based approach has been chosen [66]. The charge information is extrapolated using the Time over Threshold (ToT) technique. The time spent over threshold by the amplifier output is in general proportional to the magnitude of the input signal. Therefore, by measuring the duration of the comparator response, one can extract the information about the input charge [67-70]. The ToT technique offers several advantages with respect to a more standard amplitude measurement. In fact, it has no limitation from the point of view of the voltage dynamic range since a time measurement is still possible even in presence of large signals saturating the front-end amplifier. Moreover, it is possible to benefit from the excellent results achieved by the Time of Flight for Positron Electron Tomography (TOFPET) ASIC [63], a chip developed for medical physics applications, that inspired the measurement concept and served as the starting point for the design of the Time to Digital Converter (TDC) performing the time measurements in PASTA. The chip measurement concept is shown shown in figure 3.1.

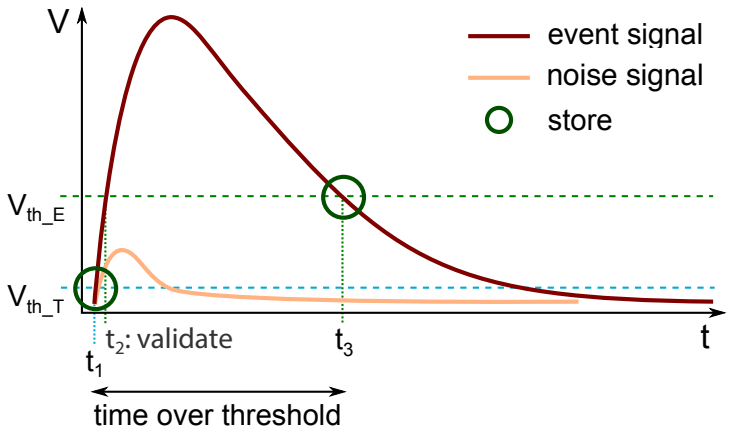


Figure 3.1: PASTA measuring concept (inspired by TOFPET). Image adapted from [2].

Points in time are measured based on two leading-edge discriminator outputs. The first one is aimed to resolve the beginning of the signal pulse

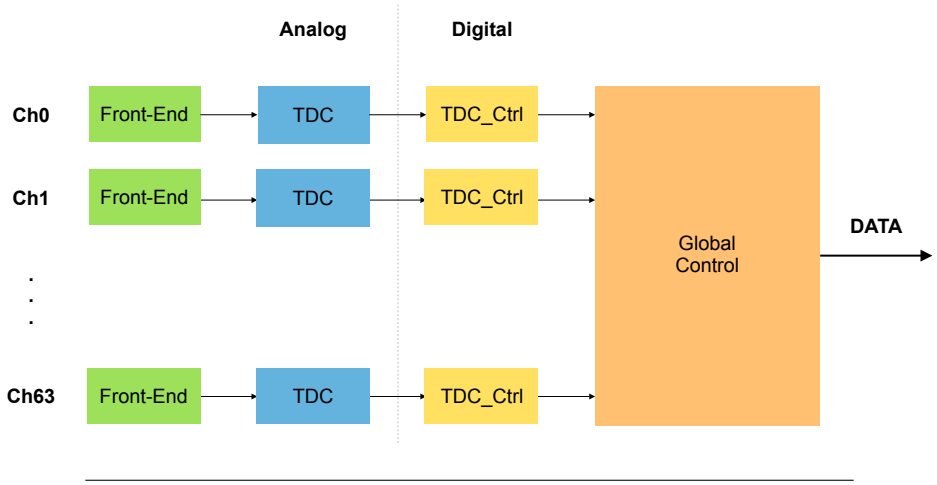


Figure 3.2: $\bar{P}$ANDA Strip ASIC building blocks.

precisely and its branch is consequently associated with the name *time*. A second discriminator measures the second point on the falling edge to get the pulse length information corresponding to the deposited charge, and since the extracted ToT contributes to energy-loss measurement used for particle identification it is named *energy* branch. Because the falling edge of the pulse is much slower than the rising edge, it generates a higher jitter on the time-stamp, therefore another discriminator with a higher threshold is used. PASTA is divided into four major parts (see figure 3.2):

- **Analog Front-End Amplifier** (section 3.1)
- **Analog Time to Digital Converter** (section 3.2)
- **Digital Blocks** (section 3.3)

Besides the main blocks, further auxiliary circuitry exists:

- **Calibration Circuit**, generating test pulses with a configurable amplitude with the possibility to have only one channel triggered at the time.
- **I/O Drivers**, transforming incoming and outgoing signals from/to LVDS standard.
- **Bias Cells**, providing the necessary voltage levels for the analog components.

The main topic of this thesis is the description of the PASTA front-end amplifier architecture, thus just a broad overview will be given for the other blocks. The performance of the chip will instead be described in chapter 4 making a comparison between simulations and data.

3.1 PASTA Front-End Amplifier

The main design goals of the PASTA front-end amplifier regards a linear relationship between the signals length and the input charge, low electronic

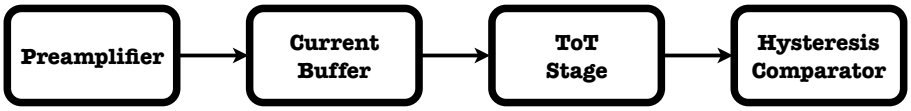


Figure 3.3: PASTA front-end amplifier building blocks.

noise, and low power consumption. The amplifier can be sub-divided into four main blocks, which are also shown in figure 3.3:

- **Preamplifier**, providing a first amplification of the small signals coming from both n- and p-type strips.
- **Current Buffer**, enhancing the charge amplification and offering the proper impedance matching between the two main stages.
- **ToT Stage**, improving the linearity of the system.
- **Hysteresis Comparator**, setting the thresholds for the time and energy branches.

3.1.1 Preamplifier

The first stage of the PASTA front-end amplifier is the preamplifier (shown in figure 3.4). It can be divided into three main blocks that will be studied separately: the charge sensitive amplifier (CSA), the active feedback network, and the peaking time adjuster stage. This is the stage providing a first amplification of the small input signals coming from the micro strips. An important requirement is that the amplifier does not saturate, otherwise undesired voltage variations would occur in the node providing the direct connection to the sensor. Two different feedback networks have been implemented in order to allow the processing of signals coming from both n-type and p-type strips. Through a series of switches driven by the digital global controller, it is thus possible to select the proper configuration.

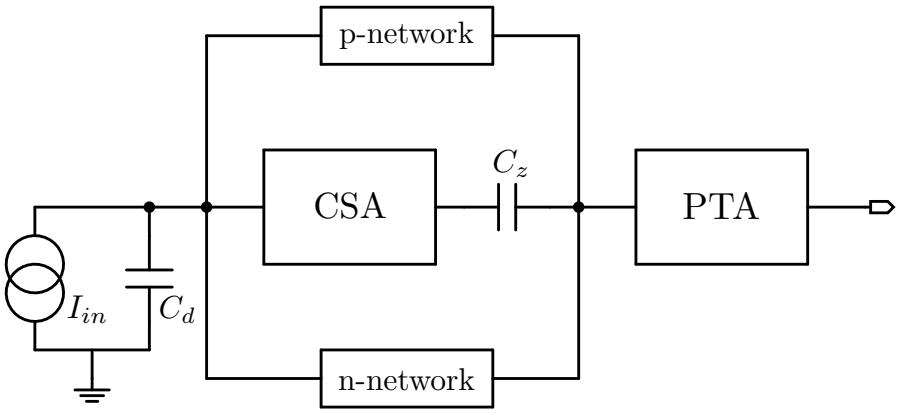


Figure 3.4: Preamplifier stage building blocks. The feedback capacitance C_f is not indicated because it is contained within the CSA.

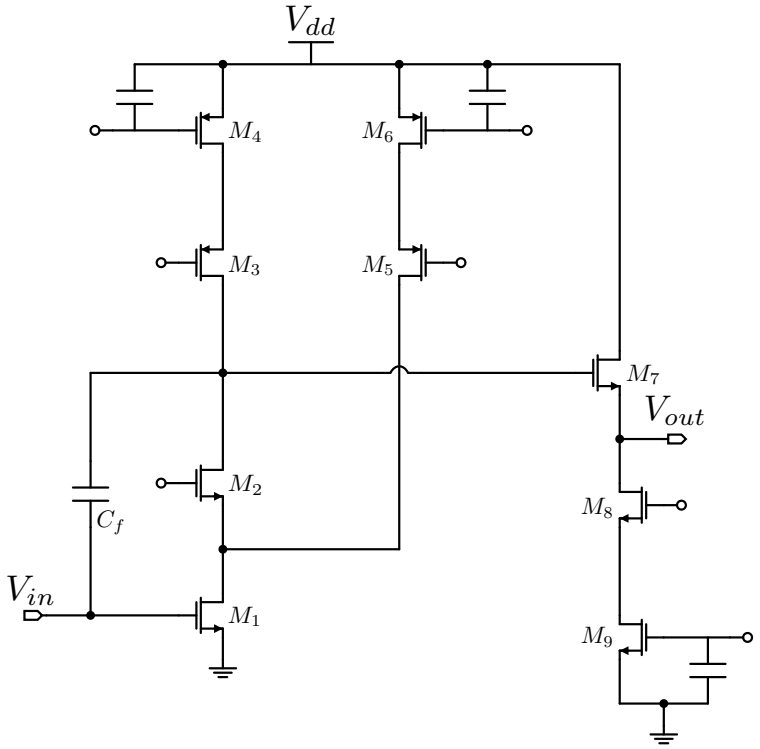


Figure 3.5: Charge sensitive amplifier of the PASTA preamplifier stage.

3.1.1.1 Charge Sensitive Amplifier

The CSA designed for the PASTA front-end amplifier is a telescopic cascode amplifier (M_1-M_4) with split bias current (M_5-M_6) [64] ending with a source follower output stage (M_7-M_9) working as a buffer (see figure 3.5). The transconductance of the cascode is basically given by the one of the input transistor and the load is provided by the parallel combination of the output resistance of the two cascode stages. In a first approximation, a cascode can therefore be represented with the same small signal equivalent circuit describing a common source amplifier, with g_m given by the transconductance of the input transistor and load resistor R_L by the parallel combination of the cascode resistances. The gain can hence be written as:

$$A_v = -g_{m1} R_L = -g_{m1} \left(r_{0casN} /\!/ r_{0casP} \right) \tag{3.1}$$

It can be proven that $r_{0casN} = r_{01} + r_{02} + (g_{m2} + g_{mb2})\, r_{01} r_{02}$ [64] (the same is of course true for r_{casP}), thus the above equation becomes:

$$A_v = -g_{m1} \left[r_{01} + r_{02} + (g_{m2} + g_{mb2})\, r_{01} r_{02} \right] /\!/ \left[r_{03} + r_{04} + (g_{m3} + g_{mb3})\, r_{03} r_{04} \right] \tag{3.2}$$

The further bias branch built by M_5-M_6 allows for a better optimization of the cascode amplifier for low power operation. In fact, the main branch powers the cascode devices with only a fraction of the total current, while

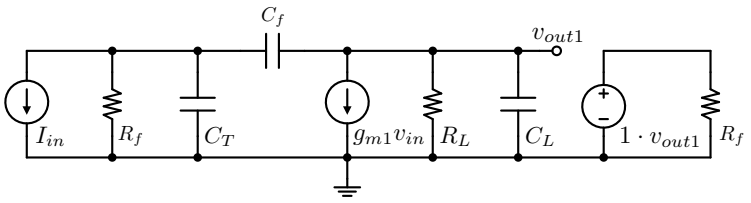


Figure 3.6: Small signal equivalent circuit of the PASTA CSA. The resistor R_f represents the equivalent impedance provided by the active feedback network, R_L and C_L are the equivalent load impedance and capacitance respectively, and v_{out1} is the output voltage of the first stage.

most of the bias current is delivered to the input transistor by the additional branch.

It is important to observe that in the schematic of figure 3.5 the feedback capacitance is connected between the input node of the CSA and the output of the first stage. This design choice stems from the study of the small equivalent circuit of the CSA shown in figure 3.6. The total transfer function is:

$$T(s) = \frac{\left(g_{m1} - sC_f\right) R_L R_f}{s^2 R_f R_L C_1^2 + s\left[R_L\left(C_f + C_L\right) + R_f\left(C_T + C_f\right) + A_v R_f C_f\right] + 1} \tag{3.3}$$

where

$$C_1^2 = 2C_f^2 + C_f C_L + C_T C_f + C_L C_T \tag{3.4}$$

In general, the coefficient of s is dominated by the term multiplying the DC voltage gain A_v, thus a more simplified version of the transfer function can be written as:

$$T(s) \approx \frac{\left(g_{m1} - sC_f\right) R_L R_f}{s^2 R_L R_f C_1^2 + sA_v R_f C_f + 1} \tag{3.5}$$

Assuming that the two poles are real and well separated in frequency, the denominator of the above expression can be written as:

$$\left(1 + s\tau_1\right)\left(1 + s\tau_2\right) = s^2\tau_1\tau_2 + s\left(\tau_1 + \tau_2\right) + 1 \approx s^2\tau_1\tau_2 + s\tau_1 + 1 \tag{3.6}$$

where the assumption $\tau_1 \gg \tau_2$ has been made. Comparing the above relationship with the simplified transfer function the result is:

$$\begin{cases} \tau_1 = A_v R_f C_f & \longrightarrow \omega_1 = -\frac{1}{\tau_1} = \frac{1}{g_{m1} R_L R_f C_f} \\ \tau_2 = -\frac{R_L R_f C_1^2}{A_v R_f C_f} & \longrightarrow \omega_2 = -\frac{1}{\tau_2} \approx \frac{g_{m1} C_f}{C_T\left(C_L + C_f\right)} \end{cases} \tag{3.7}$$

where the last approximation derives from the assumption $C_T \gg C_L, C_f$. Considering that the two dominant poles are those corresponding to the input and the output of the first stage, connecting the feedback capacitance

between those two nodes offers a better stability with respect to an architecture where it would be connected between the gate of the input transistor and the output of the source follower stage.

3.1.1.2 Active Feedback Network

As discussed in section 2.2.4, the pole-zero cancellation in a standard front-end amplifier is obtained through a resistor R_z connected in parallel to the capacitance C_z at the output of the CSA so that $R_f C_f = R_z C_z$, where R_f is the impedance providing the DC feedback path. In the PASTA preamplifier, the pole-zero cancellation is achieved using active components as shown in figure 3.7, but in this case it is not straightforward to see that such a network actually provides the desired effects. To verify that the active network is performing the pole-zero cancellation, it is necessary to evaluate the equivalent impedances $(R_f)_{eq}$ and $(R_z)_{eq}$. The first is the resistance seen between the input and the output nodes of the CSA and, in the case of the p-strips configuration, it can be evaluated considering the following steps:

1. The CSA is a transimpedance amplifier, so the input current I_{in} is converted into a voltage value V_{CSA}.
2. V_{CSA} is turned back into a current equal to $g_{mp1} V_{CSA}$ by M_{p1}.
3. The current is converted into a voltage by M_{p2}.
4. Finally the voltage becomes a current equal to $V_{CSA} g_{mp1} \frac{g_{mp3}}{g_{mp2}} \equiv I_{in}$

The final expression obtained is:

$$(R_f)_{eq} = \frac{V_{CSA}}{I_{in}} = \frac{1}{g_{mp1}} \left(\frac{g_{mp2}}{g_{mp3}} \right) \tag{3.8}$$

Following similar steps, $(R_z)_{eq}$ is given by:

$$(R_z)_{eq} = \frac{V_{CSA}}{I_{out}} = \frac{1}{g_{mp1}} \left(\frac{g_{mp2}}{g_{mp4}} \right) \tag{3.9}$$

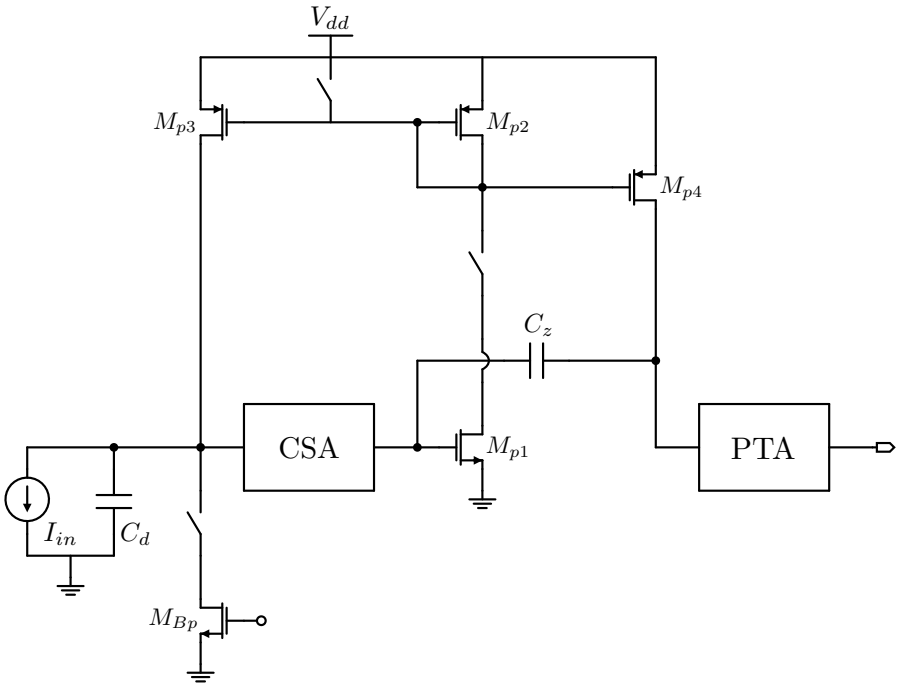
The above equations show that the pole-zero cancellation is achieved by a proper sizing of the transistors building the feedback network. In fact, considering that the transconductance of a MOS transistor is proportional to its aspect ratio W/L (where W and L indicate the width and the length of the MOSFET gate respectively) the following condition can be easily satisfied:

$$\frac{(R_f)_{eq}}{(R_z)_{eq}} = \frac{g_{mp4}}{g_{mp3}} = \frac{\left(\frac{W}{L}\right)_{p4}}{\left(\frac{W}{L}\right)_{p3}} = \frac{C_z}{C_f} \tag{3.10}$$

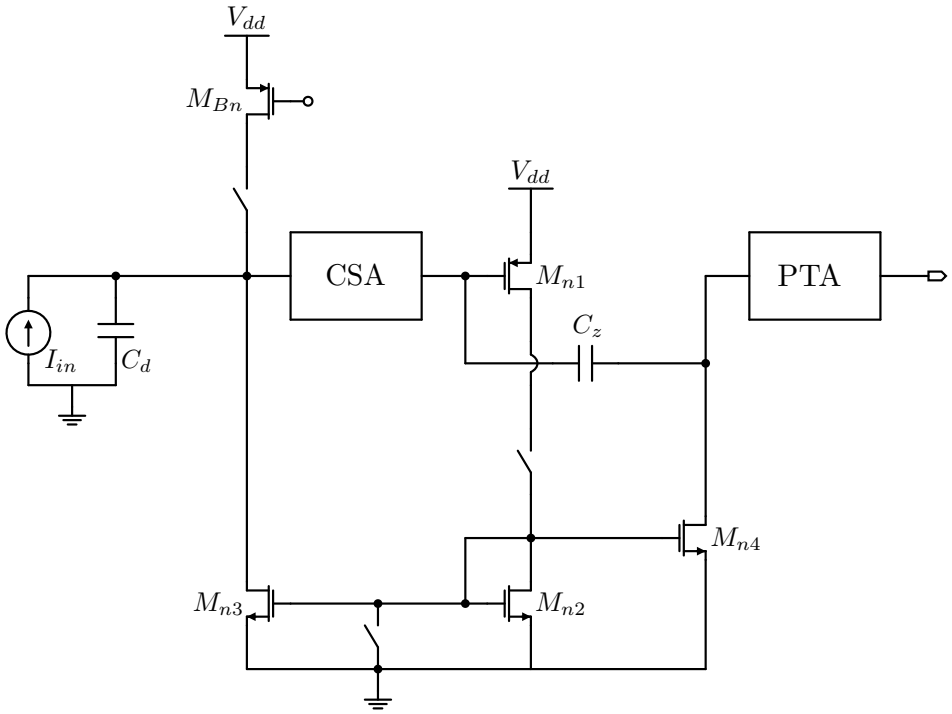
This result is verified looking at the DC operating points from the simulations shown in table 3.1. Considering that

$$C_z = 20 \cdot C_f = 20 \cdot 200\,\text{fF} \tag{3.11}$$

the result is:



(a) p-strips configuration



(b) n-strips configuration

Figure 3.7: PASTA preamplifier acrive feedback network. The transistors labelled $M_{Bp,n}$ provide the DC current according to the configuration used.

Table 3.1: Relevant DC operating points of the active feedback network of the preamplifier stage (p-strips configuration).

Parameter	Value
g_{mp3}	$1.37\,\mu S$
g_{mp4}	$26.34\,\mu S$

$$\tau_f = \frac{C_f}{g_{mp3}} = 146.20\,\text{ns} \tag{3.12}$$

$$\tau_z = \frac{C_z}{g_{mp4}} = 151.84\,\text{ns} \tag{3.13}$$

so the two time constants can be considered equal within an error in the order of $\sim 4\,\%$.

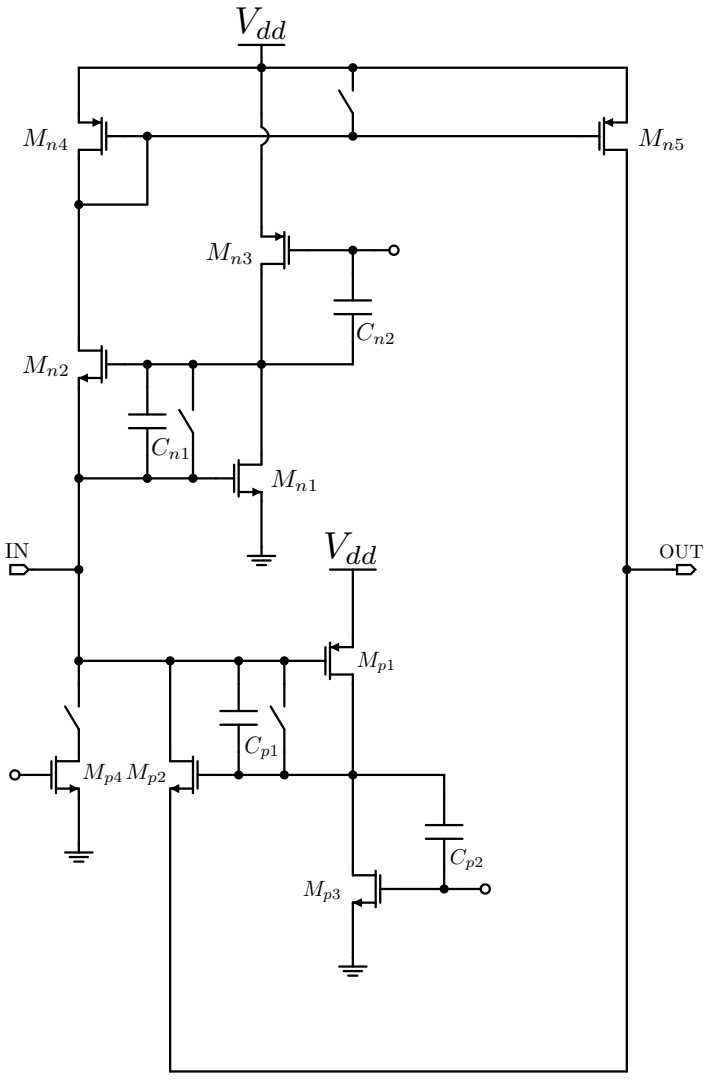
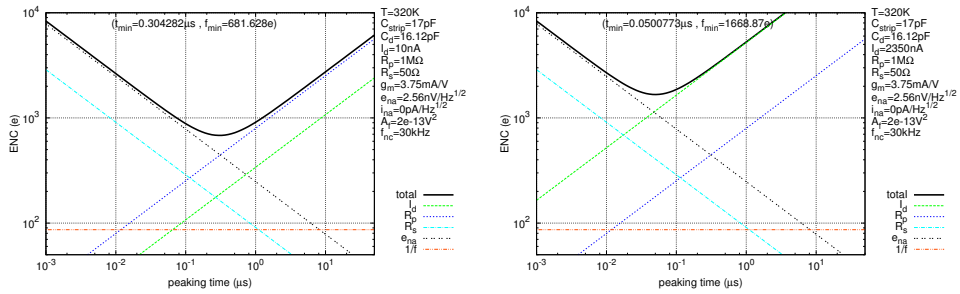


Figure 3.8: Peaking time adjuster stage of the preamplifier stage.

3.1.1.3 Peaking Time Adjuster

The output stage of the preamplifier is the peaking time adjuster shown in figure 3.8. The reason for this name is that it was introduced to increase the peaking time of the signal to improve the performance in terms of equivalent noise charge (ENC) in an irradiated regime [62]. The expected radiation field is going to affect all active electronic components inside the MVD in different ways. Naturally, a higher susceptibility to these effects can be found in analog circuitry with high sensitivity or high gain factors. The sensors and the preamplifier stages of the front-ends are such elements. The calculated ENC for different irradiation scenarios is reported in figure 3.9.



(a) Equivalent noise charge in dependence of shaping time without assumed infliction of radiation effects

(b) Equivalent noise of the preamplifier connected with sensor irradiated to $2.5 \times 10^{13}\,\mathrm{n_{1\,MeVeq}/cm^2}$ after an accumulated ionizing dose of $5\,\mathrm{Mrad}$

Figure 3.9: Expected equivalent noise charge under different irradiation scenarios. Images from [62].

Without this stage, the peaking time of the front-end amplifier is in the order of $\mathcal{O}\,(10\,\mathrm{ns})$, while introducing these networks it moves towards values of $\mathcal{O}\,(50\,\mathrm{ns})$ guaranteeing better performance in case of irradiation.

Besides the discussed motivations, this stage provides further voltage amplification exploiting the g_m-boosting technique [64] that will be explained into more detail in the next section in the description of the current buffer. Since the preamplifier aims at being the only stage dealing with the dual polarity of the input signals, the output current must flow in the same direction for both p- and n-configurations. In fact, in the schematic can be observed that in the n-network the output stage is a pMOS current mirror matching the flowing direction of the current coming from the p-network. To understand the effects of this stage, it is better to study the two different networks separately. The n-network is shown in figure 3.10.

To simplify the study, it is helpful to split the circuit into two different parts:

- The output transistor of the pMOS current mirror M_{n5} delivering the current $I_{out} = g_{mn5} v_{sgn5}$
- The network comprised of $M_{n1} - M_{n4}$

The small equivalent circuit for the above mentioned network is shown in figure 3.11. The nodal equations to solve are the following:

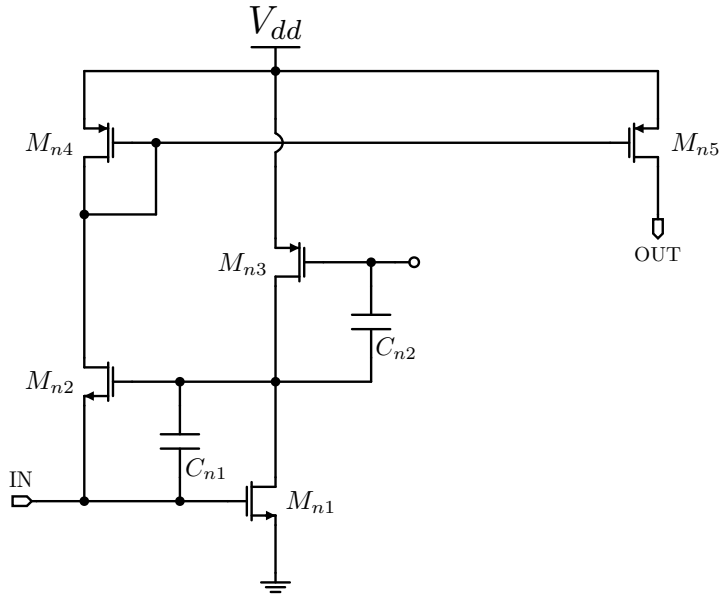


Figure 3.10: The n-network of the peaking time adjuster stage.

$$\begin{cases} g_{mn4}v'_{out} + g_{mn2}\left(v_{gn2} - v_{in}\right) + \frac{v'_{out} - v_{in}}{r_{0n2}} = 0 \\ \left(v_{gn2} - v_{in}\right) sC_{1n} + g_{mn1}v_{in} + v_{gn2}\left(\frac{1}{r_{0n1}/\!/r_{0n3}} + sC_{n2}\right) = 0 \\ I_{in} + \frac{v_{in}}{R_{in}} - g_{mn2}\left(v_{gn2} - v_{in}\right) + \frac{v_{in} - v'_{out}}{r_{0n2}} + \left(v_{in} - v_{gn2}\right) sC_{1n} = 0 \end{cases} \tag{3.14}$$

where $v_{sgn5} \equiv v'_{out}$ is the output voltage of the $M_{n1} - M_{n4}$ stage. The complete solution of such a system is a complicated expression from which it is impossible to get immediate information. However, to a first approximation, it is possible to consider only the most dominant terms, i.e. the

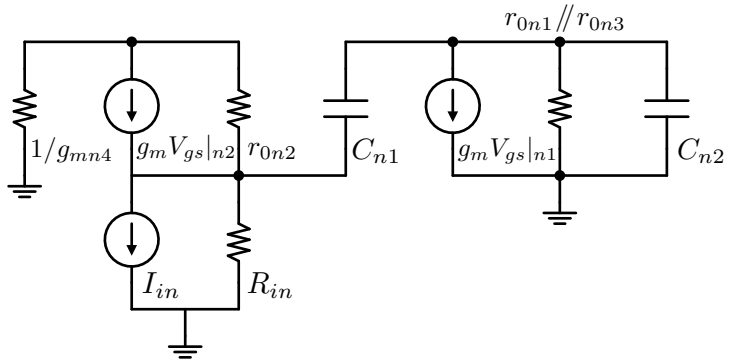


Figure 3.11: Small signal equivalent circuit of the $M_{n1} - M_{n4}$ stage of the peaking time adjuster n-network.

ones multiplied by "$g_m r_0$"-type factors. The terms to take into account are the following:

- $g_{mn2} r_{0n2} R_{in} \left(1 + g_{m1} r_{n1n3} + s r_{n1n3} C_{n2}\right)$ (numerator)
- $g_{mn1} r_{n1n3} R_{in} s C_{n1} \left(1 + s \frac{C_{n2}}{g_{mn1}}\right) \left(1 + g_{mn4} r_{0n2}\right)$ (denominator)
- $g_{mn2} g_{mn4} r_{0n2} R_{in} \left(1 + g_{mn1} r_{n1n3} + s r_{n1n3} C_{n2}\right)$ (denominator)

Performing a DC simulation of the p-network of the peaking time adjuster stage, the operating points of the involved devices can be used to estimate the value of some terms of the above expressions. In particular, the most useful to make some approximation are reported in table 3.2.

Table 3.2: Relevant DC operating points of the n-network of the peaking time adjuster stage.

Parameter	Value
g_{mn1}	$731\,\mu\text{S}$
g_{mn4}	$42\,\mu\text{S}$
r_{n1n3}	$59\,\text{k}\Omega$
r_{0n2}	$53\,\text{M}\Omega$

where $r_{n1n3} \equiv r_{0n1} \,/\!/\, r_{0n3}$. According to these results, some approximations can be made:

$$g_{mn1} r_{n1n3} \approx 44 \Longrightarrow 1 + g_{mn1} r_{n1n3} \approx g_{mn1} r_{n1n3} \tag{3.15}$$

$$g_{mn4} r_{0n2} \approx 2206 \Longrightarrow 1 + g_{mn4} r_{0n2} \approx g_{mn4} r_{0n2} \tag{3.16}$$

Hence, the approximated version of the solution of the system of equations (3.14) is:

$$\frac{v'_{out}}{I_{in}} \approx -\frac{\cancel{g_{mn1} g_{mn2} r_{n1n3} r_{02} R_{in} \left(1 + s \frac{C_{n2}}{g_{mn1}}\right)}}{\cancel{g_{mn1} g_{mn2} r_{n1n3} r_{02} R_{in} \left(1 + s \frac{C_{n2}}{g_{mn1}}\right)} g_{mn4} \left(1 + s \frac{C_{n1}}{g_{mn2}}\right)} \tag{3.17}$$

The final expression of the current gain of the stage is obtained using the relationship $I_{out} = g_{mn5} v'_{out}$ yielding to:

$$\frac{I_{out}}{I_{in}} = -\frac{g_{mn5}}{g_{mn4}} \frac{1}{1 + s\tau_n} \tag{3.18}$$

with $\tau_n = C_{1n}/g_{mn2}$. From the above expression it might seem that the capacitance C_{n2} plays no role in the transfer function of the circuit, but this is mainly due to the approximations made. In fact, the actual position of zero (without any approximation of the numerator) of the transfer function is not

$$s_z = -\frac{g_{mn1}}{C_{n2}} \tag{3.19}$$

but

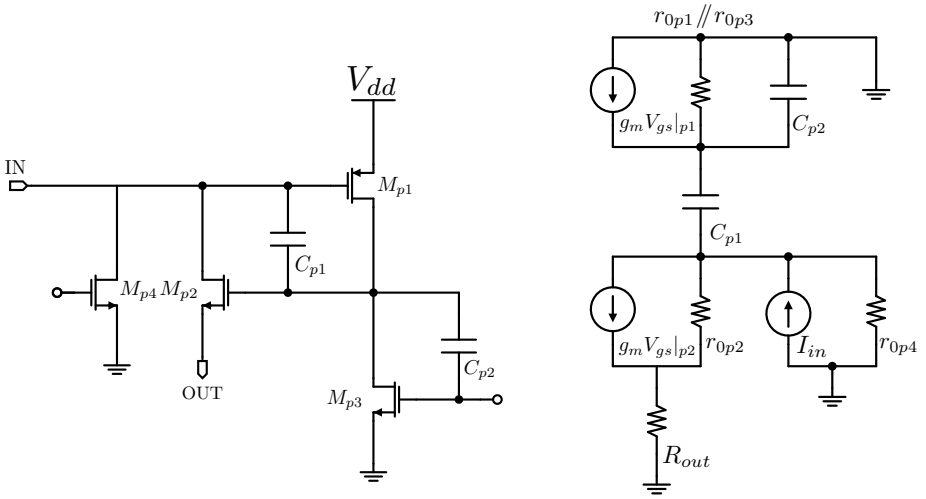
$$s_z = -\frac{g_{mn1} g_{mn2} r_{0n2}}{C_{n1} + g_{mn2} r_{0n2} C_{n2}} \tag{3.20}$$

Hence, in the case $C_{n2} = 0$, the transfer function would be:

$$\frac{I_{out}}{I_{in}} \approx -\frac{g_{mn5}}{g_{mn4}} \frac{1 + s\tau_z}{1 + s\tau_n} \tag{3.21}$$

with $\tau_z = \tau_n / g_{mn1} r_{0n2}$. Therefore, it can be deduced that the capacitance C_{2n} acts as stabilizing component through a pole-zero cancellation compensation.

The p-network of the peaking time adjuster and its small signal equivalent circuit are shown in figure 3.12.



(a) Schematic (b) Small signal equivalent circuit

Figure 3.12: Input stage of the PASTA current buffer stage.

The corresponding equations are:

$$\begin{cases} g_{mp1} v_{in} + v_{gp2} \left(\frac{1}{r_{0p1} /\!/ r_{0p3}} + sC_{p2} \right) + \left(v_{gp2} - v_{in} \right) sC_{p1} = 0 \\ g_{mp2} \left(v_{in} - v_{gp2} \right) + \left(v_{in} - v_{gp2} \right) sC_{p1} + \frac{v_{in} - v_{out}}{r_{0p2}} + \frac{v_{in}}{r_{0p4}} = I_{in} \\ -g_{mp2} \left(v_{in} - v_{gp2} \right) + \frac{v_{out} - v_{in}}{r_{0p2}} + \frac{v_{out}}{R_{out}} = 0 \end{cases} \tag{3.22}$$

In this case, the role of the input is played by M_{p4} through its equivalent impedance r_{0p4}, but the output resistance R_{out} must be taken into account with respect to the previous case where it was given by $1/g_{mn4}$. Again, for the sake of simplicity, only the most dominant term of the obtained result will be reported:

$$\frac{v_{out}}{I_{in}} \approx \frac{\cancel{g_{mp1} g_{mp2} r_{p1p3} r_{0p2} r_{0p4} R_{out} \left(1 + s\frac{C_{p2}}{g_{mp1}} \right)}}{\cancel{g_{mp1} g_{mp2} r_{p1p3} r_{0p2} r_{0p4} \left(1 + s\frac{C_{p2}}{g_{mp1}} \right)} \left(1 + s\frac{C_{p1}}{g_{mp2}} \right)} \approx \frac{R_{out}}{1 + s\frac{C_{p1}}{g_{mp2}}} \tag{3.23}$$

This time, the relationship utilized to get the current gain is $I_{out} = v_{out}/R_{out}$ and the final result is:

$$\frac{I_{out}}{I_{in}} \approx \frac{1}{1 + s\tau_p} \tag{3.24}$$

with $\tau_p = C_{p1}/g_{mp2}$. Even in this case, the capacitance C_{p2} increases the output signal stability through a pole-zero compensation effect.

The results obtained studying the implemented architectures show that the only difference between the n- and the p-network is the DC gain. In particular, in the case of the n-network the factor g_{mn5}/g_{mn4} reduces the amplitude of the signal by a factor of ~ 0.7 since the aspect ratio of the two transistors is:

$$\frac{\left(\frac{W}{L}\right)_{M_{n4}}}{\left(\frac{W}{L}\right)_{M_{n5}}} = \frac{2}{3} \tag{3.25}$$

This architectural choice has been adopted to reduce the noise contribution of the current mirror.

3.1.2 Current Buffer

The second stage of the PASTA front-end amplifier is a current buffer (shown in figure 3.13).

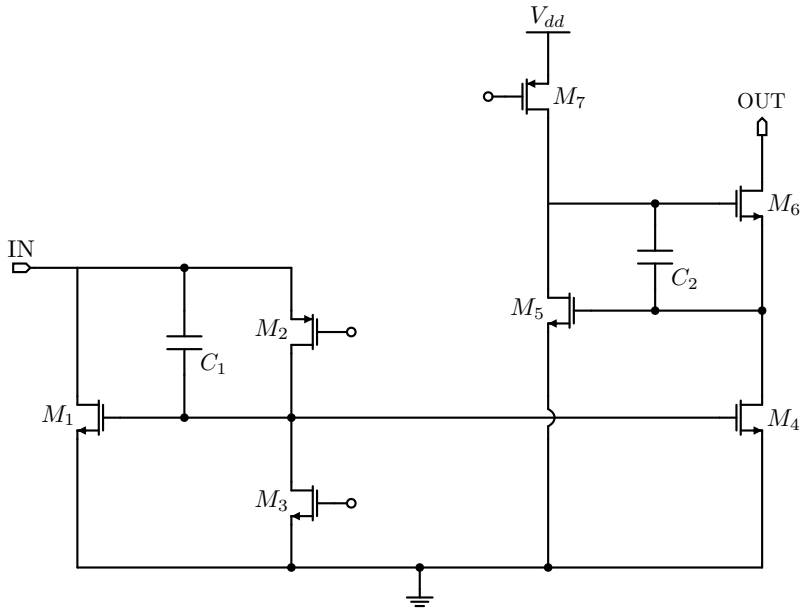


Figure 3.13: Current buffer stage of the PASTA front-end amplifier.

It has two main purposes: produce a further current (and thus charge) amplification besides the one given by the pole-zero cancellation network, and provide the correct impedance between the two amplification stages. This two goals are achieved with the previously mentioned g_m-boosting technique. To understand the principle of such an approach, it is helpful to

start from the easiest architecture for a current buffer: a current mirror. It can be shown that:

$$R_{in} \approx \frac{1}{g_{m,in}} \tag{3.26}$$

$$R_{out} \approx r_{0,out} \tag{3.27}$$

where R_{in} and R_{out} are respectively the input and the output resistances of the current mirror, $g_{m,in}$ is the transconductance of the input transistor (the one with the diode-connection), and $r_{0,out}$ is the equivalent impedance of the output transistor. An ideal current amplifier has null input and infinite output impedance, thus the goal is to get as close as possible to this situation. This is achieved with the schematic presented in figure 3.14.

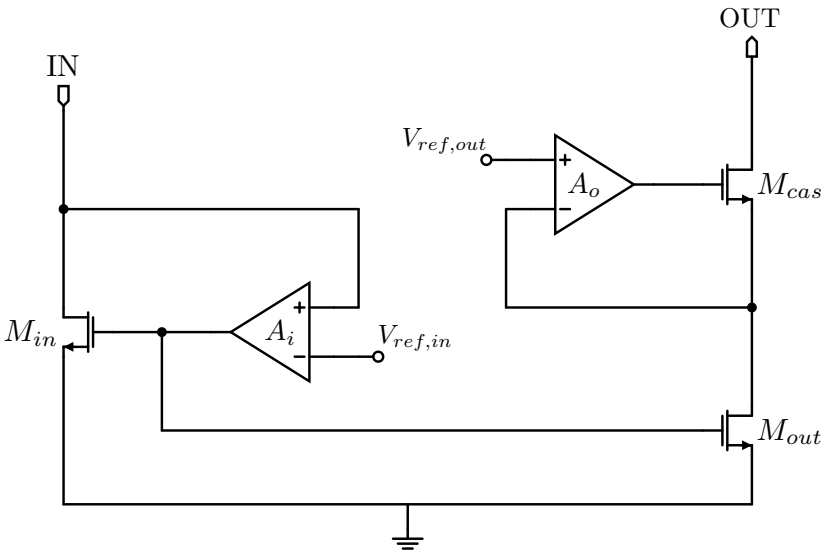


Figure 3.14: Example of current mirror with g_m-boosting technique.

To simplify the study, the input and the output stage are treated separately. Figure 3.15 shows the small signal equivalent circuit of the input stage of the architecture shown in figure 3.14.

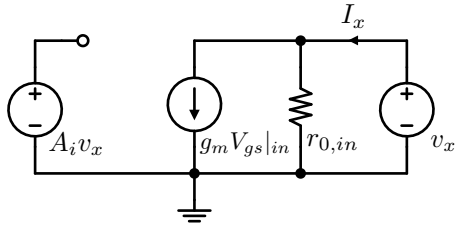


Figure 3.15: Small signal equivalent circuit of the input stage of the schematic shown in figure 3.14.

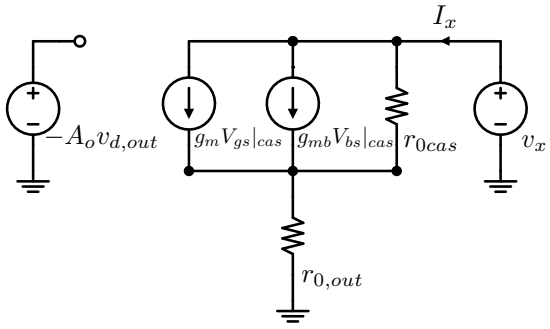


Figure 3.16: Small signal equivalent circuit of the output stage of the schematic shown in figure 3.14.

The input impedance can be calculated solving the following equation:

$$A_i g_{m,in} v_{in} + \frac{v_{in}}{r_{0,in}} = I_{in} \implies R_{in} = \frac{v_{in}}{I_{in}} = \frac{1}{A_i g_{m,in} + \frac{1}{r_{0,in}}} \approx \frac{1}{A_i g_{m,in}} \tag{3.28}$$

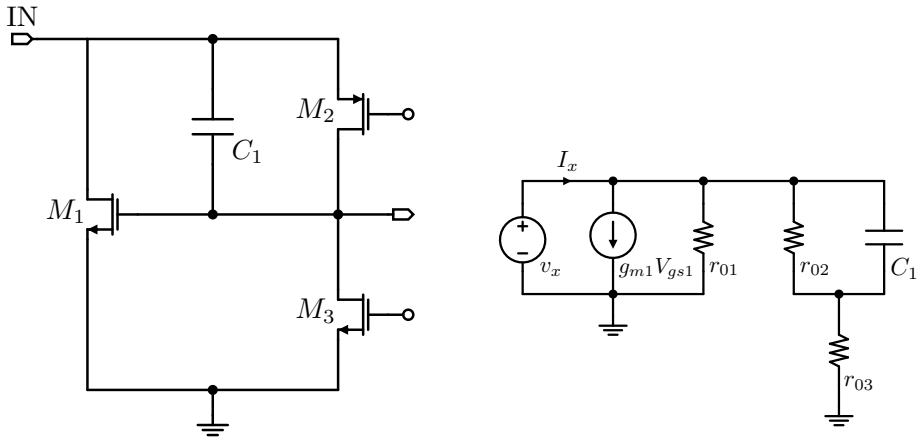
where the assumption $A_i g_{m,in} r_{0,in} \gg 1$ has been used to obtain the rightmost expression. Figure 3.16 shows the small signal equivalent circuit of the output and its nodal equations are:

$$\begin{cases} I_{out} = g_{mcas}\left(-A_o v_{d,out} - v_{d,out}\right) - g_{mbcas} v_{d,out} + \frac{v_{out} - vd,out}{r_{0cas}} \\ I_{out} = \frac{v_{d,out}}{r_{0,out}} \end{cases} \tag{3.29}$$

Solving the above equations yields to the following result:

$$R_{out} = \frac{v_{out}}{I_{out}} = r_{cas,out} + A_o g_{mcas} r_{0,out} r_{0cas} \tag{3.30}$$

where $r_{cas,out} = r_{0,out} + r_{0cas} + \left(g_{mcas} + g_{mbcas}\right) r_{0,out} r_{0cas}$ is the already mentioned output impedance of a cascoded common source amplifier. In both cases, it is interesting to observe that the effect of the amplifiers is to increase ("boost") the transconductance of the transistor building the network, hence the name of the technique. In the practical implementation, A_i and A_o are common source amplifiers. To prove that the implemented architecture has the same characteristics studied so far, the procedure is the same followed in the example. The first step is to study the input stage shown in figure 3.17 together with its small signal equivalent circuit. The system of equations to solve is the following:



(a) Schematic (b) Small signal equivalent circuit

Figure 3.17: Input stage of the PASTA current buffer stage.

$$\begin{cases} g_{m1}v'_{out} + \frac{v_x}{r_{01}} + \left(v_x - v'_{out}\right)\left(\frac{1}{r_{02}} + sC_1\right) = I_x \\ \left(v'_{out} - v_x\right)\left(\frac{1}{r_{02}} + sC_1\right) + \frac{v'_{out}}{r_{03}} = 0 \end{cases} \tag{3.31}$$

where v'_{out} is the output voltage of the input stage. The result of the above system of equations is:

$$R_{in} = \frac{v_x}{I_x} = \frac{r_{01}\left(r_{02} + r_{03} + sr_{02}r_{03}C_1\right)}{r_{02} + r_{03} + sr_{02}r_{03}C_1 + r_{01}\left(1 + g_{m1}r_{03}\right)\left(1 + sr_{02}C_1\right)} \tag{3.32}$$

Using the high gain hypothesis, the expression of R_{in} becomes:

$$R_{in} \approx \frac{1}{A_i g_{m1}} \tag{3.33}$$

where

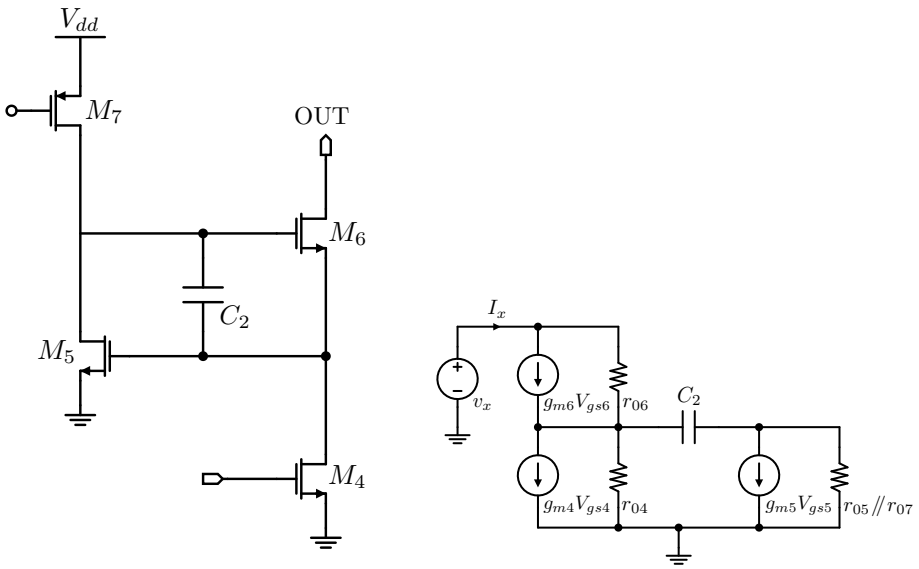
$$A_i = \frac{r_{03}}{r_{02} + r_{03}} \frac{1 + s\tau_1}{1 + s\tau_2} \tag{3.34}$$

$$\tag{3.35}$$

and

$$\begin{cases} \tau_1 = r_{02}C_1 \\ \tau_2 = \left(r_{02} \mathbin{/\!/} r_{03}\right) C_1 \end{cases} \tag{3.36}$$

To evaluate the output resistance, the circuit to study is shown in figure 3.18 where, this time, the current I_x is forced into the output node.



(a) Schematic (b) Small signal equivalent circuit

Figure 3.18: Output stage of the PASTA current buffer stage.

The small signal equivalent circuit has the following nodal equations:

$$\begin{cases} g_{m6}\left(v_{g6}-v_{g5}\right)+\frac{v_x-v_{g5}}{r_{06}}=I_x \\ -g_{m6}\left(v_{g6}-v_{g5}\right)+\frac{v_{g5}-v_x}{r_{06}}+I_x+\frac{v_{g5}}{r_{04}}+\left(v_{g5}-v_{g6}\right)sC_2=0 \\ g_{m5}v_{g5}+\frac{v_{g6}}{r_{05}/\!/r_{07}}+\left(v_{g6}-v_{g5}\right)sC_2=0 \end{cases} \tag{3.37}$$

With the usual approximation $g_m r_0 \gg 1$, the solution to the above system is given by:

$$R_{out}=\frac{v_{out}}{I_x}\approx\frac{r_{cas46}+A_o g_{m6}r_{04}r_{06}}{1+s\tau_4} \tag{3.38}$$

where

$$r_{cas46}=r_{04}+r_{06}+g_{m6}r_{04}r_{06} \tag{3.39}$$

$$A_o=g_{m5}\left(r_{05}/\!/\,r_{07}\right)\left(1+s\tau_3\right) \tag{3.40}$$

$$\tag{3.41}$$

and

$$\begin{cases} \tau_3=\frac{C_2}{g_{m6}} \\ \tau_4=g_{m5}\left(r_{05}/\!/\,r_{07}\right)r_{04}C_2 \end{cases} \tag{3.42}$$

These results show that the implemented current buffer is working as intended. In fact, the expression of R_{in} and R_{out} in the DC domain, i.e. $s=0$, obtained with the analysis of the circuit are the same observed with the ideal network. The frequency dependent factors stem, of course, from the presence of the capacitances C_1 and C_2, whose purpose is to further

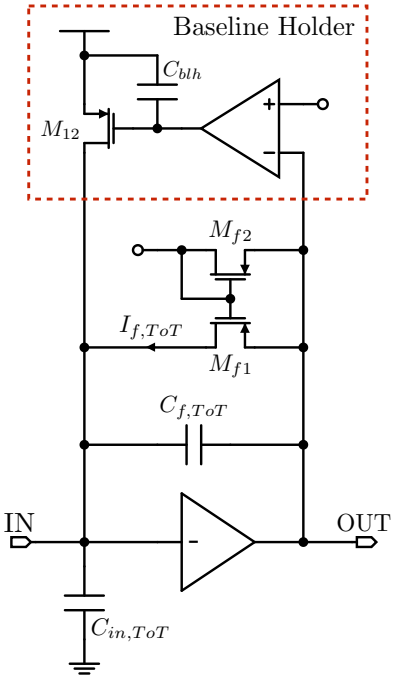


Figure 3.19: Time over threshold stage of the PASTA front-end amplifier.

increase the peaking time and the stability of the signal delivered to the ToT stage.

3.1.3 ToT Stage

The time over threshold stage, shown in figure 3.19, is where the linear relationship between the length of the signals and the input charge is achieved. It can be divided into two blocks: a differential amplifier with a feedback network formed by a capacitance and a constant current source, and a baseline holder.

3.1.3.1 ToT Amplifier

The amplifier is a simple integrator obtained by connecting a capacitor $C_{f,ToT}$ in the feedback loop of a high-gain amplifier. The current pulse coming from the current buffer is integrated on $C_{f,ToT}$, which is discharged by a constant feedback current $I_{f,ToT}$. The time needed to remove the charge is given by:

$$T = \frac{Q_{in,ToT}}{I_{f,ToT}} \tag{3.43}$$

where $Q_{in,ToT}$ is the charge at the output of the current buffer. The output signal has a triangular shape and the time over threshold is linearly proportional to the input charge. It is important to notice that the ToT is independent on the value of $C_{f,ToT}$. The ratio between $I_{f,ToT}$ and C_f, ToT defines the slope of the triangular signal when it returns to the baseline. The peak amplitude is given by $Q_{in,ToT}$, therefore if $C_{f,ToT}$ is halved, both the

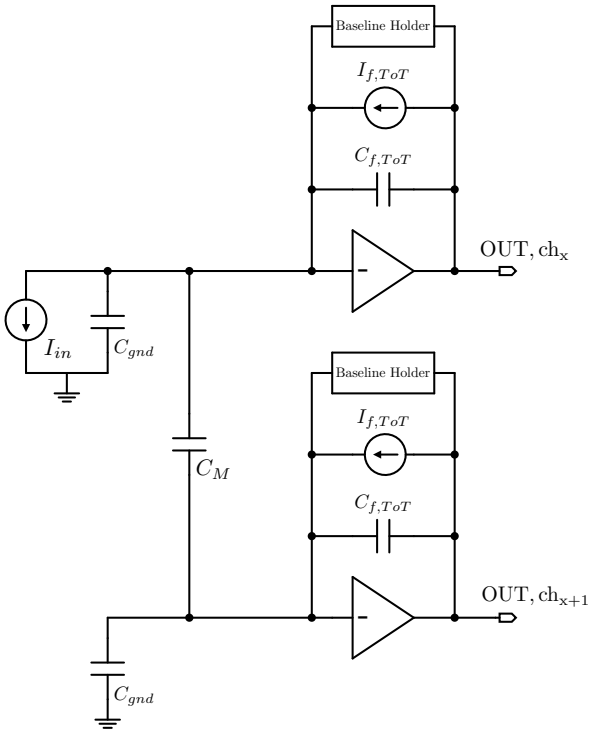


Figure 3.20: Example of cross-talk between neighbouring channels.

slope and the peak amplitude are doubled, and the time needed to return below threshold is unchanged. Another interesting feature of ToT systems is that the core amplifier can saturate without automatically compromising the linearity of the measurement. In fact, when the amplifier saturates, its DC gain drops. The virtual ground approximation is not valid and the extra charge is integrated on the amplifier input node. This charge is however removed by the feedback current, so equation (3.43) still holds. The linearity of the measurement is affected if the voltage swing at the input is high enough to push the transistors that are used in the constant current generator out of their desired working region. The lower the amplifier gain, the higher the swing of the input voltage will be, coupling part of the signal to the neighbours and generating cross-talk. This situation is sketched in figure 3.20. In the figure, C_{gnd} represents the portion of the input capacitance that can be referred to the signal ground while C_M is the mutual capacitance coupling between the two stages.

To reduce the voltage swing occurring at the input of the ToT amplifier, the input capacitance $C_{in,ToT}$ has been introduced. Its effect can be understood observing the following equation:

$$\frac{dQ_{in,ToT}}{dt} = \frac{dV_{bl}}{dt} C_{in,ToT} \tag{3.44}$$

So if $dQ_{in,ToT}/dt = const$, the bigger $C_{in,ToT}$ the lower will be the baseline fluctuation. The feedback current source is built using pMOS transistors since they have a better radiation hardness [71]. This device is one of the most important of the whole chain, in fact, when the amplifier saturates, it must recharge the feedback capacitance $C_{f,ToT}$ where the current

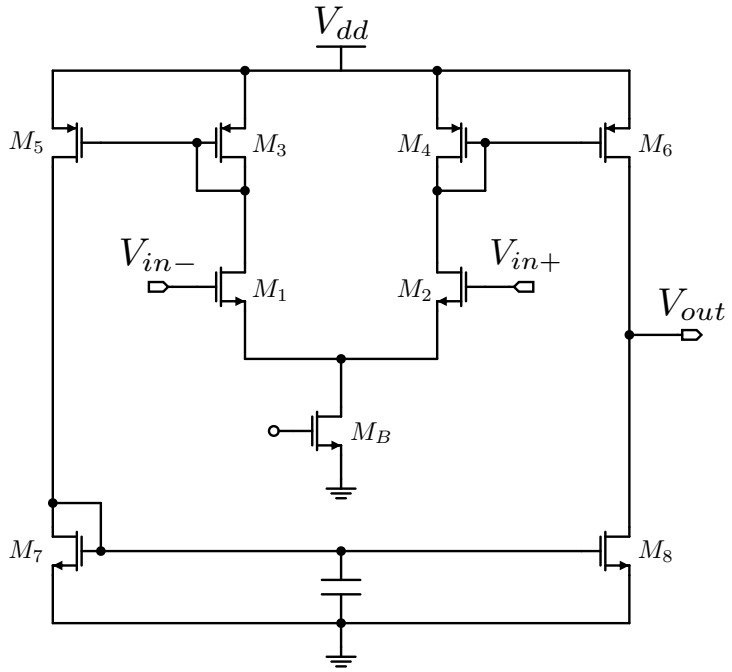


Figure 3.21: ToT stage core amplifier.

is integrated. Therefore, the output linearity of the system depends on the linear behaviour of this current source, thus on the possibility of the pMOS transistors to work in their saturation region. For a better comprehension of the above statements, it is helpful to consider the three operating regions of the current generator:

1. **Quiescent point**
   When no input occurs at this stage, the pMOS transistor M_{f1} acts like a linear resistor providing the DC feedback path.

2. $\boldsymbol{V_{out,ToT} < V_{DSf1,sat}}$
   In presence of low input charge, the output signal of the ToT Amplifier is so small that M_{f1} cannot work in its saturation region. In this case, M_{f1} acts like a non-linear resistor and as result the ToT measure is proportional to the output signal amplitude (this issue will be discussed in the next chapter where the results of the CAD simulations regarding the $ToT(Q_{in})$ linearity will be presented).

3. $\boldsymbol{V_{out,ToT} > V_{DSf1,sat}}$
   This is the correct working region of the current source. In fact, in this case M_{f1} is saturated and together with M_{f2} forms a current mirror providing the correct constant recharge current.

The architecture chosen to build the core amplifier of the ToT stage (see figure 3.21) is the same used for the pixel sensors readout [72,73]. It can be divided into two stages: a fully differential amplifier (M_1-M_4), and a common source amplifier (M_5-M_8).

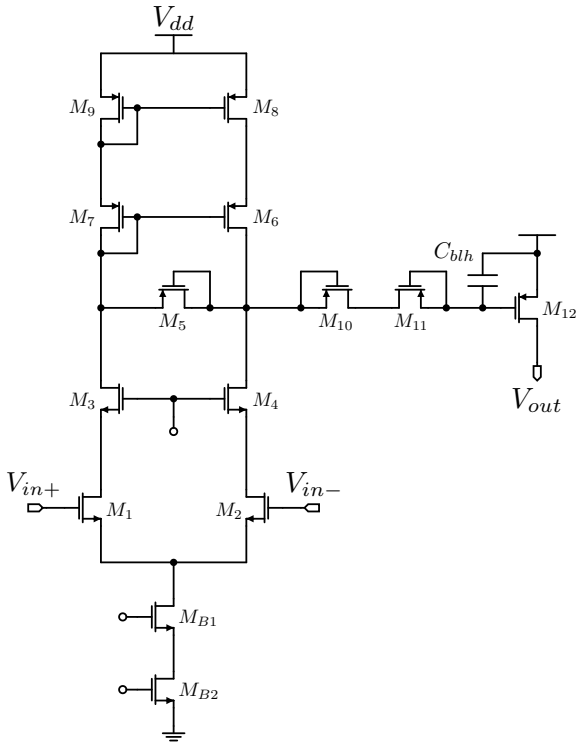


Figure 3.22: Baseline holder core amplifier.

3.1.3.2 Baseline Holder

Together with the capacitance $C_{in,ToT}$ at the input of the ToT amplifier, the baseline fluctuations are reduced with a baseline holder. The implemented architecture, shown in figure 3.22, is the same discussed in section 2.2.4.2 where a differential amplifier controls a pMOS transistor providing the proper current to the input node. Observing the schematic, the role of transistors M_9, M_{10} and M_{11} may not be immediate to understand. The first transistor limits the voltage swing at the differential stage output, the last two provide a high equivalent impedance to form a RC filter with the capacitance C_{blh}. The cut-off frequency of this filter must be as small as possible to prevent the longest signals from being clipped by the leakage compensation circuit thus avoiding the introduction of non-linearities. For this reason the equivalent impedance has been implemented with two pMOS transistors with their gate and source shorted. The need for two devices is due to the dual polarity of the variations occurring at the output of the differential stage: in case of negative variations M_{11} acts as a high value resistor and M_{10} becomes a diode connected transistor with consequent drop of its equivalent impedance, while the two transistors exchange their role in case of positive variations.

3.1.4 Hysteresis Comparator

The last stage of the PASTA front-end amplifier is a hysteresis comparator [73,74]. The circuit, shown in figure 3.24 is a symmetrical operational transconductance amplifier with a cross-coupled pair formed by M_5 and

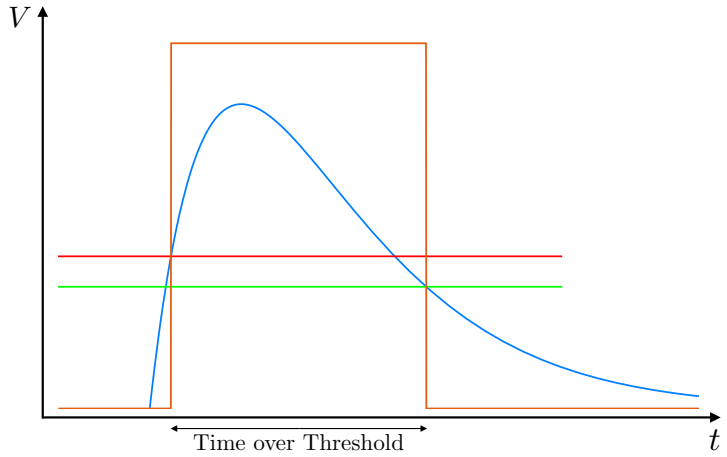


Figure 3.23: Threshold splitting as effect of the hysteresis. The comparator output signal (orange) starts when the input signal (blue) crosses the higher threshold (red) and ends when the input goes below the lower threshold (green).

M_6 acting as load. By design, the aspect ratio of the cross-coupled transistors is greater than that of the diode connected ones, thus a positive feedback is introduced and the comparator has a hysteresis. The effect of the hysteresis is to split the trip points of the discriminator, which become different if the input signal is heading a positive or a negative edge (see figure 3.23), thus avoiding the risk of multiple commutations due to noise when the signal is in proximity of the threshold.

The hysteresis mechanism can be understood by referring to figure 3.24. Supposing that initially V_{in+} is much smaller than V_{in-}, M_1 is off and all the bias current is taken by M_2. M_6 tries to mirror the current in M_4 towards V_{out1}, but since M_1 is off it can not sink any current, hence M_6 is driven into the linear region, pulling V_{out1} to V_{dd}. If V_{in+} increases, M_1 starts sinking current and when it turns on, the voltage V_{out1} is high, so M_1 is in saturation and M_3 is off. M_1 sinks its current from M_6, which is in the linear region and behaves as a resistor. As the current in M_1 increases, the current in M_2 decreases and the resistance of M_6 increases. When the current required by M_1 becomes greater than the one which can be provided by M_6, M_1 is driven in linear region and V_{out1} decreases sharply, making the comparator quickly flip. All the bias current is now taken by M_1 and mirrored by M_5. However, M_2 can not receive the current from M_5, which is driven in the linear region, pulling V_{out2} to V_{dd}. At the switching point, the following set of conditions must be verified:

$$\begin{cases} I_1 = I_6 \\ I_2 = I_4 \\ I_6 = kI_4 = kI_2 \\ I_B = I_1 + I_2 \end{cases} \tag{3.45}$$

Combining the above relationships, we can write I_1 and I_2 as a function of the bias current and of the parameter k:

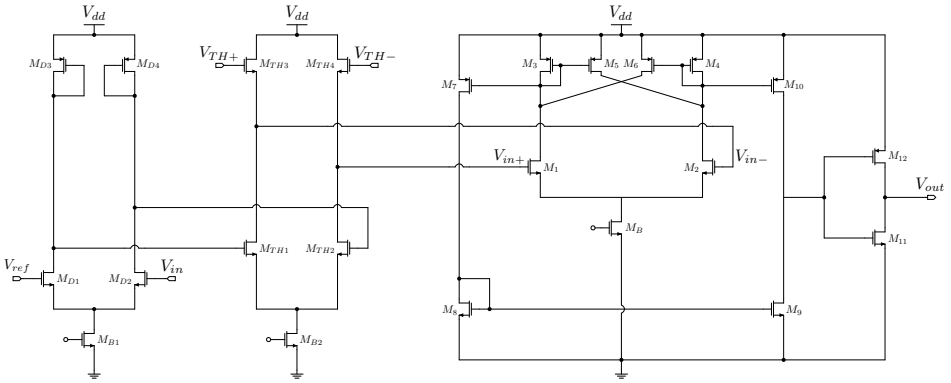


Figure 3.24: Hysteresis comparator of the PASTA front-end amplifier.

$$I_1 = \frac{k}{k+1} I_B \tag{3.46}$$

$$I_2 = \frac{1}{k+1} I_B \tag{3.47}$$

The current in M_1 is greater than the one in M_2, so at the trip point v_{gs1} must be greater than v_{gs2} and the comparator flips for $v_{gs1} - v_{gs2} = \Delta V > 0$. All the quantities in equation (3.48) are known, so v_{gs1} and v_{gs2} can be computed. When the voltage at the gate of M_1 swings back towards a low value, the role of M_1 and M_2 are exchanged, so the comparator switches again when:

$$I_1 = \frac{1}{k+1} I_B \tag{3.48}$$

$$I_2 = \frac{k}{k+1} I_B \tag{3.49}$$

Therefore, the circuit flips in the negative direction for $v_{gs1} - v_{gs2} = -\Delta V$. An important point is that when hysteresis is used, the baseline of the circuit driving the comparator must be below the lower threshold, otherwise the comparator does not return to the zero state when the signal is over, but keeps memory of the previous transition. To minimize the power consumption, the comparator should be used so that at the quiescent state the gate of M_1 is lower than the one of M_2. In fact, the current of M_1 is mirrored by M_3 and M_7 and fed to the diode connected load M_8. Hence, if at the quiescent point M_1 drives current, so does the branch formed by M_7 and M_8, increasing significantly the power consumption of the circuit.

In the PASTA front-end amplifier, the threshold is provided with a differential scheme to further improve the noise immunity. The single ended signal coming from the current buffer is converted into a differential one by the low gain differential amplifier. The second stage is formed only by

nMOS transistors and has approximately unity gain. M_{TH3} and M_{TH4} behave as source followers, and set the threshold to the discriminator. Design examples of discriminators employing differential stages with cross-coupled loads can be found for instance in [75,76].

3.2 Analog Time to Digital Converter

The measurement concept of the PASTA time to digital converter is shown in figure 3.25.

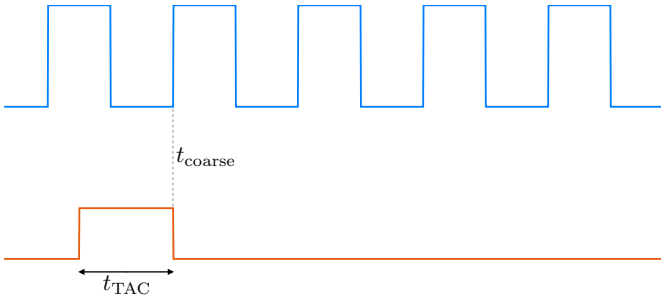


Figure 3.25: Measurement principle of the PASTA time to digital converter.

The time measurements can be divided into two steps: coarse and fine times. The coarse time is a time stamp generated with the ASIC internal counter incremented by the clock, hence its resolution is $6.25\,\text{ns}$ since the nominal clock frequency is $160\,\text{MHz}$. The second step is to measure the time t_{TAC} which, in the default configuration, is given by the difference between the time at which the hysteresis comparator of the front-end amplifier fires and the first positive edge of the clock after either a positive or negative transition. Therefore, t_{TAC} can assumes values within a certain range. To evaluate this range, two boundary cases must be taken into account: a discriminator signal occurring right before a negative edge of the clock set the minimum value $t_{\text{TAC,min}} = 0.5 \cdot T_{clk}$, while if the front-end output starts right after a negative edge of the clock the maximum value is fixed at $t_{\text{TAC,min}} = 1.5 \cdot T_{clk}$ (see figure 3.26). To achieve a higher resolution of up to $50\,\text{ps}$, the time t_{TAC} is measured with a time to digital converter.

As mentioned in the introduction of this chapter, the TDC of PASTA was adapted from a pre-existing chip. However, several changes were made in order to meet the different requirements of the two ASICs. The most significant new aspect is the change of CMOS technology from $130\,\text{nm}$ to $110\,\text{nm}$. Additionally, a tighter constraint on the total area of the chip with respect to the TOFPET ASIC made a redesign of the analog circuit necessary. The analog part of the implemented TDC is a low-power and compact structure offering a high time precision. Figure 3.27 (a) shows the simple blocks building the analog interpolator: a current source providing two different currents, a Time to Amplitude Converter (TAC), and a latched comparator.

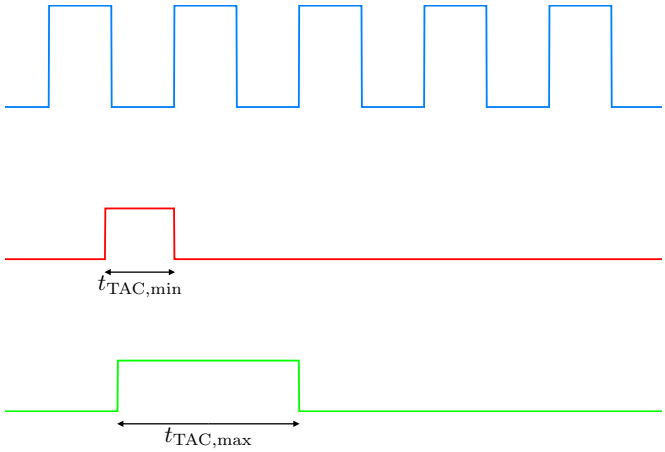
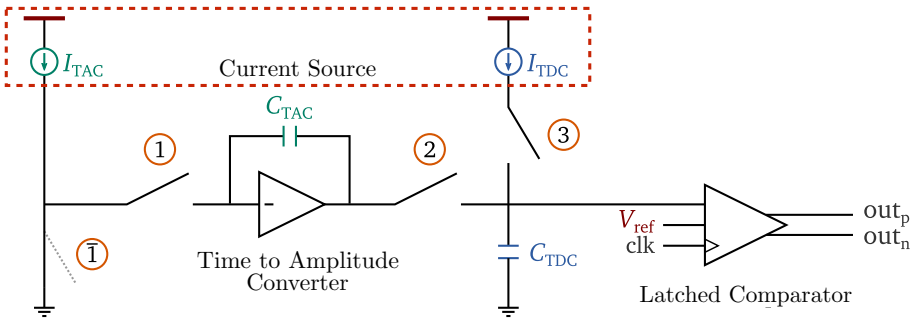
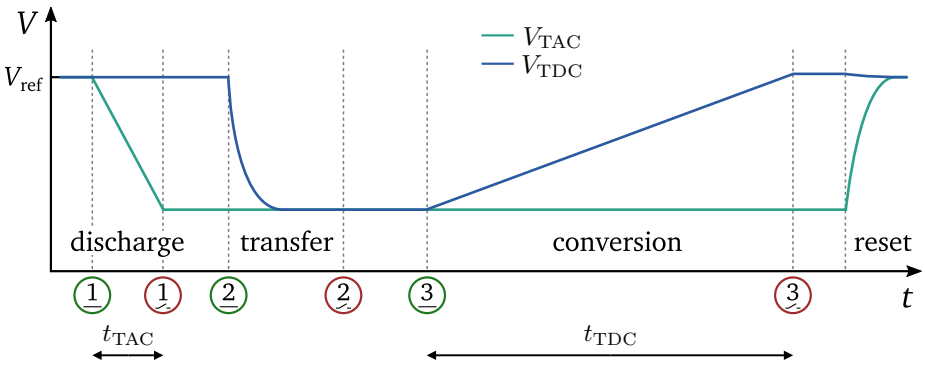


Figure 3.26: Estimation of the range of t_{TAC}.



(a) Analog TDC architecture.



(b) Working principle.

Figure 3.27: Analog TDC architecture and working principle. In case an event occurs, the switch 1 is closed. This status is maintained while a signal is issued which is synchronous to the clock and has a configurable delay up to three clock cycles. The current I_{TAC} discharges the capacitance C_{TAC} and thus the voltage V_{TAC} drops. When the local controller is ready for further operation, the switch 2 is closed and the collected charge is shared to C_{TDC}. During the last step, the switch 3 is closed and the current I_{TDC} recharges the capacitance increasing the voltage V_{TDC}. Images adapted from [2].

In the current design, each channel is provided with four different TACs to minimize the risk of missed events. Only one of them is active at the same time and the selection is performed by the digital local controller. It also controls the switches, named from 1 to 3, whenever triggered by the front-end amplifier outputs. An interpolation factor of 128 is achieved through a proper choice of the values of the currents and the capacitances according to the following formulae:

$$C_{\mathrm{TDC}} = 4 \cdot C_{\mathrm{TAC}} \tag{3.50}$$

$$I_{\mathrm{TDC}} = \frac{1}{32} \cdot I_{\mathrm{TAC}} \tag{3.51}$$

$$V_{\mathrm{TDC}} = V_{\mathrm{TAC}} \iff \frac{I_{\mathrm{TDC}} \cdot t_{\mathrm{TDC}}}{C_{\mathrm{TDC}}} = \frac{I_{\mathrm{TAC}} \cdot t_{\mathrm{TAC}}}{C_{\mathrm{TAC}}} \tag{3.52}$$

and from (3.50), (3.51), and (3.52) it is obtained:

$$t_{\mathrm{TDC}} = 128 \cdot t_{\mathrm{TAC}} \tag{3.53}$$

The values of I_{TDC} and I_{TAC} are precisely controlled by a built-in Digital to Analog Converter (DAC) in the current source stage. Considering a chip clock frequency of 160 MHz, the resulting time bin width is ~ 50 ps.

3.3 Digital Blocks

The digital logic of PASTA contains two main blocks: a local and a global controller [2]. The global controller is quite similar to the one designed for the TOFPET chip, while the local TDC controller has been strongly improved. By redesigning the structure from scratch, it was possible to optimize the logic keeping only the desired functionalities and getting rid of unnecessary parts. A major improvement is due to a new concept of the control of the TAC and TDC charging operation. In TOFPET, each of the four TACs had a complete module responsible for the operations described in Figure 3.27. However, only one TAC branch is active at a time, so an implementation with one control block removes this redundancy. Internal status flags for each TAC branch are used to select the next free slot. Another important modification is related to the location where time-stamp data is buffered. In the older version this was done in the local controller, while in PASTA the registers are placed in the global controller yielding compactness of the TDC controller and therefore speed up the behavioural simulations. This re-optimization of the logic allowed a shrinking in the order of 80 % (see figure 3.28) and a significant reduction of the power consumption with the same magnitude.

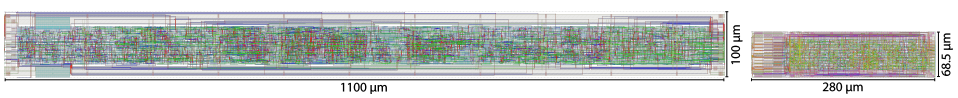


Figure 3.28: Digital TDC controller shrinking from TOFPET to PASTA. Image adapted from [2].

However, the most important implementation regards radiation-hardness in both digital blocks. In particular, two different kinds of Single Event Upset (SEU) protection had been introduced: Triple Modular Redundancy and Hamming encoding [77]. The first is used to protect single bit registers like the internal trigger based on the output signals of the front-end amplifier, while the second is used for multiple bit registers like stored configuration or the central clock counters. With these two methods, all operation-critical registers have been protected to prevent undesired freezes in operation.

Chapter 4

Simulations

The analog electronics designer's best friend is, apart from his skills, the electronic design automation (EDA) software. The one used for the simulations of the PASTA front-end amplifier is probably most popular among the experts: Cadence Design System. In particular, the features extensively used are: Virtuoso Schematic Editor, providing a complete design environment with well defined component libraries and the possibility to create new ones; and Virtuoso Analog Design Environment (ADE), allowing all kind of simulations on the designed schematic, from the parametric analysis to the Monte Carlo simulations, in order to thoroughly understand the circuit behaviour. As stated in chapter 3, the main design goals of the PASTA front-end amplifier regards a linear relationship between the signal length and the input charge, low electronic noise, and low power consumption. Nevertheless, other important studies have been performed to have a better comprehension of the overall performance of the chip and those will be the subject of this chapter.

4.1 Linearity

The results of the simulations to estimate the linearity of the PASTA front-end amplifier are shown in figure 4.1. The parameters of the simulations are:

- detector capacitance $C_d = 20\,\mathrm{pF}$
- ToT amplifier feedback current $I_{f,ToT} \approx 500\,\mathrm{nA}$
- effective hysteresis comparator threshold $V_{th} \approx 16\,\mathrm{mV}$

The value of the detector capacitance has been chosen to approximate the measured $17\,\mathrm{pF}$ for the long strips. The default value of the ToT amplifier feedback current stems from studies regarding the trade-off between the linearity and the output signal amplitude. In fact, as discussed in section 3.1.3.1 for low signals the transistor $\left(M_{f1}\right)_{ToT}$ cannot work in its saturation region thus acting like a non-linear resistor worsening the linearity of the system (as can be observed from the simulations presented in figure 4.1). The threshold set with the hysteresis comparator is the minimum allowed. The reason for that has been discussed in section 3.1.4. For lower values of the threshold, the splitting of the comparator tripping points introduced by the hysteresis would cause the lower threshold to go below the baseline value.

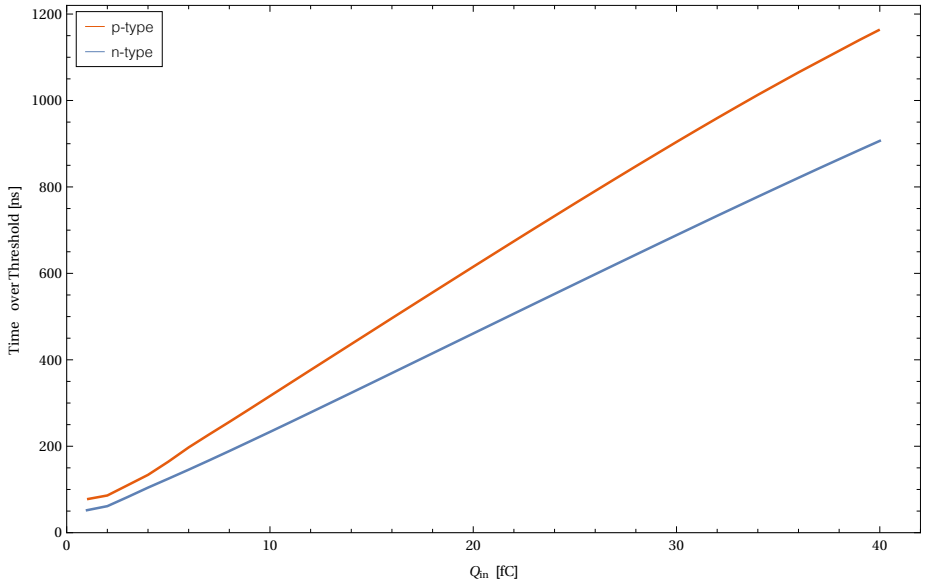


Figure 4.1: Time over threshold linearity in the input charge range of 1–40fC.

Since this is the result of a software simulation and not a real measurement, to estimate the goodness of the fit a percentage error can be defined as follows:

$$\sigma_{\%} = Mean\left[\frac{ToT_{fit} - ToT_{sim}}{ToT_{fit}}\right] \tag{4.1}$$

Using the above relationship, the percentage errors for the two different configurations are:

$$\sigma_{\%}(p) = 2.27\,\% \tag{4.2}$$
$$\sigma_{\%}(n) = 1.97\,\% \tag{4.3}$$

The main reason for this result is the non-linear behaviour of the ToT amplifier for low charges discussed above. Considering the time-based approach of the ASIC, gains of the front-end amplifier for the p- and n-configurations can be expressed using the slope of the linear fit equation, yielding to:

$$G(p) = 28.84\,\mathrm{ns/fC} \tag{4.4}$$
$$G(n) = 22.43\,\mathrm{ns/fC} \tag{4.5}$$

The difference between the two configurations will be explained in the following section, where the charge amplification of the chain will be studied. An interesting observation regards the maximum time over threshold since it determines the high-rate capability of the chip. The following values can be obtained multiplying the gain for each configuration by the maximum input charge $Q_{max} = 40\,\mathrm{fC}$:

$$ToT_{max}(p) \approx 1150\,\text{ns} \tag{4.6}$$
$$ToT_{max}(n) \approx 900\,\text{ns} \tag{4.7}$$

giving a total busy time of the front-end stage $<1.5\,\mu\text{s}$ corresponding to a rate capability $>600\,\text{kHz}$. However, the rate capability of the chip is limited by two other bottlenecks: event processing in the TDC and the data storage and transmission. The estimation of the ASIC rate capability has been discussed in [2] and the results are summarized in table 4.1.

Table 4.1: The dead time and maximum rate caused by the three bottlenecks in PASTA. Each one influences a different aspect of event rate, hence a comment clarifies the impact. The numbers are given for full clock speed ($160\,\text{MHz}$) and maximum transmission speed (combined $640\,\text{Mbit/s}$). Table adapted from [2].

Rate limiting stage	Time [µs]	Rate [kHz]	Comment
Front-end stage	<1.5	<700	Product of the maximum ToT for the input charge range of $1\,\text{fC}$ to $40\,\text{fC}$ and the gain of the front-end amplifier (longest signals refer to the p-strips configuration).
TDC	1200	<850	Product of the interpolation factor of the analog TDC 128 and the maximum $t_{\text{TAC}} = 1.5 \cdot T_{clk}$
Data transmission	10	100	Maximum continuous event rate per channel for all 64 channels. Higher rates lead to event loss due to output bandwidth limitations.

4.2 Charge Amplification

As mentioned in the introduction of chapter 3, one of the main advantage offered by the time over threshold technique is the possibility to work with a saturated amplifier. On the other hand, the amplitude of the output signals cannot be used as parameter to estimate the gain of the amplifier, hence the charge amplification has been studied. By design, the theoretical values, for p- and n-type strips respectively, should be:

$$G_{amp,p} = \frac{Q_{out}}{Q_{in}} = \frac{Q_{CSA}}{Q_{in}} \frac{Q_{CB}}{Q_{CSA}} = 20 \cdot 10 = 200 \tag{4.8}$$
$$G_{amp,n} = \frac{Q_{out}}{Q_{in}} = \frac{Q_{CSA}}{Q_{in}} \frac{Q_{PTA}}{Q_{CSA}} \frac{Q_{CB}}{Q_{PTA}} = 20 \cdot 0.67 \cdot 10 = 133 \tag{4.9}$$

where the factors stem from:

- $\frac{Q_{CSA}}{Q_{in}} = \frac{C_z}{C_f} = \frac{4\,\text{pF}}{0.2\,\text{pF}} = 20$
- $\frac{Q_{CB}}{Q_{CSA}} = \frac{W_{M_1}}{W_{M_4}}\Big|_{CB} = \frac{150\,\mu\text{m}}{30\,\mu\text{m}} = 10$
- $Q_{PTA}/Q_{CSA} \approx 0.67$ in the n-configuration is due to the $2/3$ aspect ratio of the output current mirror of the n-network of the peaking time adjuster stage (see 3.1.1.3)

A detailed study of the charge amplification of each block has been performed and the results of the simulations are reported below.

1. **Charge Sensitive Amplifier**
   As mentioned above, the amplification coming from the very first stage is due to the ratio between the capacitance C_z at the output of the charge sensitive amplifier and the CSA feedback capacitance C_f. The result of the performed simulations is shown in figure 4.2.

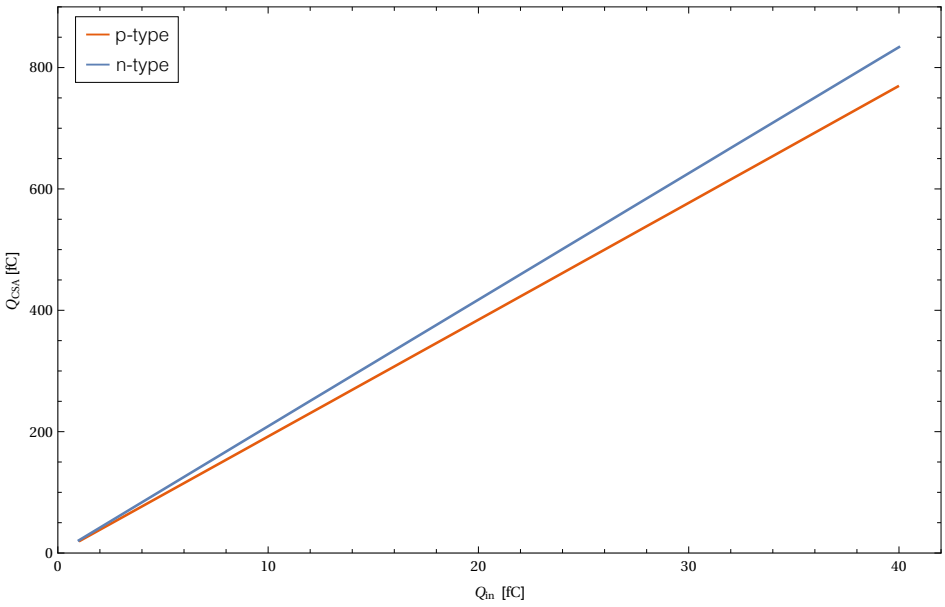


Figure 4.2: Charge amplification between the input and the output of the charge sensitive amplifier.

It can be observed that the charge amplification is linear and slightly higher for the n-configuration. In particular, the gains in charge given, as in the linearity study, by the slope of the linear fit, are:

$$\frac{Q_{CSA}}{Q_{in}}(p) = 19.25 \tag{4.10}$$

$$\frac{Q_{CSA}}{Q_{in}}(n) = 20.84 \tag{4.11}$$

2. **Peaking Time Adjuster**
   The result of the simulations performed on this sub-stage of the PASTA preamplifier are shown in figure 4.3.

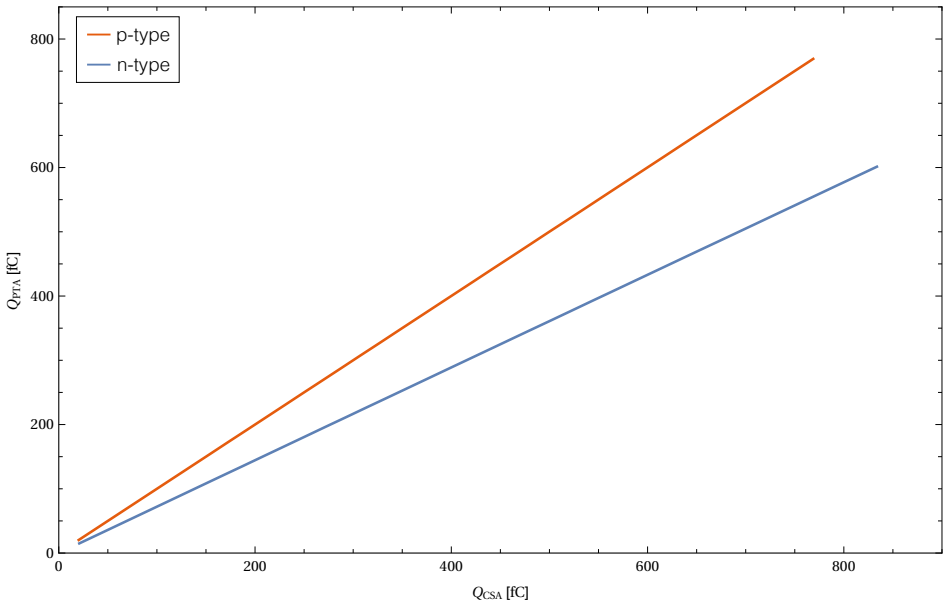


Figure 4.3: Charge amplification between the charge sensitive amplifier and the peaking time adjuster.

In this case, the gain in the p-configuration is much higher, but this is due to the already discussed $2/3$ ratio between the transistors building the current mirror of the n-network of the peaking time adjuster. The effect of this architectural choice can be noticed looking at the slopes of the linear fits:

$$\frac{Q_{PTA}}{Q_{CSA}}(p) = 1.00 \tag{4.12}$$

$$\frac{Q_{PTA}}{Q_{CSA}}(n) = 0.72 \tag{4.13}$$

3. **Current Buffer**
   The last stage where a charge amplification is expected is the current buffer. The simulated performance of this stage are shown in figure 4.4.

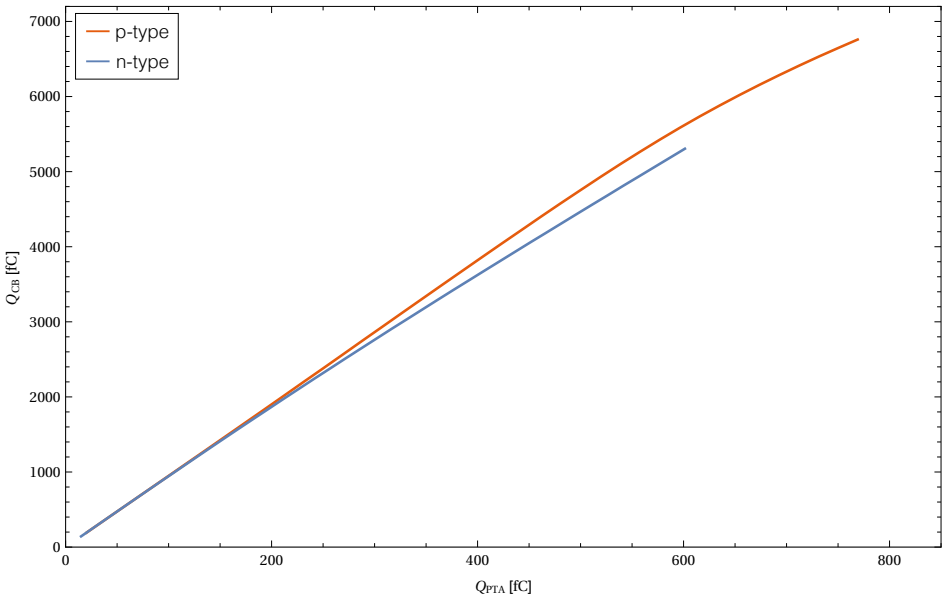


Figure 4.4: Charge amplification between the peaking time adjuster and the current buffer.

In this case a non-linearity can be observed in the p-configuration for high charges, while in the n-configuration the compression is much less pronounced. The slopes of the linear fits in this case would not give a reliable information on the charge amplification, hence the number of points considered for the fit has been reduced until an intercept close to zero is reached. The results of this analysis are:

$$\frac{Q_{CB}}{Q_{PTA}}(p) = 9.52 \tag{4.14}$$

$$\frac{Q_{CB}}{Q_{PTA}}(n) = 9.19 \tag{4.15}$$

In both configurations, the slope of the fit is comparable with the expected value of 10 given by the main transistors of the current buffer.

4. **ToT Stage**
   The time over threshold stage is not supposed to provide charge amplification. The results of the studies on this stage are reported in figure 4.5

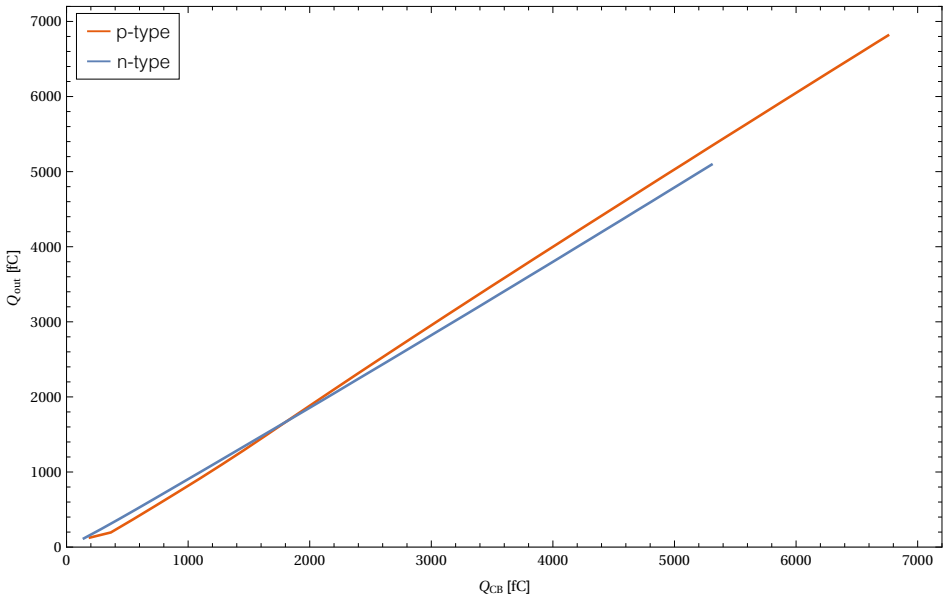


Figure 4.5: Charge amplification between the current buffer and the ToT stage.

The plot shows the presence of a non-linearity in the p-configuration for low charges. Hence, even in this case, a lower number of points has been considered for the linear fit and the slopes obtained are the following:

$$\frac{Q_{out}}{Q_{CB}}(p) = 1.04 \tag{4.16}$$

$$\frac{Q_{out}}{Q_{CB}}(n) = 0.97 \tag{4.17}$$

Finally, with the data collected with this analysis, the charge amplification of the whole chain is shown in figure 4.6. The compression for high charges introduced in the current buffer can be noticed especially for the p-strips configuration. The reason for this difference is in the intrinsic charge gain of this configuration with respect to its counterpart. In fact, the slopes of the two linear fits (with a proper amount of points considered) are:

$$\frac{Q_{out}}{Q_{in}}(p) = 190.31 \tag{4.18}$$

$$\frac{Q_{out}}{Q_{in}}(n) = 129.56 \tag{4.19}$$

The ratio between the expected values $Q_{amp,th}$ and the one obtained with the data analysis $Q_{amp,data}$ gives the following percentage errors:

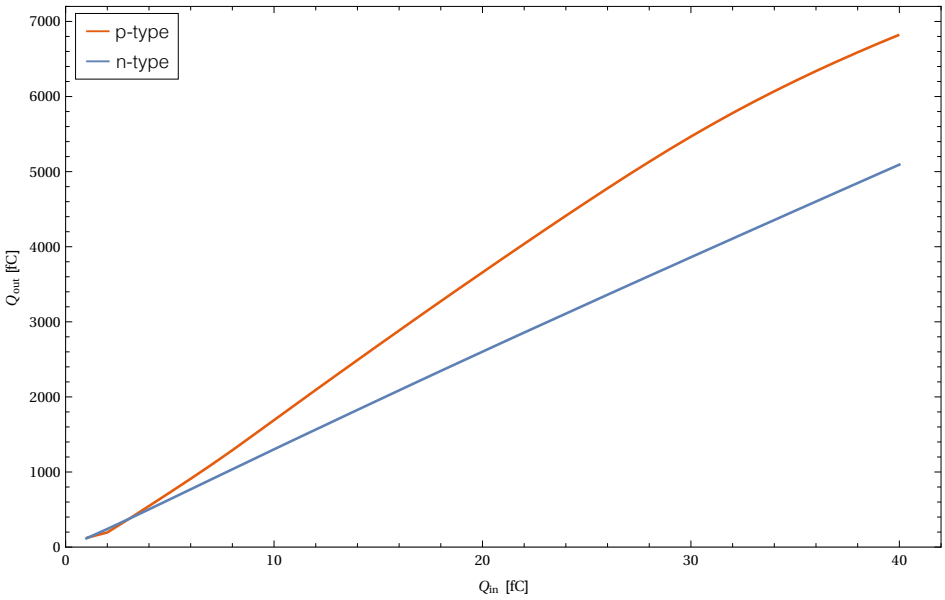


Figure 4.6: Charge amplification of the PASTA front-end amplifier.

$$\frac{Q_{amp,exp} - Q_{amp,data}}{Q_{amp,exp}}(p) = 4.85\,\% \tag{4.20}$$

$$\frac{Q_{amp,exp} - Q_{amp,data}}{Q_{amp,exp}}(n) = 2.59\,\% \tag{4.21}$$

4.3 Process Corners

The manufacturing process cannot guarantee an absolute precision of the key parameters defining the characteristic of the transistors. Process corners represent the extremes of the variations occurring to these parameters. A circuit running on devices fabricated at these process corners may run slower or faster than specified and at lower or higher voltages, hence it is necessary to simulate the behaviour of the chip under these extreme conditions. The figure of merit chosen to estimate to characterize the front-end amplifier is the linearity of the time over threshold with respect to the input charge. Figure 4.7 shows the simulated performance of the PASTA front-end amplifier in the condition where both pMOS and nMOS transistors are faster than their nominal speed and the voltage power supply is $V_{dd} = 1.3\,\mathrm{V}$ ($100\,\mathrm{mV}$ higher than the nominal value).

Two things can be noticed from the plot: a worsening of the linearity for high charges and an increasing of the ToT gain (especially for the p-strips). In particular, the percentage errors, calculated with (4.1), are:

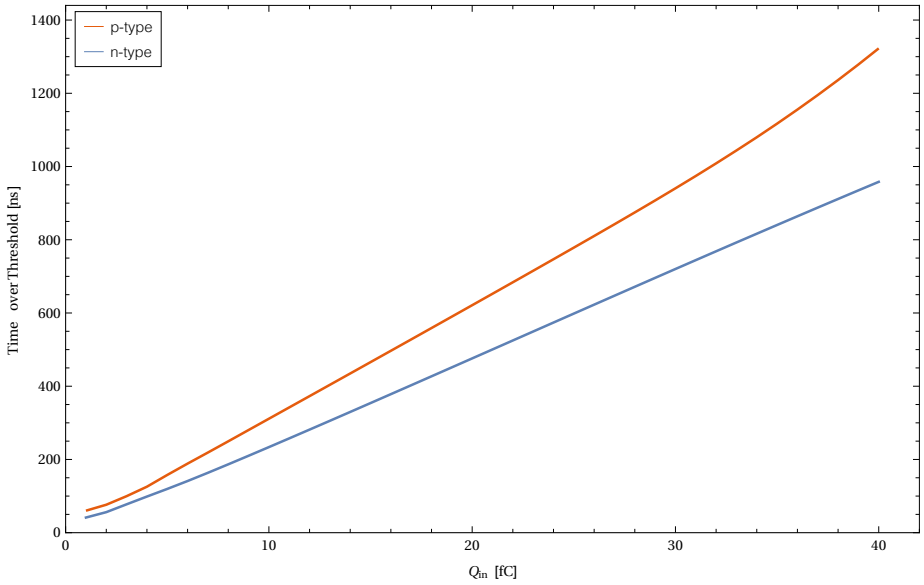


Figure 4.7: Time over threshold in the input charge range of 1 fC to 40 fC when all the transistors are faster than their nominal speed.

$$\sigma_{\%,\mathrm{ff}}(p) = 6.98\,\% \tag{4.22}$$
$$\sigma_{\%,\mathrm{ff}}(n) = 3.53\,\% \tag{4.23}$$

while the gains:

$$G_{\mathrm{ff}}(p) = 32.10\,\mathrm{ns/fC} \tag{4.24}$$
$$G_{\mathrm{ff}}(n) = 23.98\,\mathrm{ns/fC} \tag{4.25}$$

yielding to:

$$ToT_{max,\mathrm{ff}}(p) \approx 1300\,\mathrm{ns} \tag{4.26}$$
$$ToT_{max,\mathrm{ff}}(n) \approx 950\,\mathrm{ns} \tag{4.27}$$

The same simulations have been performed in the condition of slower devices and lower voltage power supply $V_{dd} = 1.1\,\mathrm{V}$. The results are shown in figure 4.8 and required the setting of a higher threshold since, with the default settings the lower threshold of the hysteresis comparator was lower than the baseline voltage. In this case, the gain is similar to the nominal condition, but it can be noticed a much more pronounced worsening in the linearity for low charges with respect to the standard situation. On the other hand, the linearity improves for high charges and this is confirmed by the following results:

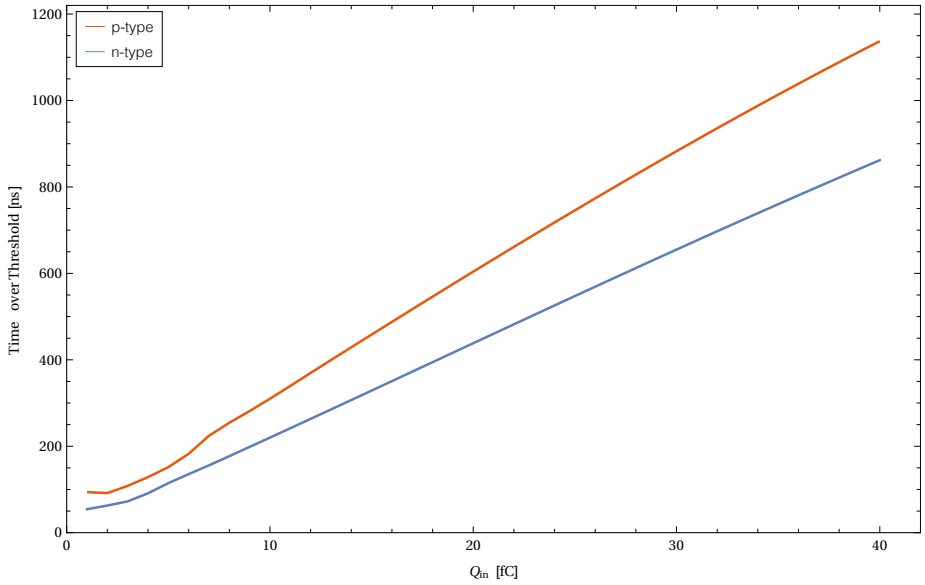


Figure 4.8: Time over threshold in the input charge range of 1 fC to 40 fC when all the transistor are slower than their nominal speed.

$$\sigma_{\%,\mathrm{ff}}(p) = 3.29\,\% \tag{4.28}$$
$$\sigma_{\%,\mathrm{ff}}(n) = 3.11\,\% \tag{4.29}$$

The percentage errors are lower than the one estimated for the fast case, meaning that the non-linearity observed for low charges is compensated by the better behaviour for high charges. The time over threshold gains in this case are:

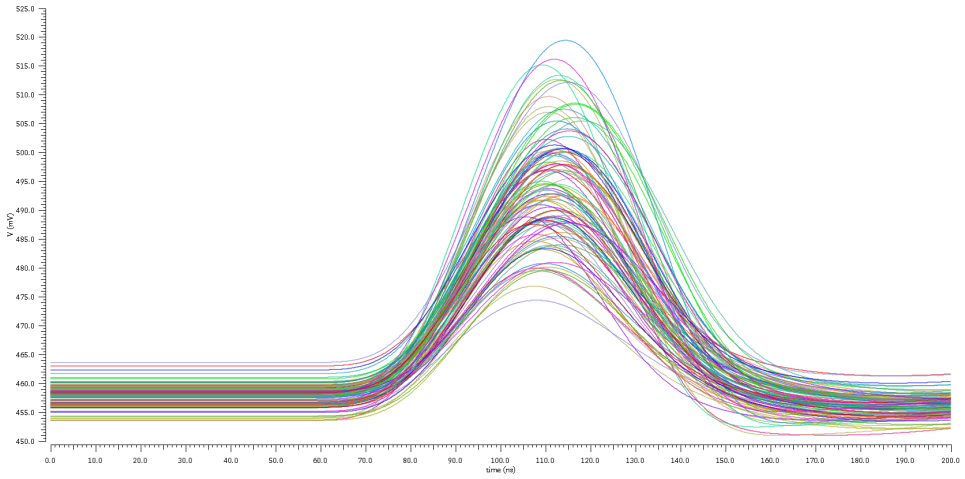
$$G_{\mathrm{ss}}(p) = 28.07\,\mathrm{ns/fC} \tag{4.30}$$
$$G_{\mathrm{ss}}(n) = 21.39\,\mathrm{ns/fC} \tag{4.31}$$

leading to:

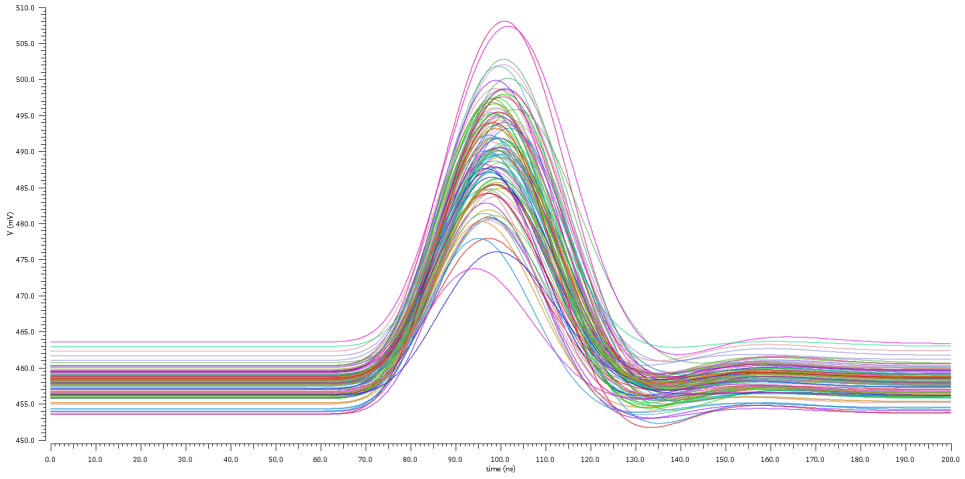
$$ToT_{max,\mathrm{ss}}(p) \approx 1100\,\mathrm{ns} \tag{4.32}$$
$$ToT_{max,\mathrm{ss}}(n) \approx 850\,\mathrm{ns} \tag{4.33}$$

4.4 Monte Carlo Simulations

During the manufacturing of integrated circuits, small random variations occur in the characteristics of devices designed to be identical. These *mismatches* yield to unexpected behaviours of both analog and digital circuitry. Since such variations affect differently each device, it is difficult to analytically predict their effect. Hence, a more sophisticated method is needed and that is why one of the most useful tools to characterize an ASIC is represented by the Monte Carlo simulations. By analysing a large set of circuit



(a) p-strips configuration



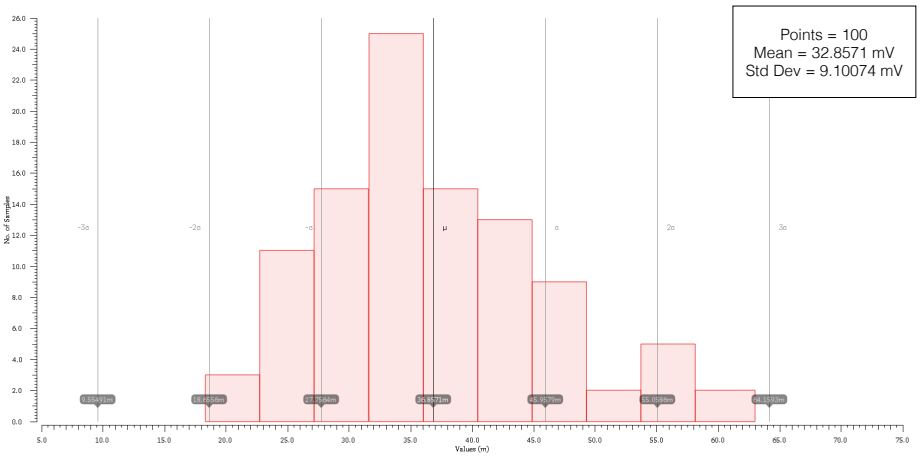
(b) n-strips configuration

Figure 4.9: Monte Carlo simulation (100 runs) of the PASTA front-end amplifier response to an input charge $Q_{in} = 1\,\text{fC}$ in presence of mismatch variations.

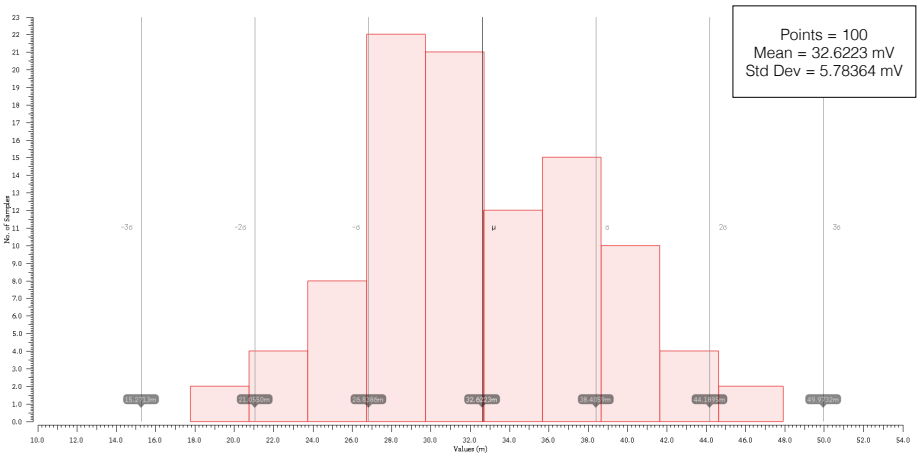
instantiations with randomly varied devices, it is possible to predict the impact of mismatch variations and try to mitigate them with proper design techniques. Figure 4.9 shows the shape variations occurring at the output of the front-end amplifier when an input charge of $1\,\text{fC}$ is injected.

Three figures of merit have been chosen to estimate the effects of the mismatches between identically designed devices: the amplitude, the rms noise, and the time over threshold.

1. **Amplitude**
   Since the ToT amplifier does not saturate for low input charges, the amplitude of its output signal can be used to evaluate the mismatch variations. Figure 4.10 shows the histograms obtained with 100 Monte Carlo runs.



(a) p-strips configuration



(b) n-strips configuration

Figure 4.10: Monte Carlo simulation (100 runs) of the amplitude of the PASTA front-end amplifier response to an input charge $Q_{in} = 1\,\mathrm{fC}$ in presence of mismatch variations.

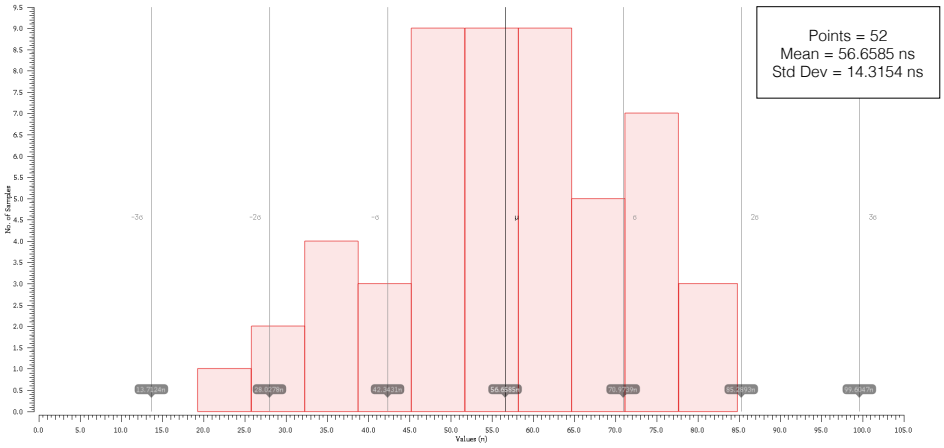
The percentage errors for the p- and n-strips configurations are, respectively:

$$\frac{\sigma}{\mu}(p) = 24.7\,\% \tag{4.34}$$

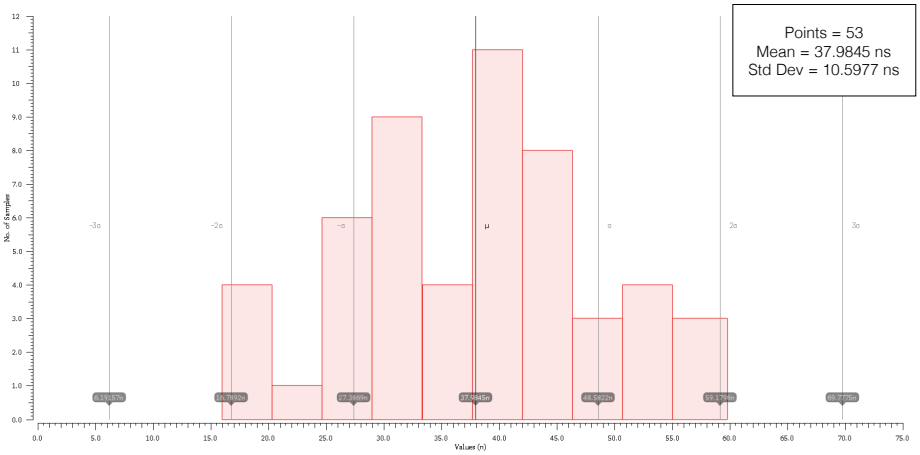
$$\frac{\sigma}{\mu}(p) = 17.7\,\% \tag{4.35}$$

The effects of these variations in the amplitude of the signal fed to the hysteresis comparator are discussed in the next paragraph.

2. **Time over threshold**
   The time over threshold is one of the most important parameters to observe in the PASTA front-end amplifier. The results of 100 Monte Carlo runs are shown in figure 4.11



(a) p-strips configuration



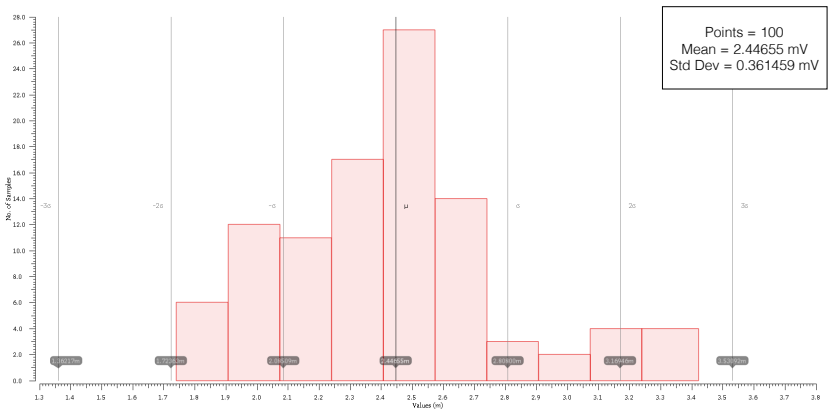
(b) n-strips configuration

Figure 4.11: Monte Carlo simulation (100 runs) of the time over threshold of the PASTA front-end amplifier response to an input charge $Q_{in} = 1\,\text{fC}$ in presence of mismatch variations.

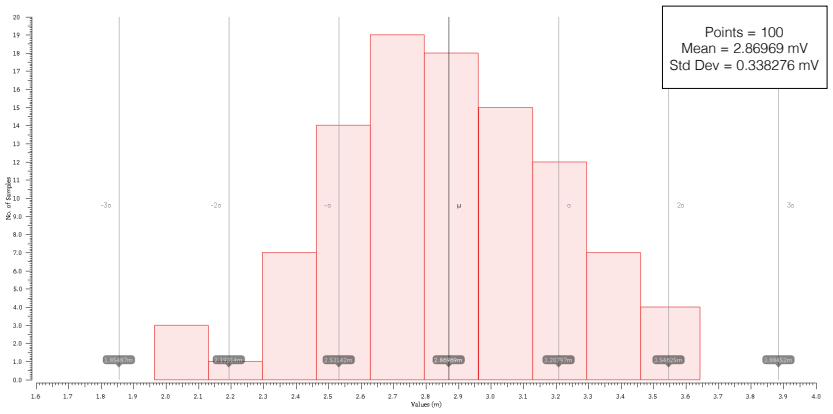
The first thing to notice from the histograms is that even if 100 runs

have been performed, i.e. 100 signals have been fed to the discriminator, only about half of them produces a measurement. This means that the variations of the amplitude are such that in some cases the input charge of $1\,\mathrm{fC}$ cannot be detected. Therefore, two different kinds of digital to analog converters have been implemented to set the threshold of the two hysteresis comparators of each channel (time and energy branches): two global and one digital DACs. The global configuration sets the values of V_{TH+} and V_{TH-} (see 3.1.4), while the local DACs allow a finer tuning ($\mathcal{O}\,(\mathrm{mV})$).

3. **Noise**
   The last figure of merit taken into account is the rms noise. In figure 4.12 the histograms for the two polarities are reported.



(a) p-strips configuration



(b) n-strips configuration

Figure 4.12: Monte Carlo simulation (100 runs) of the time over threshold of the PASTA front-end amplifier response to an input charge $Q_{in} = 1\,\mathrm{fC}$ in presence of mismatch variations.

The corresponding equivalent noise charges are:

$$ENC(p) = 414 \pm 119 \,\text{electrons} \tag{4.36}$$
$$ENC(n) = 549 \pm 117 \,\text{electrons} \tag{4.37}$$

The errors have been obtained propagating the standard deviations of the rms noise and the amplitude according to the following relationship:

$$\sigma_{ENC} = \sqrt{\left(\frac{\partial ENC}{\partial V_{rms}}\right)^2 \sigma^2_{V_{rms}} + \left(\frac{\partial ENC}{\partial Amp}\right)^2 \sigma^2_{Amp}} \tag{4.38}$$

4.5 Temperature

Another important parameter whose variations may lead to unexpected behaviours is the temperature. The figure of merit chosen is, once again, the linearity of the time over threshold in the nominal input charge range. The performance with three different temperatures have been evaluated:

1. **Temperature** $T = 0\,^{\circ}\text{C}$

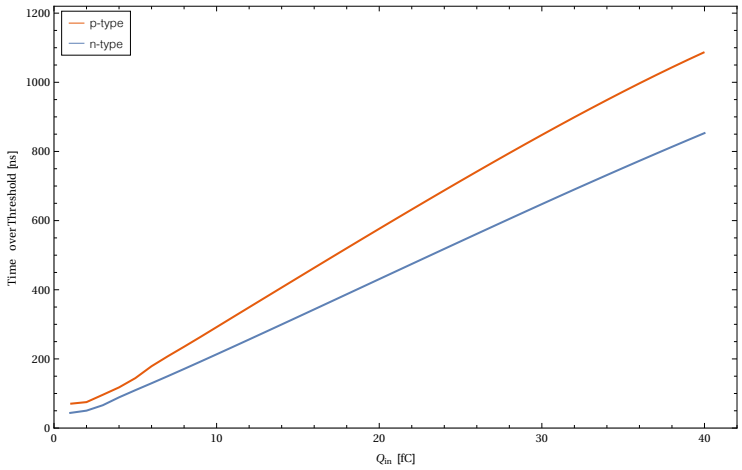


Figure 4.13: Time over threshold in the input charge range of $1\,\text{fC}$ to $40\,\text{fC}$ with temperature $T = 0\,^{\circ}\text{C}$.

$$\sigma_{\%,0\,^{\circ}\text{C}}(p) = 2.93\,\% \tag{4.39}$$
$$\sigma_{\%,0\,^{\circ}\text{C}}(n) = 2.79\,\% \tag{4.40}$$

2. **Temperature** $T = 50\,^{\circ}\mathrm{C}$

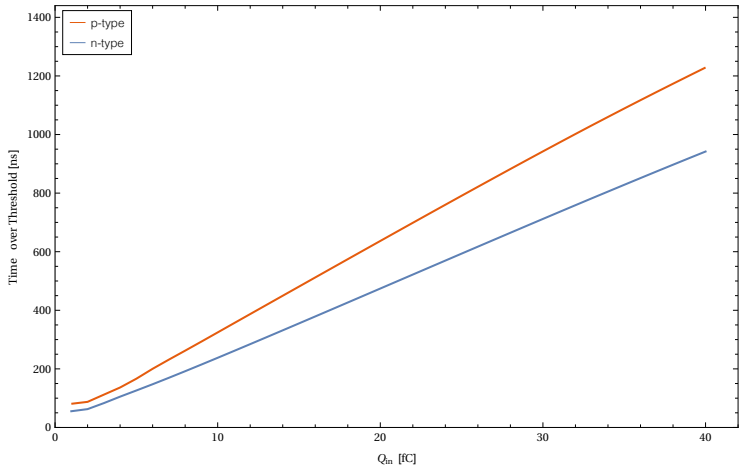


Figure 4.14: Time over threshold in the input charge range of $1\,\mathrm{fC}$ to $40\,\mathrm{fC}$ with temperature $T = 50\,^{\circ}\mathrm{C}$.

$$\sigma_{\%,50\,^{\circ}\mathrm{C}}(p) = 2.28\,\% \tag{4.41}$$

$$\sigma_{\%,50\,^{\circ}\mathrm{C}}(n) = 2.83\,\% \tag{4.42}$$

3. **Temperature** $T = 100\,^{\circ}\mathrm{C}$

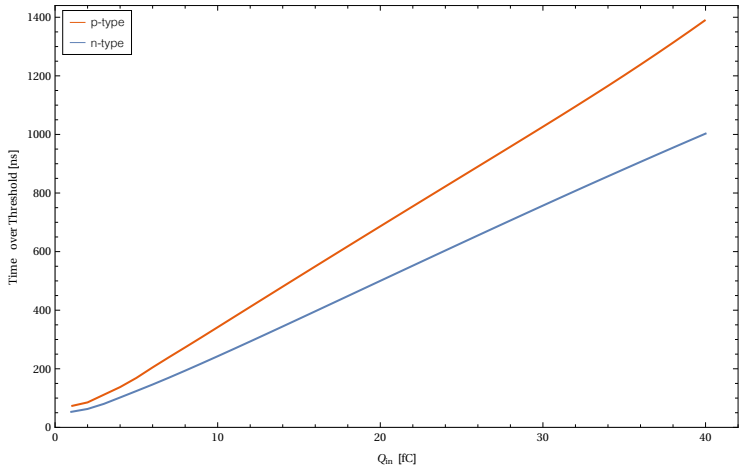


Figure 4.15: Time over threshold in the input charge range of $1\,\mathrm{fC}$ to $40\,\mathrm{fC}$ with temperature $T = 100\,^{\circ}\mathrm{C}$.

$$\sigma_{\%,0\,^{\circ}\mathrm{C}}(p) = 3.57\,\% \tag{4.43}$$

$$\sigma_{\%,0\,^{\circ}\mathrm{C}}(n) = 4.89\,\% \tag{4.44}$$

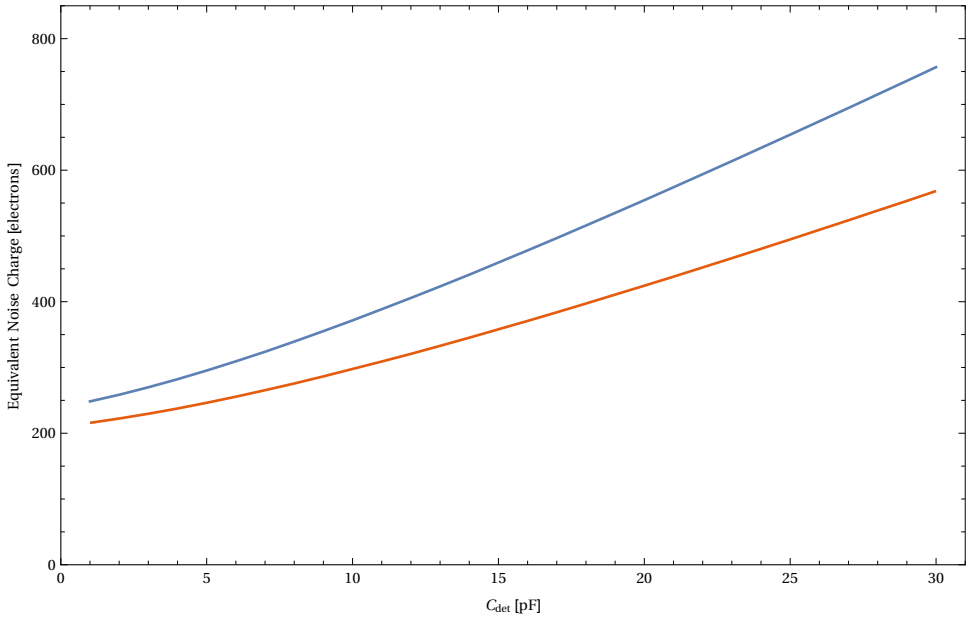


Figure 4.16: Equivalent noise charge of the PASTA front-end amplifier response to an input charge $Q_{in} = 1\,\mathrm{fC}$ with input capacitance ranging from $1\,\mathrm{pF}$ to $30\,\mathrm{pF}$.

Observing the percentage errors of each linear fit, it can be concluded that even if the ASIC is supposed to work at room temperature (default value for simulations is $T = 27\,^{\circ}\mathrm{C}$), eventual temperature variations would not affect drastically its performance.

4.6 Noise

Together with the linearity of the time over threshold with respect to the input charge, the most important analysis regards the equivalent noise charge (ENC) in relation with the input capacitance. In fact, as introduced in section 1.4, the micro strip sensors of the $\bar{\mathrm{P}}$ANDA Micro Vertex Detector come in different shape and size depending on where they are placed (barrels or disks). Therefore, the input capacitance has been varied in a range 1–$30\,\mathrm{pF}$ (see figure 4.16).

The percentage errors for a linear fit are:

$$\sigma_{\%}(p) = 2.36\,\% \tag{4.45}$$

$$\sigma_{\%}(n) = 2.36\,\% \tag{4.46}$$

The plot shows that for both configurations, the electronic noise is lower than $800\,\mathrm{electrons}$ for detectors with input capacitance up to $30\,\mathrm{pF}$. Taking into account that the maximum measured capacitance for the strips is $17\,\mathrm{pF}$, the performance of PASTA are even more remarkable with an estimated equivalent noise charge below $600\,\mathrm{electrons}$ for both p- and n-type strips.

4.7 Comparator Jitter

As introduced in section 2.1.4, the noise of the front-end amplifier yields to an uncertainty in the threshold crossing time called timing jitter. An estimation of this parameter has been done using the following relationship:

$$\sigma_t = \sqrt{\left(\frac{v_n}{\frac{\partial v_{out}}{\partial t}}\right)^2_{LE} + \left(\frac{v_n}{\frac{\partial v_{out}}{\partial t}}\right)^2_{TE}} \tag{4.47}$$

where v_n is the rms noise and the subscripts LE and TE refers to the leading and the trailing edges of the output signal of the front-end amplifier, respectively. For the two available configurations, the results are:

$$\sigma_t(p) = 3.34\,\text{ns} \tag{4.48}$$
$$\sigma_t(n) = 2.93\,\text{ns} \tag{4.49}$$

The jitter can also be used to give an evaluation of the signal-to-noise ratio:

$$SNR_t(p) = \frac{ToT(p)}{\sigma_t(p)} \approx 23 \tag{4.50}$$
$$SNR_t(n) = \frac{ToT(n)}{\sigma_t(n)} \approx 18 \tag{4.51}$$

It is interesting to notice that this result is different with respect to the one obtained dividing the amplitude of the signal and the rms noise:

$$SNR_v(p) = \frac{Amp(p)}{v_n(p)} \approx 15 \tag{4.52}$$
$$SNR_v(n) = \frac{Amp(n)}{v_n(n)} \approx 11 \tag{4.53}$$

The most important remark is that despite the formula used, the SNR is >10 for both input polarities which is a common threshold used to estimate the performance of an amplifier.

Chapter 5

Conclusions

This thesis aims at describing the design of the $\bar{\text{P}}$ANDA Strip ASIC (PASTA), the prototype developed to read out the micro strip sensors of the $\bar{\text{P}}$ANDA Micro Vertex Detector (MVD). The research work presented have been performed in the context of the $\bar{\text{P}}$ANDA experiment, hence an overview on the physics program and the experimental setup has been given in chapter 1 with particular focus on the MVD. Moreover, since the main subject of this document is the design of an ASIC, chapter 2 provide basics electronics theory to help the reader in the comprehension of the discussed topics.

The core of this thesis is the implementation of the front-end amplifier of the PASTA chip, therefore it can be considered as part of the work presented in the PhD theses of Alberto Riccardi and André Zambanini [78,2] describing the development of the analog time to digital converter and the digital blocks of the ASIC, respectively.

During the very first stages of the design process, a time-based approach was identified as the most suitable because it offered the advantage to benefit from the remarkable performance of the Time of Flight for Positron Electron Tomography (TOFPET) ASIC [63]. This chip was developed as a readout solution for scintillating crystals for the EndoTOFPET-US project jointly exploiting the technologies of Time of Flight (TOF) in a positron emission tomography (PET) experiment with ultrasound (US) endoscopy to increase detection efficiency in medical examinations of cancerous patients [79]. However, since TOFPET was designed to serve Silicon Photo Multipliers (SiPMs), the development of a new architecture for the $\bar{\text{P}}$ANDA strip sensors readout chip became necessary.

A detailed description of the building blocks of the PASTA front-end amplifier is provided in chapter 3. The most important design goals driving the development of the implemented architecture are: the linearity of the signals duration with respect to the input charge and a low electronic noise. Non-linear systems could also be considered since they are easier to design from the electronics point of view, however the calibration of such systems can be cumbersome and that is why it is preferable to achieve a linear relationship between the input and the output parameters. For what concerns the electronic noise, the specifications of the detector demand a maximum output noise in the order of orderof$1000\,\text{electrons}$, therefore the results of the simulations are promising since the expected performance foresee an equivalent noise charge lower than $800\,\text{electrons}$ even for high detector capacitances up to $30\,\text{pF}$.

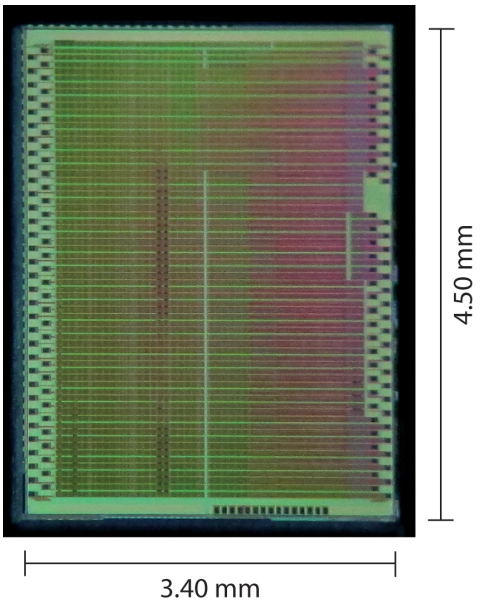


Figure 5.1: Photograph of a PASTA prototype.

The design of the chip was submitted in April 2015 and the first prototypes were returned from the foundry at the beginning of October 2015 (figure 5.1). The development of a readout system is still ongoing, but the first tests are being performed in these months. Two different setup are available to characterize the ASIC: the first, and probably most reliable, has been developed and thoroughly used to evaluate the performance for both ToPix and TOFPET, while the second is a brand new project aiming at being a multi-purpose evaluation system reusable for a wide variety of different front-ends [2]. The preliminary tests already performed suggests that a beam test is the next step, but possible new features to improve the design have already been identified.

The first goal of the second design phase is, of course, to further improve the performance in terms of linearity and electronic noise. To achieve a better linearity in the low charge region, an architecture foreseeing a dynamic $I_{f,ToT}$ will be explored. As discussed in section 3.1.3.1, the constant current discharging the feedback capacitance in the ToT stage is a crucial parameter influencing the output linearity: a low current yields to higher amplitudes of the signals fed to the discriminators at the cost of longer times over threshold; on the other hand, higher values reduce the deadtime of the chain worsening the signal-to-noise-ratio. Therefore, a dynamic system providing a low current during the rising of the signals and higher values during its falling would lead to faster signals with sharper trailing edges (i.e. lower jitter) without affecting the performance of the amplification stage in terms of amplitude gain. As regards the noise, the low power consumption of the chip (lower than the limit imposed by the specifications deriving from the cooling system design) allow to increase the current of the input stage. In particular, this possibility will be tested directly on the prototype thanks a dedicated pad designed to force an external source into the additional biasing branch of the front-end charge sensitive amplifier.

Moreover, to adapt the performance of the ASIC to the different phases of the experiments in terms of radiation doses, the flexibility of two building blocks of the front-end amplifier can be enhanced. First, the values of the capacitances increasing the peaking time in the preamplifier stage can be made adjustable to regulate this important value according to the degradation of the sensors. The other block offering the possibility to customize a crucial parameter is the hysteresis comparator, in fact the separation between the upper and the lower thresholds depends on the aspect ratio of the cross-coupled transistors of the discriminator (see 3.1.4).

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